Thermal Investigation of GaAs Microwave Power Transistors

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Abstract

The lower thermal conductivity of gallium arsenide (GaAs) compared to silicon (Si) requires a careful thermal design for optimizing device performance and reliability. In this paper a recently developed thermal simulation tool (TRESCOM II) is applied for investigating the thermal behavior of a heterojunction GaAs power field effect transistor (FET). Main features of the simulation tool are an easy model creation procedure and an efficient numerical solver. Moreover, the tool allows to consider temperature dependent material properties and temperature dependent boundary conditions. The investigation of the thermal behavior of the power transistor has two goals. First goal is to establish the temperature distribution within the active layer of the FET to allow predictions of thermal-electrical interactions. A deeper insight into thermal-electrical interaction will lead to better equivalent circuit models used in electrical circuit design. Due to the fact that reliability of the component is mainly determined by thermal load and induced thermomechanical stress, second goal of this work is to investigate the influence of chip thickness and die bonding variations on the thermal behavior. Thermal response on different power levels is investigated and the influence of chip thickness tolerances and die bonding on the thermal performance of the device is discussed.

Introduction

Wireless communication and advanced radar systems require circuitry that can operate at frequencies greater than 2 GHz and at high power levels [1]. Due to the several times higher peak average electron velocity and mobility in gallium arsenide (GaAs) compared to silicon (Si), GaAs technology plays an important role in achieving sufficient high frequency performance [2]. However, due to the low thermal conductivity of GaAs (46 W/mK at 300 K, figure 1) compared to that of Si (148 W/mK at 300 K) thermal characterization of GaAs devices becomes a major task.

The investigation of the thermal behavior of the device is important for two reasons. Firstly, electrical parameters like phase shift, output power, efficiency, and gain vary with temperature. For this reason particularly GaAs power transistors need the development of advanced models taking into account the dependencies of electrical characteristics from the local temperature distribution within the structure [4]. Secondly, the investigation of the thermal performance is needed to improve lifetime and reliability of the device by minimizing the influence of thermomechanically induced stress and thermal load. Heat generation within a GaAs power transistor is concentrated in a few small discrete locations. This in combination with the low thermal conductivity results in large thermal gradients. High effort is required for measuring temperature distributions of power transistors with the required resolution at such small scales [1].

The number of measurements can be reduced significantly using thermal simulation. In this paper a thermal simulation tool (TRESCOM II) is presented and applied for the thermal characterization of GaAs heterojunction power FETs. The tool developed at our institute is based on an efficient model creation procedure and allows to generate and maintain

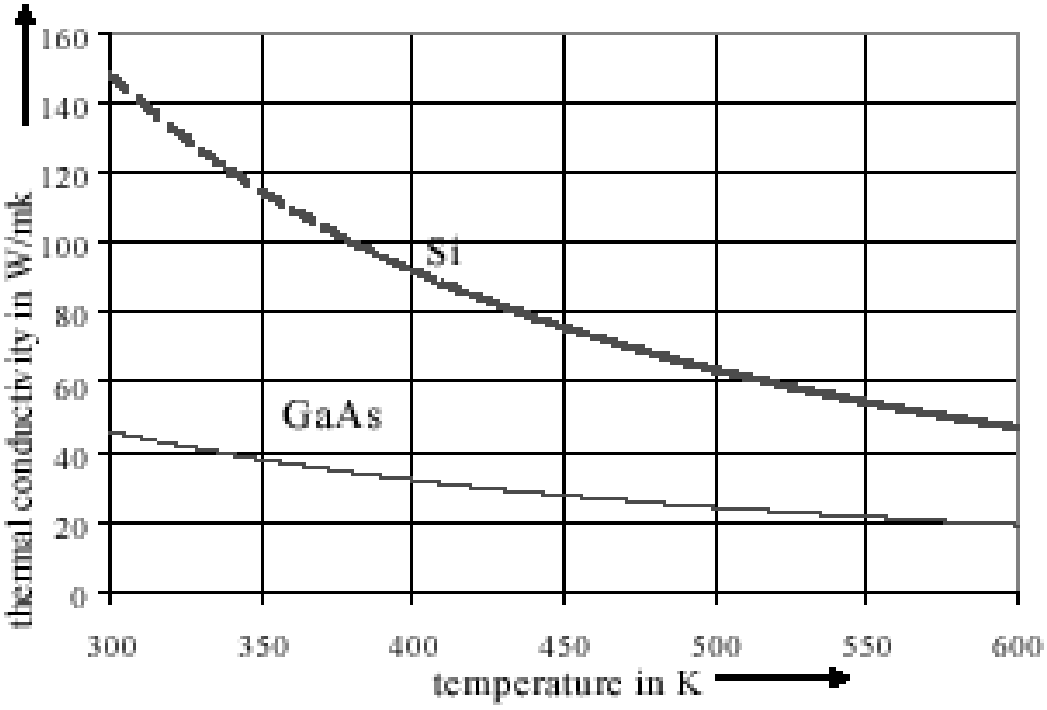

Figure 1: Temperature dependent thermal conductivity of silicon (Si) and gallium arsenide (GaAs) [1].

models in short time. Thermal parameters of common materials are implemented in a material database. The developed solver based on an alternating direction implicit (ADI) algorithm is efficiently processing high node numbers (up to several 10^6) for computing nonlinear steady-state and unsteady-state heat transfer problems including the consideration of temperature dependent material parameters and boundary conditions [5, 6].

The Investigated GaAs FET

Figure 2 shows a microscopic view of the structure of the investigated GaAs power transistor (Excelics EPA480CV). The transistor consists of 20 parallel gates with 4800 µm total width and 0.5 µm gate length. The lateral chip dimension is 680 µm x 620 µm, the chip thickness is 75 µm (±13 µm). The depth of the conducting channel is 0.3 µm. Metallization thickness is 0.3 µm over the gates and 2.6 µm elsewhere. Gate and source metallizations are electrically insulated using air bridges. Main dimensions of the chip layout are given in figure 3. The chip is attached to a chip carrier using high thermal conductivity Ag/Epoxy adhesive silver paste (DIEMAT DM6030Hk). Main dimensions of the chip carrier are depicted in figure 4.

Experimental Set-up

Simulation results are compared to those established in experiments. In the experimental set-up chip and chip carrier are placed on a heat sink which is temperature controlled using a thermocouple for temperature measurement and peltier elements for heat removal. In this way a known and constant temperature is achieved as boundary condition at the bottom of the carrier while natural convection and heat radiation act as boundary conditions at other surfaces.

The direct measurement of chip temperatures is a difficult task [7]. For this reason integrated circuits are frequently provided with an additional diode which acts as a temperature sensor. [8]. However, this was not the case in our transistor.

Therefore, we fabricated miniaturized Au/Al thermocouples using 25 µm gauged wires. As a new approach the thermocouples were formed by wedge bonding the wires to the gold metallization of the chip (location T_CC in figure 8). The thermoelectric voltage between the Au and the Al wire is the measure for the local temperature. Since the thermoelectric voltage

(Seebeck coefficient) is strongly influenced on the composition of the involved materials and our Al wire is alloyed with 1% silicon for an improved bondability, we had to establish the Seebeck coefficient in a separated calibration measurement and found a value of approximately 4.6 µV/K (figure 5).

Modeling and Thermal Simulation

Main feature of the developed thermal simulation tool is an easy model generation and maintenance procedure. In our concept a model is established by dividing the investigated object into layers. For modeling the GaAs power FET assembly 15 layers are used (figure 6). Layer 1-4 are modeling the chip carrier (material: brass). Layer 5 considers the die attach layer of which the thermal conductivity has been varied to study the influence of die bonding on the thermal behavior of the chip. The GaAs power FET itself is modeled in layer 6-15: Due to the chip thickness tolerance (75 µm ± 13 µm) three different models were established. One with a chip thickness of 75 µm according to the nominal thickness and two models with the chip thickness of 62 µm and 88 µm according to the tolerance limits (layer 6-12). In our work it is assumed that heat is generated under the gate within the 0.3 µm thick channel and each channel generates an equal quantity of heat (layer 13). The last two model layers are considering the metallization with 0.3 µm thickness over the gates and 2.6 µm elsewhere.

After defining the layer structure of the model each layer is subdivided into volume elements (cells). Cell dimensions can be varied in all three dimensions to allow a non-uniform model discretization. The cell structure itself is designed using routines similar to polygon drawing functions in pixel oriented paint programs. Predefinable sets of material parameters can be assigned simply by filling the respective structure with a certain color. Table 1 lists the used materials and the their thermal properties. As depicted in this table, the temperature dependent thermal conductivity of GaAs was considered in our investigation using a simple power law. This approximation is in a good agreement with experimental data [3].

The model generation modul of our simulation tool allows to use digital images of the investigated object (e.g. digital photographs) as templates. Due to the fact, that one cell of our model is represented by one pixel, the size of the template is free scalable (width and height) to allow an optimal adjustment to the model space. In this way it is also possible to use templates whenever unequal cell dimensions in x- and y-direction are used.

Figure 7 shows the model generation modul of our simulation tool actually showing the metallization of the GaAs Fet (layer 14) using a photograph of the chip (Figure 2) as template (the gold structures are displayed in red). As depicted in this figure only one

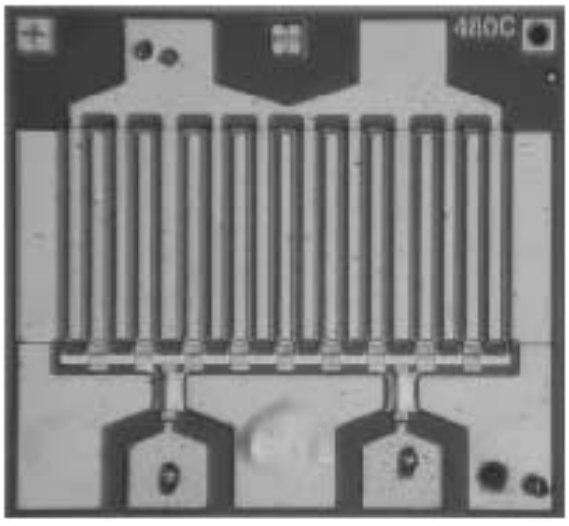

Figure 2: Microscopic view of the top side of the investigated GaAs power FET.

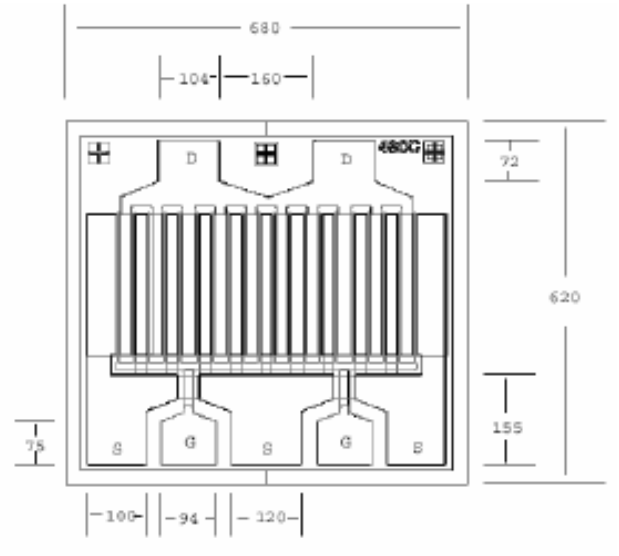

Figure 3: Main dimensions of the investigated GaAs power FET (in µm).

Table 1: Thermal properties of the used materials.

material	thermal conductivity in W/(m·K)	density in kg/m^3	spec. heat in J/(kg·K)
GaAs	$46 \cdot (T/300\ K)^{-1.25}$	8500	176
Au	295	19290	128
brass	113	8840	376
Al_2O_3	20	3780	800
Adhesive paste	30-60	2600	800

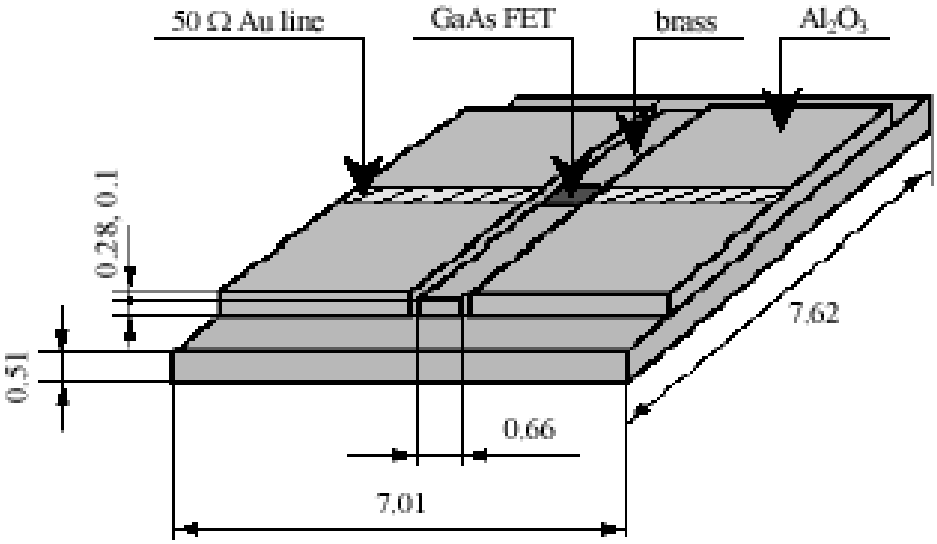

Figure 4: Main dimensions of the chip carrier (in mm).

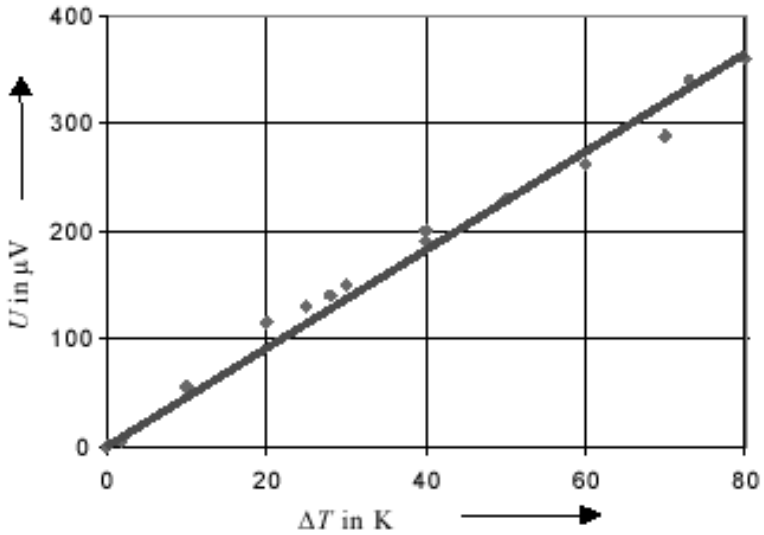

Figure 5: Result of the calibration measurement: Thermo-electric voltage U as a function of the difference T between thermocouple and reference temperature.

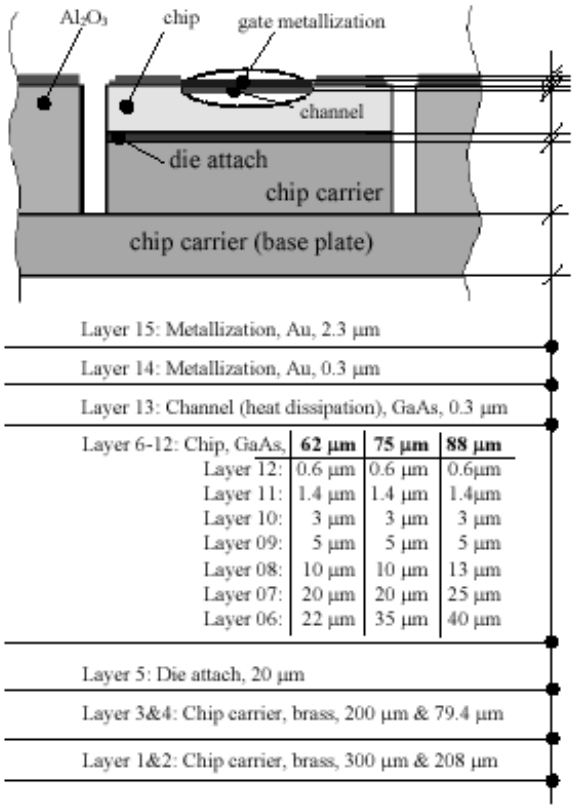

Figure 6: Layer structure of the GaAs power FET assembly.

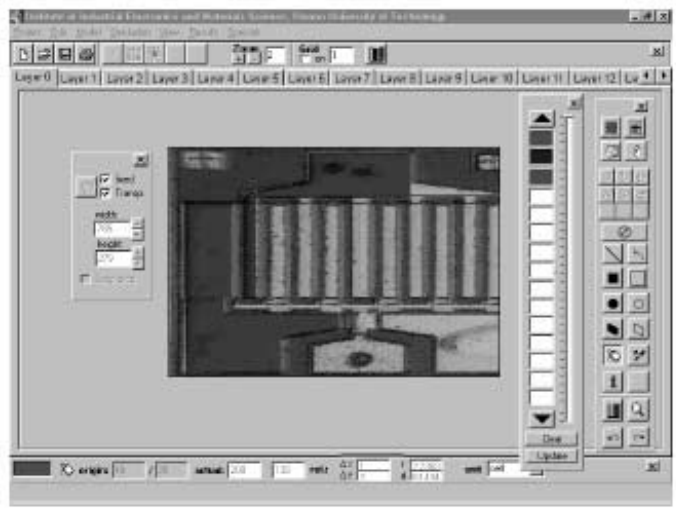

Figure 7: Model generation modul actually modeling the metallization of the GaAs Fet (layer 14) using a photograph of the chip (Figure 2) as template.

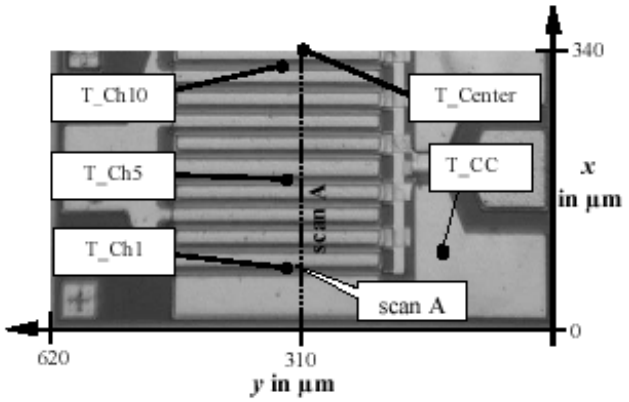

Figure 8: Significant points and line scans used for illustrating the thermal behavior of the transistor.

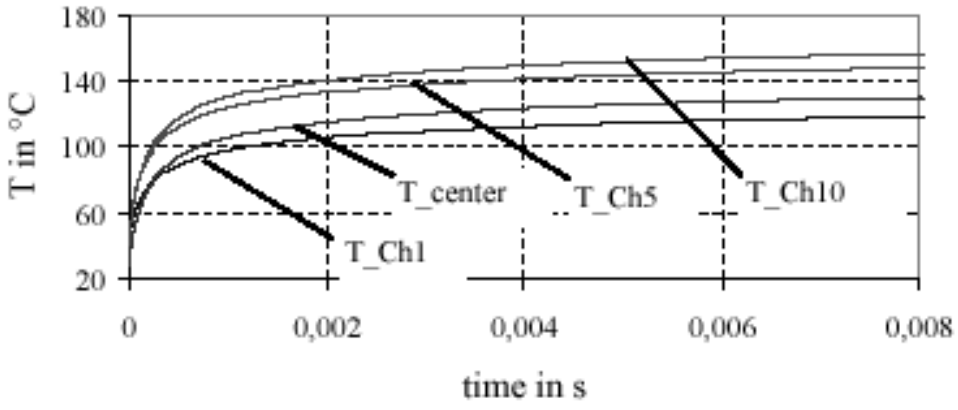

Figure 9: Temperature-versus-time functions at significant points (loss power: 4 W, chip attach: 30 W/mK, 20 µm thick).

half of the assembly has to be modeled due to the existing thermal symmetry.

For modeling the GaAs transistor two models with different discretization were established: The coarser model uses cells with with Δx = 2 µm and Δy = 6 µm edge length in x- and y-direction. This leads to a total number of 175 100 cells for modeling the chip. The finer model consists of cells with Δx = 1 µm and Δy = 3 µm edge length resulting in 700 400 cells for the whole model.

For both models, parts of the chip carrier which are not covered by the transistor are non-uniformly discretized using cells with an edge length from 1 µm to 600 µm. The resultant model of the chip and the carrier consists of $1.34 * 10^6$ volume elements for the finer model and $417 * 10^3$ cells for the coarser one.

The implemented solver of our simulation tool is based on the so called alternating-direction implicit method (ADI-method). The origin of the ADI-method goes back to the early sixties when Peaceman, Rachford and Douglas presented new finite difference methods for solving unsteady-state (parabolic) and steady-state (elliptic) problems (*Peaceman-Rachford method* [9], *Douglas-Rachford method* [10]). As a main advantage the presented methods require only the line-by-line solution of small sets of simultaneous equations that can be solved by a direct, non-iterative method. The general idea is to attack a multi-dimensional problem in such a way that only one-dimensional computations are required. This idea led to a variety of methods in the past decades. The effectiveness of ADI-methods is hard to generalize. However, considering the relative accuracy, the ease of programming, the computation time, and computer storage requirements, a comparison between nine numerical methods gave preference to ADI methods [11].

More details of the implemented solver and its application for computing heat transfer problems in the regime of electronic packaging can be found in e.g [5, 6].

Discussion of Results

For illustrating the thermal behavior of the power transistor, in the following section temperature-versus-time functions at significant points as well as a line scan of the temperature at the surface of the component are given (figure 8).

Figure 9 shows the thermal response on a power-on step of 4 W. In this simulation the nominal chip thickness of 75 µm and a thermal conductivity of the die attach adhesive of 30 W/mK were used (thickness of the adhesive layer: 20 µm). As depicted in this figure, temperature differences within the chip have reached their final levels after about 5 ms, after approximately 18 ms temperatures differ less then 1 K from their steady-state value. Figure 10 shows the temperatures along line scan A (figure 8) at different times calculated with the same parameters as before. The figure illustrates the strong temperature raise within the channels leading to enormous temperature gradients up to 10 K/µm. The curves for 1 µs and 10 µs show nearly equal maximum temperatures of the different channels. After 0.1 ms different peak channel temperatures occur which may lead to different currents in the channel.

The influence of varying chip thickness and thermal conductivity of the adhesive is depicted in figure 11 and figure 12 (ambient temperature: 25°C). Figure 11 shows the temperature-versus-time function at T_Ch10 for the nominal chip thickness value of 75 µm, the lower tolerance limit of 62 µm, and the upper limit of 88 µm. With increasing time temperature differences due to chip thickness variation are rising up to a value of approximately 20 K. In this simulation the power loss was 6 W, and 60 W/mK was assumed for the adhesive's thermal conductivity. Results for varying thermal conductivity are depicted in figure 12 (chip thickness: 70 µm). In this case also temperature differences of approximately 24 K were observed for a variation of the conductivity from 20 W/mK to 60 W/mK.

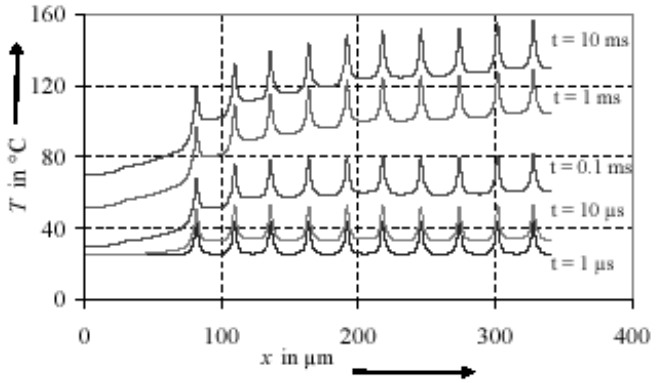

Figure 10: Temperatures along line scan A (figure 8) at different times (loss power: 4 W, chip attach: 30 W/mK, 20 µm thick).

Figure 13 shows the calculated steady-state temperatures along line scan A. As depicted in this figure, for increasing power loss the difference between the mean and the maximum temperature in the active layer increases and also the difference between the peak temperatures of the channels. This can also be observed in an increasing maximum thermal resistance from 28 K/W at P = 2 W to 35 K/W at P = 6 W while the mean thermal resistance only increases from 9.5 K/W at P = 2 W to 10.2 K/W at P = 6 W.

Frequently, the lower surface of the GaAs which is in contact with the die adhesive is metallized with a gold layer acting as a heat spreader (e.g. EPA1200A). For the investigated structure, a 20 µm thick gold heat spreader leads to a decrease of the maximum thermal resistance of about 10% while the mean thermal resistance remains nearly constant.

As already mentioned, simulation results were compared with those established in experiments. However, due to uncertainties concerning chip thickness and adhesive's thermal conductivity a direct comparison is difficult to achieve. Nevertheless a sufficient agreement for lower power levels but increasing deviations for a higher power loss were observed as listed in table 2. In this table we compared measured and calculated temperatures at point T_CC (location of the thermocouple) and defined the relative deviation δ of calculated temperature T_s (in K) from measured temperatures T_m (in K) as $\delta = (T_s - T_m) / T_m * 100$, in per cent.

The higher deviation for increasing power loss can be explained due to the fact that in our simulation equal heat generation was assumed in all channels. However, due to the negative temperature coefficient (TC) of GaAs FETs an increasing temperature decreases the current in the respective channel leading to an overall unequal power distribution. Due to a constant total power and unequal power distribution, channels near the edge generate comparatively more power than the inner one resulting in a higher temperature at the thermocouple location. In future works we will implement the negative TC to obtain a sufficient agreement also for higher power levels.

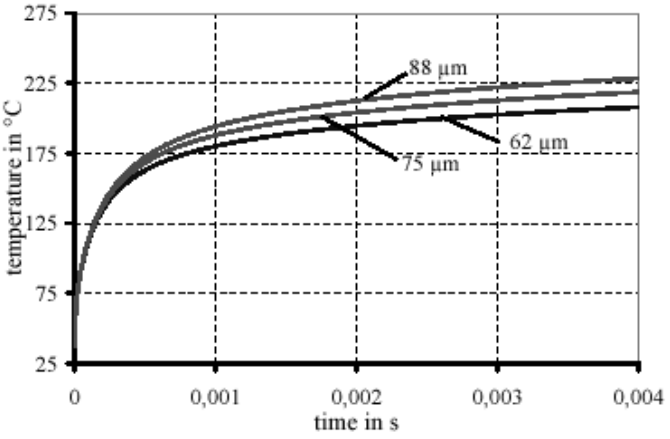

Figure 11: Temperature-versus-time functions at T_Ch10 for varying chip thickness.

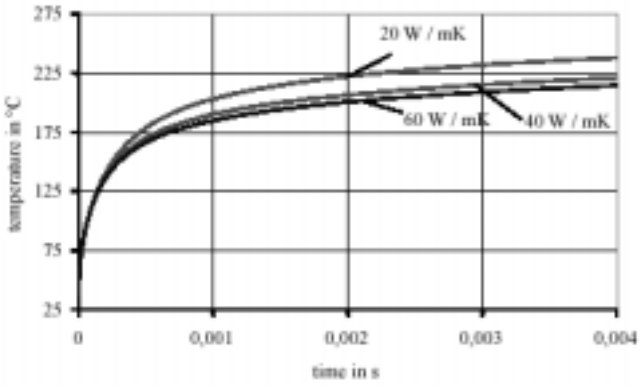

Figure 12: Temperature-versus-time functions at T_Ch10 for varying thermal conductivity of the adhesive.

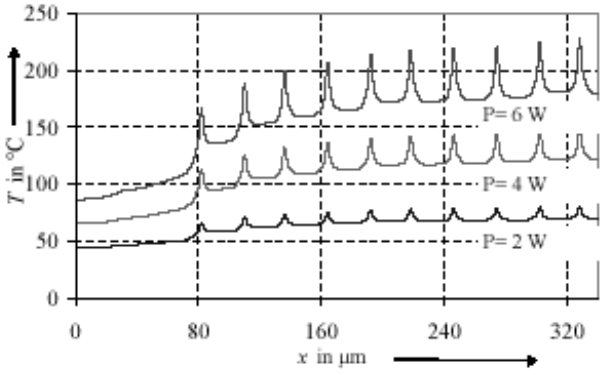

Figure 13: Temperatures along line scan A for different power levels (chip: 75 µm, die attach: 20µm, 30 W/mK).

Table 2: Relative deviation between simulated and measured values at different power levels.

	$P = 1.91$ W	$P = 4.7$ W
$t = 1.25$ ms	<-1%	- 2%
$t = 2.5$ ms	< -1%	-5%
$t = 5$ ms	-1%	-9%

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