Research on Power Electronic Integrated Module for SMPs

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Abstract

A novel structure for a power module used in switching mode power supplies (SMPs) is presented in this paper. The power module employs the three-dimensional terrace structure resulting in lowered parasitic parameters and a higher power density. Based on this structure, the characteristics of the power module, such as parasitic parameters and thermal management performance are evaluated through simulation analysis and experimental research. The measured results for a 1kw prototype demonstrate that the power module based on an aluminum substrate has higher power density, smaller volume and better thermal performance when compared to a module using a conventional structure.

Keywords

Integrated power electronic technology, parasitic parameter, switching mode power supplies (SMPS)

1. INTRODUCTION

The development of power electronic technology has changed our concept of the way we utilize electric power. Today more than 40 percent of electric power is processed through power electronic equipment. By the year 2010, the account probably will be up to 80 percent.

To this date, many power electronic products suffer from long design cycles since such equipment mainly consists of non-standard components. Thus, the manufacturing processes are labor-intensive, resulting in high cost and low reliability of the products.

Starting in the mid-1980's, diverse ways of power electronic integration including PIC and IPM have been developed. However, the scale of the integration has been low. From the mid-1990's, the concepts of PEBB (Power Electronic Building Block) and IPEMs (Integrated Power electronic modules) were proposed [1, 2, 6]. However, for middle and high power application, many technical issues were encountered, such as the electromagnetic compatibility, thermal management and materials. Much literature is available on these problems [3, 4, 5], and some new module structures are presented. However, no effective structure could be found to meet all these requirements.

In this paper, the new three-dimensional terrace structure power module is presented. The thermal resistance and thermal capacitance of the module are obtained by ANSYS software. By analyzing the oscillating waveform at the time the power switches turn off, the parasitic inductance can be calculated.

2. NEW STRUCTURE FOR POWER MODULE

A complete power electronics system should consist of active power components, driver and protection circuit, communication ports, control circuit and passive components. All individual components should be integrated into one standard module that should have commonality and can be replaced expediently with another standard module.

In the middle and high power range, however, some difficulties and problems are faced including thermal management, electromagnetic interference and electrical isolation.

Based on the combinination-integration methodology presented in this paper, the power electronic system is divided into appropriate sub-modules as shown in figure 1. Then, some key problems of the various sub-modules are individually solved. Finally, a complete power electronic equipment is fabricated by using both appropriate interconnection methods and final packaging. By adopting combination-integration methodology, the integration difficulty is reduced and the application flexibility of such power modules is improved. In the following sections, the thermal performance and parasitic inductance measurements of the active power integrated module based on an aluminum substrate are carried out.

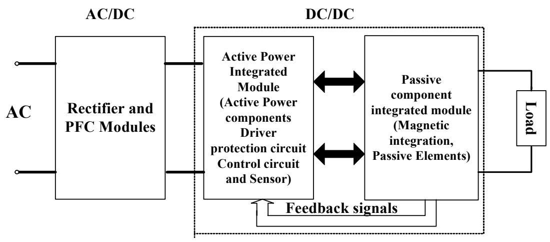


Figure 1. The configuration of SMPS based on combinination-integration

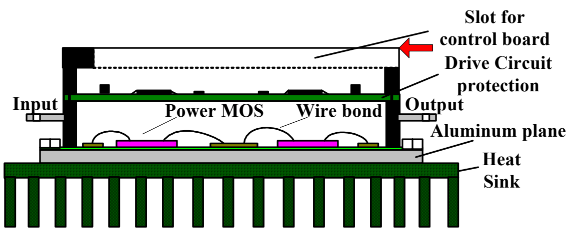


Figure 2. The inner structure of a power module using an aluminum substrate

The inner structure of an active power integration module using an aluminum substrate is shown in figure 2. The under layer of the module is the aluminum substrate on which four power dies (IRFP460LC) and some sensing circuits are soldered. The full bridge circuit topology is employed in the module. The middle layer includes the driving and protection circuits. It is connected to the substrate using contact pins embedded in the shell. The top layer is the slot for a control and communication adaptor-card circuit board.

3. CHARACTERISTICS ANALYSIS

Analyzing the characteristics of a combination-integrated module is more critical than that for a conventional structure power electronic equipment, because of its smaller volume and compact structure. The characteristics of the integrated module covered here are the thermal performance determined by the thermal resistance and capacitance, and parasitic parameters including parasitic inductance and coupling capacitance.

3.1. Thermal Performance Analysis

The thermal model in ANSYS is shown in figure 3. The cross-section of the aluminum substrate is given in figure 4. Molybdenum is used as the soldering transition layer. The main properties of the various materials used in performing the thermal analysis simulation are given in table 1.

The dimensions of the power MOS die are 9.15mm × 6.53 mm. The 100W power dissipation is uniformly applied to each power die and a heat sink at a constant temperature of 298K (25^{o}C) is applied to the backside of the aluminum substrate. The contact resistance between various materials is not taken accounted for in the analysis.

The temperature distribution of the top aluminum substrate is shown in figure 5. Figure 5(a) shows the result when the power is applied to all four dies, and figure 5(b) shows the result when the power is applied to only one die. From the simulation it can be seen that the highest die temperature in both cases is almost the same. This indicates that the dies do not influence each other temperature-wise.

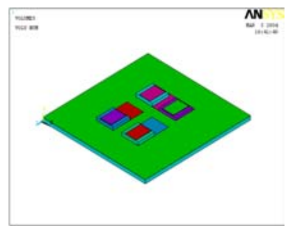


Figure 3. ANSYS model

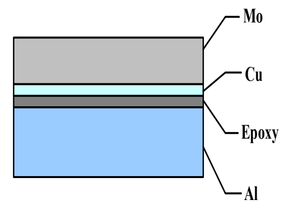
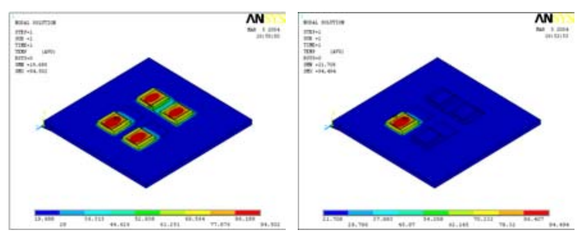


Figure 4. The cross-section of Aluminum substrate

TABLE 1. THE PROPERTY OF VARIOUS MATERIALS

Material	Thermal Conductivity W/(Km)	Thickness mm	Density g/cm^3	Specific Heat J/g*K	CTE PPm/K
Cu	400	0.08	8.96	0.38	16.50
Epoxy	2.2	0.1	2.50	0.9	40.00
Al	237	2	2.70	0.91	23.03
Mo	138	1.5	10.22	0.25	5.430



(a) (b)

(a) Power dissipation applied to four dies
(b) Power dissipation applied to one die

Figure 5. The temperature distribution of aluminum substrate

The junction-to-case thermal resistance of power module can be calculated by [7]:

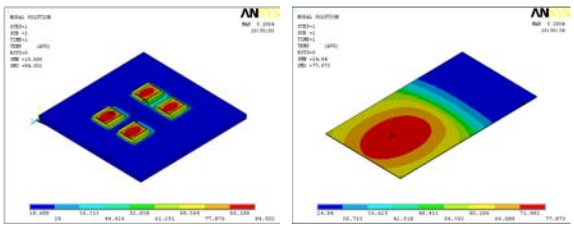
$$R_{th1} = \frac{\Delta T}{P} = \frac{94.502 - 25}{400} = 0.174(\mathrm{K/W})$$

The junction-to-case thermal resistance for per power is given by

$$R_{th2} = \frac{\Delta T}{P} = \frac{94.494 - 25}{100} = 0.695(\mathrm{K/W})$$

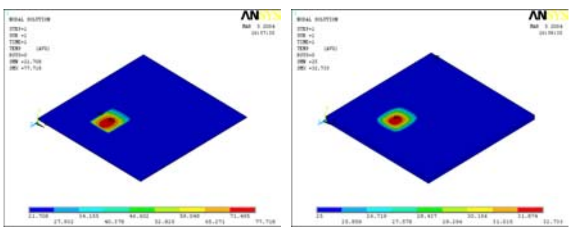
According to the manufacturer's catalog, the junction-to-case thermal resistance of a discrete IRFP460LC is 0.45K/W. In a practical application, for the discrete MOS, an isolation layer should be added to provide the electrical isolation which increases the total junction-to-heatsink thermal resistance.

In the case of the aluminum substrate power module, the thermal resistance of the isolation layer is part of the overall junction-to-case thermal resistance. In order to find the key factor that influences the total thermal resistance, the thermal resistance of each layer is calculated through the simulations as follows.



(a) (b)

(a) Temperature distribution of the top of Mo layer
(b) Temperature distribution of the bottom of Mo layer



(c) (d)

(c) Temperature distribution of the bottom of Mo layer
(d) Temperature distribution of the bottom of epoxy layer

Figure 6. The temperature distribution of each layer

The thermal resistance of molybdenum layer is

$$R_1 = \frac{94.502 - 77.873}{100} = 0.1663(\mathrm{K/W})$$

The thermal resistance of copper layer is

$$R_2 = \frac{77.873 - 77.718}{100} = 0.0016(\mathrm{K/W})$$

The thermal resistance of epoxy layer is

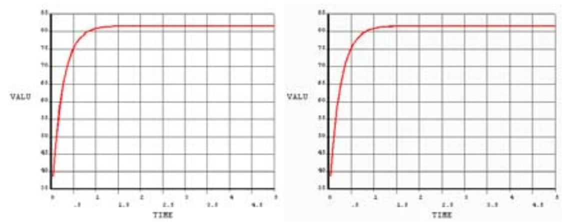
$$R_3 = \frac{77.718 - 32.733}{100} = 0.4498(\mathrm{K/W})$$

The thermal resistance of aluminum layer is

$$R_4 = \frac{32.733 - 25.000}{100} = 0.0773(\mathrm{K/W})$$

Obviously, the thermal resistance of the epoxy layer is dominant and comprises almost 65 percent of the total thermal resistance.

The evaluation of transient thermal performance is important especially for intermittent operation modes. The transient thermal response curve is showed in figure 7. The step power load of each power die is 81.73W and the other boundary conditions are the same as above. The heat exchange with the environment is not considered in the simulation.



(a) For single die (b) For four dies

Figure 7. The temperature transient response curves

The transient performance can be modeled by a thermal resistance and thermal capacitance network as shown in figure 8.

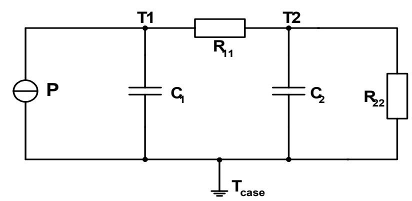


Figure 8. The thermal resistance and thermal capacitance equivalent network

The equation of the curve with reference to figure 8 can be assumed to be as follows:

$$\Delta T(t) = 56.80 \cdot (1 - x\mathrm{e}^{-a \cdot t} - y \cdot \mathrm{e}^{-b \cdot t})$$

Where, x, y, b and a are fitting constants that can be derived from the curve-fitting data.

$$x = 0.78, y = 0.22, a = 5.472, b = 2.315$$

Furthermore, R_{11}, R_{22}, C_1 and C_2 can be obtained through identical transformations.

$$R_{11} = 0.647(\mathrm{K/W}), R_{22} = 0.048(\mathrm{K/W})$$

$$C_1 = 0.301(\mathrm{W \cdot s/K}), C_2 = 8.360(\mathrm{W \cdot s/K})$$

3.2. Parasitic Parameters Analysis

One advantage of an integrated power module is the reduced parasitic inductance because of its more compact structure. But the parasitic inductance needs to be considered while the power switch operates at high frequency. For the module, the parasitic inductance be can analyzed and calculated from the oscillation voltage waveform of power switch.

The main power stage topology is showed in figure 9. The lumped parasitic parameters are high lighted in this figure.

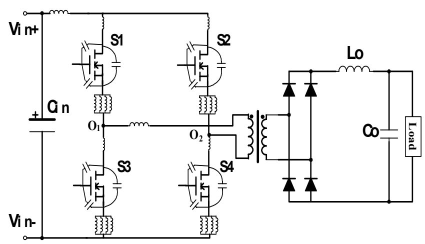


Figure 9. The main circuit topology with parasitic parameters

The ideal operation waveform of a full bride topology is shown in figure 10. The switches operate in basic hard-switching mode.

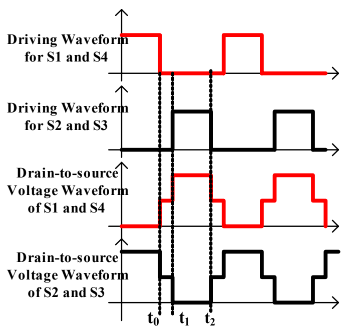
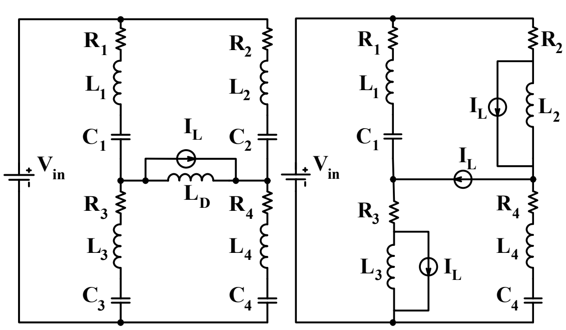


Figure 10. The ideal operation waveform

The approximate equivalent circuits at different time are given in figure 11.



(a) Equivalent circuit at t_0 **(b) Equivalent circuit at t_1**

Figure 11. The Equivalent circuit at different time

When S1 and S4 are turned off (t_0), the equivalent circuit is shown in Figure 11 (a). The current freewheels through the leakage inductor of transformer. The initial value of the leakage inductor current is the reflected current of the filter inductor at t_0. The characteristic parameters of the equivalent circuit include leakage inductance of transformer, loop line resistance, parasitic inductance and junction capacitance of power MOSFETs. Because the value of leakage inductance is much greater than that of parasitic inductor, the oscillation period is mainly determined by the leakage inductance, MOSFETs junction capacitance and coupling capacitance.

When S2 and S3 are turned on (t_1), the equivalent circuit is shown in figure 11 (b). The characteristic parameters of the equivalent circuit include line resistance, parasitic inductance and junction capacitors of power MOSFETs. In this case, the effect of parasitic inductance is significant. The oscillation period is determined almost by parasitic inductance, MOSFETs junction capacitance and coupling capacitance. For the aluminum substrate power module, increased coupling capacitance is a significant disadvantage that must be considered.

For the typical second-order oscillating circuit where R is much less than $2\sqrt{\frac{L}{C}}$ as in figure 12, the oscillation period can be expressed by

$$T = 2\pi\sqrt{LC}$$

Where, L is the parasitic inductance and C is the sum of junction capacitance and coupling capacitance. The above approximate condition can be also be applied to the practical integrated power circuit.

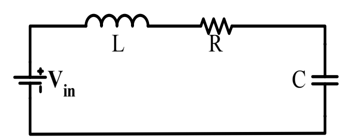
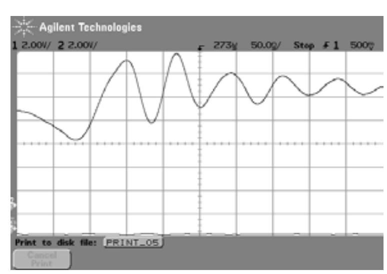


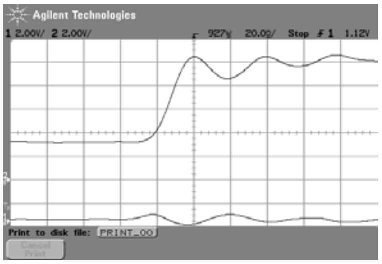
Figure 12. The typical second-order oscillating circuit

In order to calculate the parasitic inductance of a power module from the waveform, the experimental 110V/90V, 500W prototype based on active power integrated module is implemented. The power MOS die IRFP460LC is employed in the module. In addition, the other 110V/90V, 500W prototype based on a discrete device printed circuit board structure where the MOSFET IRFP460 is used. The parasitic inductance for the two different implemented structures is calculated and compared through the waveforms shown in figure 13.



X-axis: 50ns/div Y-axis: 20V/div

Figure 13(a). For discrete device printed circuit board structure



X-axis: 20ns/div Y-axis: 20V/div

Figure 13(b). For active power integrated module

Figure 13. The drain-to-source voltage oscillation waveforms when S2 and S3 are turned on

The junction capacitance of two different types is given in Table 2 for calculating the parasitic inductance.

Table 2. Junction capacitance of power MOS

	C_{iss}(pF)	C_{oss}(pF)	C_{rss}(pF)
IRFP460LC	3600	440	39
IRFP460	4200	870	350

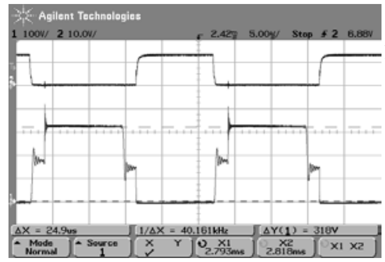
The oscillation period is 38ns for the active power integrated module and it is 70ns for the discrete device printed circuit board structure. Substituting the time period and junction capacitance into $T = 2\pi\sqrt{LC}$, the parasitic inductances, $L_{discrete}$ for the discrete device structure and $L_{integrated}$ for the integrated power module, are calculated to be as follows:

$$L_{discrete} = 142.8\text{nH} \quad L_{integrated} = 83.0\text{nH}$$

where, the parasitic inductance is the sum of L1 and L3 as shown in figure 11 for both cases. Therefore, the parasitic inductance is less for the active power integrated module.

4. EXPERIMENTAL RESULTS

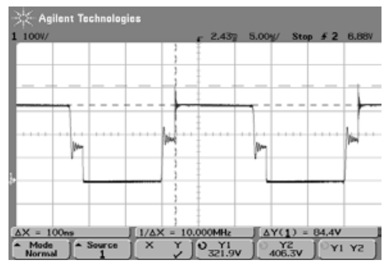
The performance of the active power integrated module is verified using an experimental 220V (AC)/220V, 1kW prototype based on the power integrated module configuration and using the following major components: power die—IRFP460LC, diode—DSEI 30-10A, output filter inductor—1mH, switching frequency—40 kHz, drive IC—IR2110, controller—SG1525, load—40Ω. The dimensions of the aluminum substrate are 65 mm × 63 mm. The measured experimental waveforms are shown in figure 14.



1 X-axis: 5μs/div
Y-axis: 100V/div

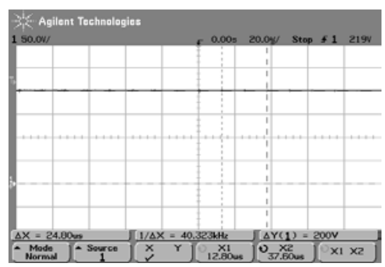
2 X-axis: 5μs/div
Y-axis: 10V/div

(a) Driving waveform and corresponding drain-to-source voltage



X-axis: 5μs/div
Y-axis: 100V/div

(b) Drain-to-source voltage overshoot measurement



X-axis: 5μs/div
Y-axis: 50V/div

(c) Output voltage waveform

Figure 14. Measured experimental waveforms

From the experimental waveform in figure14(a), the power circuit on an aluminum substrate has little influence on the upper driver and control board. The drain-to-source voltage overshot is 84.4V.

The picture of an actual power module is shown in figure 15. The top layer is the control board. The middle layer is the driver and protection layer. And, the bottom is the aluminum substrate on which the power dies and some sensors are soldered.

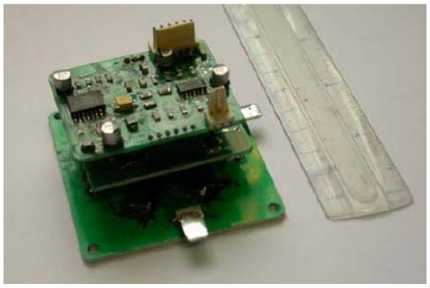


Figure 15. The picture of actual power module

5. CONCLUSIONS

In this paper, the three-dimensional terrace structure power module is implemented using an aluminum substrate. The thermal performance is simulated and evaluated by ANSYS software. The parasitic inductance is calculated from the drain-to-source oscillation waveform.

The performance of the active power integrated module is verified using an experimental 220V(AC)/220V, 1kW prototype based on the power integrated module configuration. Compared with the discrete device printed circuit board structure equipment, the equipment based on an active power integrated module has many advantages, such as a more compact structure, reduced parasitic inductance, better thermal performance and is easier to implement.

ACKNOWLEDGMENT

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BIOGRAPHIES

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Wang Zhaoan was born in Xi'an, China. He received the B.S. and M.S. degrees from Xi'an Jiaotong University, Xi'an, in 1970 and 1982, respectively, and the Ph.D. degree from Osaka University, Osaka, Japan, in 1989.From 1970 to 1979, he was an Engineer at Xi'an Rectifier Factory. He was an Associate Professor at Xi'an Jiaotong University, where he is currently a professor. He is engaged in research on power conversion system, harmonics suppression and reactive power compensation, and active power filters.