# Redistribution Layers (RDLs) for 2.5D/3D IC Integration

J. Lau,<sup>1,\*</sup> P. Tzeng,<sup>1</sup> C. Lee,<sup>1</sup> C. Zhan,<sup>1</sup> M. Li,<sup>2</sup> J. Cline,<sup>2</sup> K. Saito,<sup>2</sup> Y. Hsin,<sup>1</sup> P. Chang,<sup>1</sup> Y. Chang,<sup>1</sup> J. Chen,<sup>1</sup> S. Chen,<sup>1</sup> C. Wu,<sup>1</sup> H. Chang,<sup>1</sup> C. Chien,<sup>1</sup> C. Lin,<sup>1</sup> T. Ku,<sup>1</sup> R. Lo,<sup>1</sup> and M. Kao<sup>1</sup>

*Abstract*—Redistribution layer (RDL) is an integral part of 3D IC integration, especially for 2.5D IC integration with a passive interposer. The RDL allows for circuitry fan-outs of and allows for lateral communication between the chips attached to the interposer. There are at least two ways to fabricate the RDL, namely (1) polymers to make the passivation and Cu-plating to make the metal layer, and (2) semiconductor back-end-of-line Cu damascene. In this study, the materials and processes of these methods are presented. Emphasis is placed on the Cu damascene method.

*Keywords*—3D IC integration, through-silicon via (TSV), redistribution layer (RDL), polymer, Cu damascene

#### INTRODUCTION

**O** ne of the potential applications of 3D IC integration is wide I/O interfaces [1], which consists of a piece of device-less silicon with through-silicon vias (TSVs) and highperformance, high-density IC chips without TSV. This piece of device-less silicon (also called a passive interposer) is used to support the chips and has RDLs (mainly) for lateral communication between the chips (Fig. 1).

As mentioned in [2-5], one of the key reasons to have the intermediate substrate (passive interposer) is created by the ever increasing IC density and pin-out, and shrinking IC pad-pitch and size, the conventional package substrate cannot support these IC requirements. A couple of examples are shown in Fig. 2 (Xilinx/TSMC) [6-8] and Fig. 3 (Altera/TSMC) [9, 10] (where CoWoS stands for chip on (interposer) wafer on (package) substrate). In these cases, it can be seen that even with 12 buildup layers (6-2-6) on the package substrate, it is still not enough to support the FPGA (field-programmable gate array) chips. In addition, a passive TSV interposer with four top RDLs (three Cu damascene layers and one aluminum layer) at a 0.4  $\mu$ m pitch is needed. The minimum thickness of the RDLs and passivation is <1  $\mu$ m. Also, it can be seen that even with the term of the reaction of the term.

posers are for very high-I/O, high-performance, and highdensity applications. The RDL is the focus of this study. There are at least

two ways to fabricate RDLs. The first method is by using polymers, such as polyimide (PI) PWDC 1000 (Dow Corning), benzocyclobutene (BCB) cyclotene 4024-40 (Dow Chemical), polybenzo-bisoxazole (PBO) HD-8930 (HD Micro Systems), and the fluorinated aromatic AL-X 2010 (Asahi Glass Corporation) to make the passivation layer and electroplating (such as Cu) to make the metal layers. This method has been used by the OSAT (outsourced semiconductor assembly and test) to fabricate RDLs (without using semiconductor equipment) for wafer-level (fan-in) chip scale package [11, 12], embedded wafer-level (fan-out) ball grid array package [13], and (fan-out) redistribution chip package [14]. The second method is the Cu damascene method, which is primarily modified from the conventional semiconductor back-end-of-line to make the Cu metal RDLs such as those shown in Figs. 2 and 3. In general, much thinner structures (both dielectric layers and Cu RDLs), finer pitches, smaller line-widths, and spacing can be obtained with the Cu damascene method, which will be the emphasis in this study. The polymer/Cu-plating method will be mentioned first. Also, the fabrication of TSV and Cu reveal will be presented.

## FABRICATION OF TSV

The fabrication process of TSVs is shown in Fig. 4. The process starts with an  $SiN_x/SiO_x$  insulation layer by either thermal oxidation or PECVD (plasma enhanced chemical vapor deposition) as shown in Fig. 4. After photoresist and TSV lithography, the TSV is etched into the Si substrate by Bosch-type DRIE (deep reactive ion etch) [15] to form a high aspect ratio (10.5) via structure. The etched TSV structure is then processed with an SiO<sub>x</sub> liner by SACVD (subatmosphere chemical vapor deposition), a Ta barrier layer, and a Cu seed layer by PVD (physical vapor deposition) [16]. Cu electroplating is used to fill the TSV structure. The final blind TSV has a top opening of approximately 10 µm in diameter and a depth of about 105 µm, which gives an aspect ratio of 10.5. In such a high aspect ratio via structure, a bottom-up plating mechanism is applied to ensure a seamless TSV with a reasonably low Cu thickness in the field. The SEM (scanning-electron microscopy) cross-sectional images are shown in Fig. 5. It can be seen that the diameter of the TSV is slightly decreased at the bottom, which is expected from the etching process. The Cu thickness at the field is  $<5 \mu m$ . The postplating anneal is at 400°C for 30 min.

Received on October 10, 2013; revision received on December 22, 2013; accepted on December 23, 2013

The original version of this paper was presented at IMAPS 46th International Symposium on Microelectronics (IMAPS 2013), September 30-October 3, 2013, Orlando, FL.

<sup>&</sup>lt;sup>1</sup>Electronics and Optoelectronics Research Laboratory, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan

<sup>&</sup>lt;sup>2</sup>Rambus Inc., 1050 Enterprise Way, Suite 700, Sunnyvale, California 94089 \*Corresponding author; email: johnlau@itri.org.tw



Fig. 1. TSV/RDL passive interposer on substrate.

To complete the TSV process, excess Cu in the field is removed by CMP (chemical-mechanical polishing) [17].

# FABRICATION OF RDL BY POLYMERS

Continuing with the wafer from Fig. 4, the fabrication process for the RDLs using polymers is shown in Fig. 6 and also listed as follows. UBM (under bump metallurgy) is included.

- Step 1. Spin the polymers such as PI or BCB on the wafer and cure for 1 h. This will form a 4-7-µm-thick layer.
- Step 2. Apply photoresist and mask, then use photolithography techniques (align and expose) to open vias on the PI or BCB.
- Step 3. Etch the PI or BCB.
- Step 4. Strip off the photoresist.
- Step 5. Sputter Ti and Cu over the entire wafer.
- Step 6. Apply a photoresist and mask, and then use photolithography techniques to open the redistributiontrace locations.



Fig. 3. Altera/TSMC's CoWoS.

- Step 7. Electroplate Cu in photoresist openings.
- Step 8. Strip off the photoresist.
- Step 9. Etch off the Ti/Cu and RDL1 is completed.
- Step 10. Repeat steps 1-9 for RDL2, and so forth.
- Step 11. Repeat step 1 (for UBM).
- Step 12. Apply photoresist and mask, and then use photolithography techniques (align and expose) to open vias on the PI or BCB for the desired bump pads and to cover the redistribution traces.
- Step 13. Etch the desired vias on the PI or BCB.
- Step 14. Strip off the photoresist.
- Step 15. Sputter Ti and Cu over the entire wafer.
- Step 16. Apply photoresist and mask, and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.
- Step 17. Electroplate the Cu core.
- Step 18. Strip off the photoresist.
- Step 19. Etch off the Ti/Cu.
- Step 20. Electroless Ni and immersion Au. UBM is completed.

A typical cross section of the RDLs with polymers (e.g., BCB) as passivation and Cu plating as metal layers is shown in Fig. 7 (IZMs, 2 RDLs with BCB1, and BCB2 [18]). It can be





Fig. 4. TSV fabrication process flow.



Fig. 5. SEM images of TSV cross sections.

seen that the thickness of the passivation layers, BCB1 and BCB2, is about 6-7  $\mu$ m, and the RDL is about 4  $\mu$ m. It should be noted that photolithography can be directly applied on PI or BCB for larger dimensions. In that case the first set of photoresist is not needed.

## RDL FABRICATED BY CU DAMASCENE

Another method of RDL fabrication is by a Cu damascene process. If starting with the wafer from Fig. 4, the fabrication process of RDLs with a Cu damascene technique is primarily based on the semiconductor back-end-of-line process. The details are shown in Fig. 8 and listed below.

- Step 1.  $SiO_2$  layer by PECVD.
- Step 2. Apply photoresist and mask, then use photolithography techniques (align and expose) to open vias on the  $SiO_2$ .
- Step 3. RIE (reactive ion etch) of SiO<sub>2</sub>.
- Step 4. Strip off the photoresist.
- Step 5. Sputter Ti and Cu and electroplate Cu over the entire wafer.
- Step 6. CMP the Cu and Ti/Cu. V01 (the via connecting the TSV to RDL1) is completed.
- Step 7. Repeat step 1.
- Step 8. Apply photoresist and mask, and then use photolithography techniques to open the redistribution trace locations.
- Step 9. Repeat step 3.
- Step 10. Repeat step 4.



Fig. 6. RDL fabrication process with polymers as passivation and Cu plating as metal layers.

- Step 11. Repeat step 5.
- Step 12. CMP the Cu and Ti/Cu. RDL1 is completed.
- Step 13. Repeat step 1 through step 6 to complete V12 (the via connecting the RDL1 to RDL2).
- Step 14. Repeat step 7 through step 12 to complete RDL2 and any additional layers.
- Step 15. (For UBM) Repeat step 1.
- Step 16. Apply photoresist and mask, and then use photolithography techniques (align and expose) to open vias on the  $SiO_2$  for the desired bump pads and cover the redistribution traces.
- Step 17. Etch the desired vias on the  $SiO_2$ .
- Step 18. Strip off the photoresist.
- Step 19. Sputter Ti and Cu over the entire wafer.
- Step 20. Apply photoresist and mask, and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.



Fig. 7. IZM's RDLs with BCB polymer.

- Step 21. Electroplate Cu core.
- Step 22. Strip off the photoresist.
- Step 23. Etch off the Ti/Cu.
- Step 24. Electroless Ni and immersion Au. UBM is completed.

It should be noted that the RDLs can also be fabricated by the dual Cu damascene method as shown in Fig. 9. SEM images of the RDL cross sections fabricated by a Cu damascene technique are shown in Figs. 10 and 11. The minimum RDL line width is 3  $\mu$ m. The thickness of RDL1 and RDL2 is 2.6  $\mu$ m and of RDL3 is 1.3  $\mu$ m. The passivation thickness between RDLs is 1  $\mu$ m.

#### A NOTE ON CONTACT ALIGNER FOR CU DAMASCENE METHOD

The RDLs in this study are fabricated by the Cu damascene method. Lithography using a contact aligner provides a low-cost process as compared with a stepper/scanner under the same resolution requirements. Since the minimum line width is 3  $\mu$ m in this case, the mask had to be placed very close to the (photoresist) surface of the 300 mm wafer. In a few cases, particles on the contact aligner mask punched holes on the photoresist. In this case, shorts may happen such as that shown in Fig. 12, which happened while fabricating the V12 (the via connecting RDL1 and RDL2). This can be prevented by cleaning the mask between exposures. Alternately, if cost is not an issue, using a stepper/scanner is another solution.

#### BACKSIDE PROCESSING AND ASSEMBLY

Some of the backside processes of this wafer (shown in Fig. 8) such as the RDLs in the backside have been reported





Fig. 8. Process flow of RDLs fabricated by Cu damascene method.





Fig. 9. Process flow for fabricating RDLs by dual Cu damascene.



Fig. 10. SEM images of cross sections of RDLs fabricated by the Cu damascene method.

in [19]. The process flow of backside and assembly is shown in Fig. 13. It can be seen that after the fabrication of TSV, RDLs, passivation, and UBM, the topside of the interposer wafer is temporary bonded to a carrier by adhesive. The next step is backgrinding the interposer wafer, Si etching, low temperature passivation, and Cu revealing. Next, backside RDL (optional), UBM, and C4 (controlled collapse chip connection) wafer bumping are carried out. After that, the next step is to temporary bond another carrier wafer to the backside (with solder bumps) and de-bond the first carrier wafer. This step is followed by chip-on-wafer bonding and underfilling. After the whole interposer wafer is completed, the next step is to de-bond the second carrier wafer and transfer the thin interposer wafer with attached chips to a dicing tape for singulation.



Fig. 11. SEM images of cross sections of RDLs fabricated by the Cu damascene method.

## CONCLUSIONS

The materials and processes for the fabrication of RDLs with two different methods, namely (1) polymer (e.g., BCB) to make the passivation and Cu plating to make the metal layers, and (2) semiconductor back-end-of-line Cu damascene, have been presented. The fabrications of TSVs, UBMs, and Cu reveal of the interposer have also been described. Some important results and recommendations are summarized as follows.

- 1. The RDLs fabricated by the polymer method are usually thicker. The thickness of the passivation is 6-7  $\mu$ m and the Cu metal layer is 3-4  $\mu$ m.
- 2. The RDLs fabricated by the Cu damascene method are thinner. The thickness of the passivation and the Cu metal layer is  $\sim 1 \ \mu m$  if a contact aligner is used and in the submicron range if a stepper/scanner is used.
- 3. Lithography using a stepper/scanner can go down to submicron line width and line spacing. However, for a few microns' applications, a contact aligner will provide a lowcost process under the same resolution requirements. In order to prevent shorts (not to allow holes in the photoresist and thus the passivation during the fabrication of the vias) between the RDLs, all the particles must be cleaned off from the mask.

#### **ACKNOWLEDGMENTS**

The ITRI authors would like to thank the financial support of Rambus, USA and MOEA, Taiwan. The strong support of the 3D IC Integration program by Dr. C. T. Liu, VP and



Fig. 13. Conventional process flow for 2.5D/3D IC integration (chip on interposer wafer on package substrate).



Fig. 12. SEM/FIB showing the short between RDL1 and RDL2. The thickness of the passivation layer between RDL1 and RDL2 is  ${<}1\,\mu m.$ 

(For thin-wafer handling without temporary bonding and de-bonding, please see [20].) The individual TSV/RDL interposer with chips is attached to the package substrate by natural reflow and then underfilled.

Fig. 14 shows more detail on Cu revealing. Right after the temporary bonding of the support carrier, backgrinding the wafer to a few microns to the TSV, Si dry etching (by RIE) to a few microns below the TSV, and low-temperature passiving the SiN/SiO<sub>2</sub> are performed. Then, CMP for SiN/SiO<sub>2</sub> buffing and barrier and Cu seed layers polishing are carried out. Cu revealing is completed and shown in Fig. 15.



Fig. 14. Backside Cu reveal and UBM/solder plating process flow.



Fig. 15. TSV Cu revealing. (Left) Before dry etch of Si. (Right) After Si dry etching, low-temperature SiN/SiO<sub>2</sub>, and removal (CMP) of the isolation, barrier, and seed layer.

Director of Electronics & Optoelectronics Research Lab is greatly appreciated.

#### References

- [1] J.H. Lau, *Through-Silicon Via for 3D Integration*, McGraw-Hill, New York, 2013.
- [2] C. Selvanayagam, J.H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," Proceedings of IEEE/ECTC, pp. 1073-1081, May 2008.
- [3] C. Selvanayagam, J.H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," *IEEE Transactions* on Advanced Packaging, Vol. 32, No. 4, pp. 720-728, 2009.
- [4] X. Zhang, T. Chai, J.H. Lau, C. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, G. Tang, Y. Ong, S. Vempati, E. Wai, H. Li, B. Liao, N. Ranganathan, V. Kripesh, J. Sun, J. Doricko, and C. Vath, "Develop-

ment of through silicon via (TSV) interposer technology for large die  $(21 \times 21 \text{ mm})$  fine-pitch Cu/low-*k* FCBGA package," Proceedings of IEEE/ECTC, pp. 305-312, May 2009.

- [5] Chai, T., X. Zhang, J.H. Lau, C. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, G. Tang, Y. Ong, S. Vempati, E. Wai, H. Li, B. Liao, N. Ranganathan, V. Kripesh, J. Sun, J. Doricko, C. Vath, and Y. Tsutsumi, "Development of Large Die Fine-Pitch Cu/low-k FCBGA Package with through Silicon via (TSV) Interposer," IEEE Transactions on CPMT, pp. 660-672, 2011.
- [6] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced reliability study of TSV interposers and interconnects for the 28 nm technology FPGA," Proceedings of IEEE/ECTC, pp. 285-290, June 2011.
- [7] R. Chaware, K. Nagarajan, and S. Ramalingam, "Assembly and reliability challenges in 3D integration of 28 nm FPGA die on a large high density 65 nm passive interposer," Proceedings of IEEE/ECTC, pp. 279-283, May 2012.
- [8] B. Banijamali, S. Ramalingam, H. Liu, and M. Kim, "Outstanding and innovative reliability study of 3D TSV interposer and fine pitch solder micro-bumps," Proceedings of IEEE/ECTC, pp. 309-314, May 2012.

- [9] J. Xie, H. Shi, Y. Li, Z. Li, A. Rahman, K. Chandrasekar, D. Ratakonda, M. Deo, K. Chanda, V. Hool, M. Lee, N. Vodrahalli, D. Ibbotson, and T. Verma, "Enabling the 2.5D integration," Proceedings of IMAPS International Symposium on Microelectronics, pp. 254-267, September 2012.
- [10] Z. Li, H. Shi, J. Xie, and A. Rahman, "Development of an optimized power delivery system for 3D IC integration with TSV silicon interposer," Proceedings of IEEE/ECTC, pp. 678-682, May 2012.
- [11] J.H. Lau, C. Ouyang, and R. Lee, "A novel and reliable wafer-level chip scale package (WLCSP)," Proceedings of Chip Scale International Conference, pp. H1-H9, September 1999.
- [12] J. H. Lau, R. Lee, C. Chang, and C. Chen, "Solder joint reliability of wafer level chip scale packages (WLCSP): A time-temperature-dependent creep analysis," ASME Paper No. 99-IMECE/EEP-5, November 1999.
- [13] M. Brunnbauer, E. Furgut, G. Beer, T. Meyer, H. Hedler, J. Belonio, E. Nomura, K. Kiuchi, and K. Kobayashi, "An embedded device technology based on a molded reconfigured wafer," Proceedings of IEEE/ ECTC, pp. 547-551, May 2006.
- [14] B. Keser, C. Amrine, T. Duong, O. Fay, S. Hayes, G. Leal, W. Lytle, D. Mitchell, and R. Wenzel, "The redistributed chip package: A breakthrough for advanced packaging," Proceedings of IEEE/ECTC, pp. 286-291, May 2007.
- [15] Y.C. Hsin, C. Chen, J.H. Lau, P. Tzeng, S. Shen, Y. Hsu, S. Chen, C. Wn, J. Chen, T. Ku, and M. Kao, "Effects of etch rate on scallop of through-

silicon vias (TSVs) in 200 mm and 300 mm wafers," Proceedings of IEEE/ECTC, pp. 1130-1135, May 2011.

- [16] C. Wu, S. Chen, P. Tzeng, J.H. Lau, Y. Hsu, J. Chen, Y. Hsin, C. Chen, S. Shen, C. Lin, T. Ku, and M. Kao, "Oxide liner, barrier and seed layers, and Cu-plating of blind through silicon vias (TSVs) on 300 mm wafers for 3D IC integration," *IMAPS Transactions, Journal of Microelectronic Packaging*, Vol. 9, No. 1, pp. 31-36, 2012.
- [17] J.C. Chen, J.H. Lau, P.J. Tzeng, S. Chen, C. Wu, C. Chen, H. Yu, Y. Hsu, S. Shen, S. Liao, C. Ho, C. Lin, T.K. Ku, and M.J. Kao, "Effects of slurry in Cu chemical mechanical polishing (CMP) of TSVs for 3-D IC integration," *IEEE Transactions on CPMT*, Vol. 2, No. 6, pp. 956-963, 2012.
- [18] K. Zoschke, J. Wolf, C. Lopper, I. Kuna, N. Jürgensen, V. Glaw, K. Samulewicz, J. Röder, M. Wilke, O. Wünsch, M. Klein, M. Suchodoletz, H. Oppermann, T. Braun, R. Wieland, and O. Ehrmann, "TSV based silicon interposer technology for wafer level fabrication of 3D SiP modules," Proceedings of IEEE/ECTC, pp. 836-842, May 2011.
- [19] P.J. Tzeng, J.H. Lau, C. Zhan, Y. Hsin, P. Chang, Y. Chang, J. Chen, S. Chen, C. Wu, C. Lee, H. Chang, C. Chien, C. Lin, T. Ku, M. Kao, M. Li, J. Cline, K. Saito, and M. Ji, "Process integration of 3D Si interposer with double-sided active chip attachments," Proceedings of IEEE/ECTC, pp. 86-93, 2013.
- [20] J. Lau, H. Chien, S. Wu, Y. Chao, W. Lo, and M. Kao, "Thin-wafer handling with a heat-spreader wafer," Proceedings of IMAPS International Symposium on Microelectronics, September 2013.