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Advanced Thermal Management Solutions on PCBs for High Power Applications

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Abstract—**With increasing power loss of electrical components, thermal performance of an assembled device becomes one of the most important quality factors in electronic packaging. Due to rapid advances in semiconductor technology, particularly in the field of high-power components, the temperature distribution inside of a component is a critical parameter of long-term reliability and must be carefully considered during the design phase.**

Two main drivers in the electronics industry are miniaturization and reliability. Whereas there is a continuous improvement concerning miniaturization of conductor tracks (i.e., lines and spaces have been reduced continuously over the past years), miniaturization of the circuit carrier itself, however, has mostly been limited to decreased layer counts and base material thickness. This can lead to significant component temperature increase and thence to accelerated system degradation.

Enhancement of the system reliability is directly connected to an efficient thermal management on the PCB level. There are several approaches that can be used to address this issue: optimization of the board design, use of base materials with advanced thermal performance, and use of innovative buildup concepts.

The paper provides a short overview about standard thermal solutions such as thick copper, thermal vias, plugged vias, or metal core based PCBs. Furthermore, attention will be focused on the development of copper filled thermal vias in thin board construction. In another approach, advanced thermal management solutions are presented at the board level, exploring different buildup concepts (e.g., cavities). Advantages of cavity solutions in the board are shown that not only decrease the thermal path leading from the high power component through the board to the heat sink, but also have an impact concerning the mechanical miniaturization of the entire system (reduction of z axis). Such buildups serve as a favorable packaging solution with promising thermal performance.

Moreover, using thermal simulations different setups are compared and a deeper insight into the thermally relevant geometry and material parameters is provided, allowing production efforts to be reduced and to offering optimized designs and board buildups.

Keywords—**PCB, thermal management, power electronics, low thermal resistance, cavities**

Introduction

Modern power electronics use power components such as MOSFETs, IGBTs, GTOs, high brightness LEDs, and many more. Due to the enormously rapid advances in semiconductor technology, particularly in the regimen of high-power applications, the trend is toward smaller components with even higher switching speeds and higher current densities. In general, a strong miniaturization trend for whole modules can be seen.

With these trends and with increasing power loss densities, the thermal performance of an assembly becomes one of the most important quality factors in electronic packaging. New materials, and also new and innovative approaches in the area of the PCB-substrates, will be necessary to meet the required reliability levels.

Interest in power electronics has grown dramatically in the last few years with increasing need for electric power management and control (Smart Grid), renewable energy generation and control (wind power, photovoltaic, fuel cell, etc.), electric transportation, and the desire to improve operating efficiency of heavy systems (trains, industrial motors, electric vehicles, etc.).

Power electronic converters are found wherever there is a need to modify the voltage, current, or frequency. These range in power from few milliwatts in mobile phones to hundreds of megawatts in HVDC (high-voltage, direct current) transmission systems (Fig. 1). Usually we think of electronics in the framework of information, where speed is the primary interest. In the context of power electronics, improved efficiency and lower power losses are of prime importance.

Thermal Resistance

A. Definition of the Thermal Path and Thermal Resistance

Under steady-state conditions, the most frequently used measures for thermal performance of an electronic module are either the junction temperature T_J of the semiconductor device with the significant power loss or—even more common—the thermal resistance R_{th}. The latter is defined by the temperature difference along a thermal path, such as, $T_J - T_C$, where T_C denotes the temperature of the interface in the case of the

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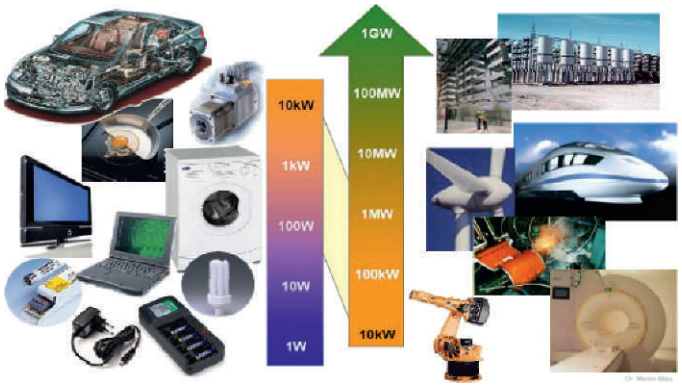


Fig. 1. Range of power electronic applications (Source: iNEMI Technology Roadmaps, Jan 2013).

module and a cooler, and the power loss P_{loss}, giving the temperature difference as

$$R_{\text{th}} = \frac{T_{\text{J}} - T_{\text{C}}}{P_{\text{loss}}} \tag{1}$$

where eq. (1) is a useful practical approach to describe the thermal performance of a power assembly and where T_{J} and T_{C} are isotherms and the entire heat flow from T_{J} to T_{C} equals P_{loss}. It should be noted that these conditions are not always fulfilled. In small silicon transistors and diodes the rather minor temperature gradients within the junction can frequently be neglected. However, as can, for example, be seen by a more detailed thermal investigation of a GaAs high-power transistor, depending on the considered semiconductor device, there are tremendously high temperature differences within the junction itself [1]. Another frequent misinterpretation of eq. (1) arises if the case temperature is not uniform enough. In fact, one major concern of thermal management at the PCB level is to reach a uniform case temperature over an area as large as possible.

A further approach to describe the thermal resistance R_{th} is shown in eq. (2). It can be seen that the thermal resistance can be minimized by reducing the length l of the thermal path or by increasing the thermal conductivity λ of the material as well as by increasing the area of the contact pad A. As mentioned in the introduction, there is a miniaturization trend in power components, so there is no chance to increase the area. For this, only the first two possibilities can be used to improve the thermal management of the system. This means that the length of the thermal path through the PCB should be as short as possible, and the material between the component and the heat sink should have a thermal conductivity as high as possible.

$$R_{\text{th}} = \frac{l}{\lambda \cdot A} \tag{2}$$

B. Motivation for Thermal Management

The main reason for deficiencies of electrical systems (apart from dust, vibration, and humidity) is by far the impact of temperature. Therefore, an efficient thermal management concept on the PCB is crucial for the reliability of power electronic systems.

As an example we take high power LED applications, which are likely to dominate in the coming years in residential and commercial lighting, and in signaling and vehicle headlights, due to efficiency and extended lifetime. LEDs that range from 500 mW to as much as 10 W in a single package have become standard, and researchers expect even higher power in the future.

Thermal management is of critical importance for high power LEDs. More than 60% of the electrical power input is converted into heat and built up at the junctions of LED chips due to nonradiative recombination of electron-hole pairs and low light extraction.

If that heat is not removed, the LEDs run at high temperature, which not only lowers their efficiency, but also makes the LED more dangerous and less reliable, and shortens operating life [2, 3]. Thus, thermal management of high power LEDs is a crucial area of research and development.

In this paper, the results of simulations and measurements of different LED modules will be shown and should serve as representative thermal solutions for general high power applications.

Standard PCB Technology for Thermal Management

A. Overview and Short Description

An effective heat removal can be based either on a short heat conduction path to a heat sink perpendicular through the PCB (e.g., thermal vias) or by a conductor layer acting as a lateral heat spreader (extended thermal pads) or a combination of both.

There are many different and well-known buildups for these heat removal concepts on PCBs. Thick copper approaches on PCBs guarantee a very good lateral heat spreading effect due to the excellent thermal conductivity of the copper and are put to good use to reduce hot spots.

IMSs (insulated metallic substrates) are also state of the art and are widely used for thermal issues in electronic systems. An IMS consists of a metallic base material (mostly aluminum or copper) with a thickness of about 0.5 mm to 3.0 mm. On the metallic base material there is a thin dielectric layer (about 30-150 μm) with a high thermal conductivity (0.5-8.0 W/mK) in respect to standard FR4-material (ca. 0.3 W/mK). The copper design layer is on top of the dielectric layer.

IMSs show a very short heat conduction path through the thin dielectric layer, because the metallic base material already serves as a first heat sink. There are several different IMS variations available depending on the requested performance.

A further buildup concept using a short heat conduction path to the heat sink is conventional through-hole plated glass fiber reinforced PCB technology. A sufficient thermal performance in the lower power loss range up to several watts can frequently be achieved by reasonable numbers for via count, via diameter, and hole plating thickness [4]. Fig. 2a shows a scheme of a PCB with open through holes serving as open thermal vias. In Fig. 2b, an example of a footprint design is shown. It can be seen that the thermal vias are situated in the extended thermal pads beyond where the component will be placed. So, to avoid the well-known problem of solder soaking, it is not possible to place open thermal vias directly underneath a component. Due to this fact, the thermal path is elongated, because the heat first has to be spread laterally on

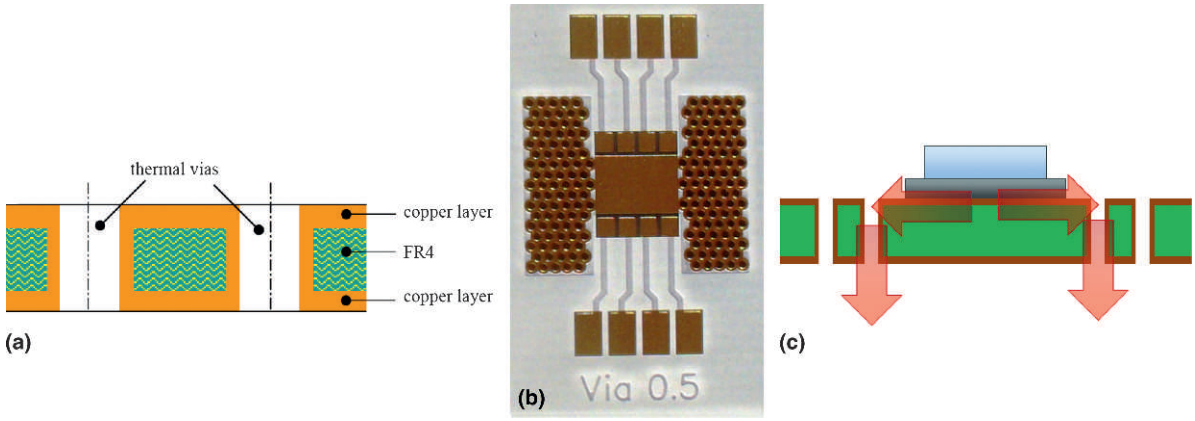


Fig. 2. PCB with open thermal vias: (a) schematic; (b) design; and (c) thermal path.

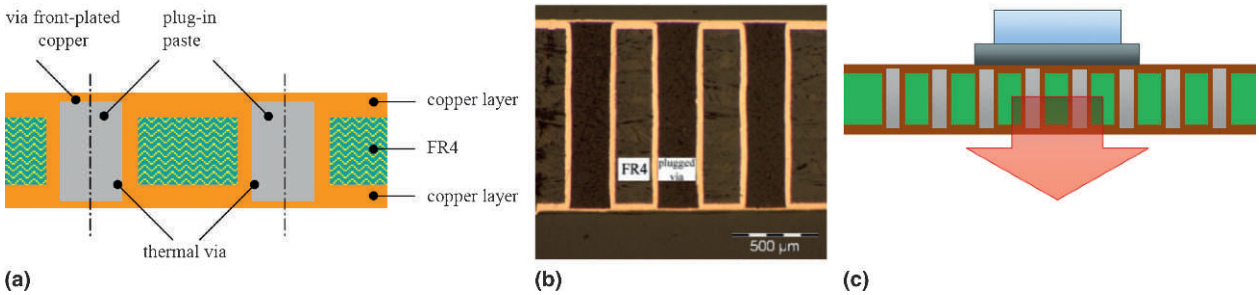


Fig. 3. PCB with plugged thermal vias: (a) schematic; (b) cross section; and (c) thermal path.

the surface before it can be guided perpendicularly through the PCB to the heat sink (Fig. 2c).

A schematic cross section as depicted in Fig. 3a demonstrates a special via plating technology featuring plugged vias with a homogeneous copper layer on the front faces. In contrast to the concept with open vias, this buildup allows vias to be directly beneath a component, which also reduces the thermal path. Fig. 3b shows a micrograph of a cross section of this type of PCB.

B. Experimental Setup

Test objects were selected with following specifications:

- DK2 (FR4, thickness = 1 mm, pads with plugged thermal vias)
- DK6 (FR4, thickness = 0.2 mm, open thermal vias with 0.3 mm diameter, laminated onto 1.5 mm thick Al substrate with a 90 µm thick prepreg)
- IMS1 (70 µm thick copper clad, 110 µm thick dielectric, thermal conductivity = 0.5 W/mK, Al substrate thickness = 1.5 mm)
- IMS3 (70 µm thick copper clad, 125 µm thick dielectric, thermal conductivity = 4 W/mK, Al substrate thickness = 1.5 mm)

All PCB samples were prepared with a size of 30 mm × 40 mm. The layout allowed the testing of two power LEDs (type: OSTAR SMT-H) at the same time (Fig. 4a), whereby the comparatively large via arrays should help to maximize heat spreading.

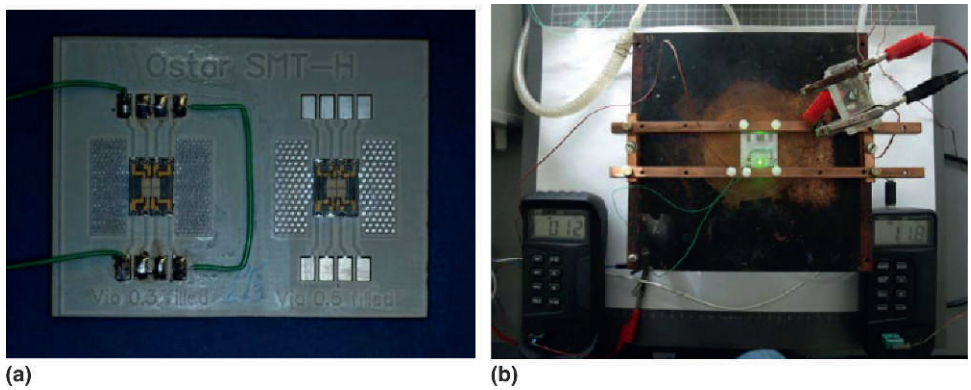


Fig. 4. Ostar SMT-H module mounted on water-cooled heat sink: (a) top view of test sample; (b) sample under test.

The most important priority of an experimental setup is to simulate boundary conditions as close as possible to the following extreme conditions:

1. The PCB itself acts as a heat sink by conducting the heat flux in the plane direction and dissipation mode, that is, by natural convection and radiation.
2. The PCB acts as a means to interconnect the power component with a cooler and to help spread the heat flux uniformly over the entire attachment surface of the cooler.

In this section we compare the thermal performance of FR4-based PCBs with thermal via arrays (two different modifications: with open vias and with plugged vias) and IMS in an experimental setup according to condition 2). For this purpose, a water-cooled copper block was used as a heat sink with constant temperature. The samples were attached to the copper block using an equally distributed thin layer of thermal grease with a thermal conductivity of 0.6 W/mK. The samples were pressed against the copper block with pointed plastic screws in order to keep the thermal resistance of this interface as stable as possible without heat removal from the top side (Fig. 4b).

Temperature distributions of the top side of the samples during operation with the nominal forward current (I_f = 700 mA) were recorded using a high-end thermography system Image IR 8300 from Infratec. An emissivity correction was made by a calibration measurement with a miniaturized thermocouple at the LED pad. For this purpose, thermographs of the sample at no operation (under isothermal conditions) are made at different temperature levels. In this way, emissivity pictures at temperature as known from the thermocouple measurement are obtained and used to convert the spatial radiation information into temperature distributions.

From the evaluation of transient thermal response on power-on-steps with the nominal power value, we see that the final temperature distribution over the entire sample surface is obtained within only a few seconds in all cases. The temperature distributions obtained by IR thermography in the steady state are compared for all four sample types in Fig. 4. During experiments with the nominal forward current, a voltage drop of $4V_f$ = 13.5 V was measured (four single LED elements in one module, connected in series). Assuming an average photonic efficiency of η = 20%, we considered a continuous power loss of 7.56 W per sample. Since establishing of the junction temperature was related to high uncertainty, we defined the pad-to-cooler thermal resistance $R_{th,p\text{-}c}$ as the relevant parameter characterizing the thermal performance of the PCBs in the following way:

$$R_{th,p\text{-}c} = \frac{T_{pad} - T_{cooler}}{4V_f \cdot I_f \cdot (1 - \eta)} \quad (3)$$

where T_{pad} is the temperature of the copper pad in the vicinity of the LED submount body and T_{cooler} is the temperature of the copper block. Using the respective temperature values from the IR thermography images and the values mentioned above, results from eq. (3) were obtained, as listed in Table I.

C. Thermal Measurements/Results

From the IR thermography picture of the DK6 sample, a well-developed heat spreading effect can be recognized (Fig. 5). The temperature gradients in the vicinity of the LED chip are the lowest ones compared with the other three types, thus the heat flux is conducted into the cooler through an enlarged area of the dielectric. This high heat spreading effect is due to the excellent thermal coupling of the two copper layers by microvia arrays. However, because of the thick dielectric—a 90 μm thick prepreg with moderate thermal conductivity of only 0.3 W/mK—the temperature distribution and therewith $R_{th,p\text{-}c}$ reaches the highest values.

Considering the copper layout the DK2 and DK6, the samples are very similar (it should be noted that the thin copper layer at the "plugged" via front faces does not contribute much to the heat dissipation). Although the thickness of the FR4 in the DK2 is five times higher than that in the DK6, the heat is conducted into the cooler at a remarkably lower temperature because the thermal vias are in intimate contact with the cooler. This also leads to a steeply declining temperature in the lateral direction outside of the LED chip.

Significantly lower as on the first two PCB types are the temperature distributions on the two IMS type samples. In spite of a heat flux density of more than 50 W/cm^2, the maximum temperature of the LEDs is lower than 40°C for the IMS1 sample and even lower than 33°C for the IMS3 sample. This can be explained by the higher thermal conducivity of the dielectric (in IMS1, 0.5 W/mK; in IMS3, 4 W/mK).

Advanced Thermal Management Solutions: Cavity Boards

A. Introduction

Another possibility to reduce the thermal resistance of the PCB is the use of cavities. Local depth reduction (through

Table I
IR Thermography Measurement Results and Evaluated Thermal Resistance Values

Sample type	$T_{pad,IR\text{-}cam}$ (°C)	T_{pad} (°C)	T_{cooler} (°C)	I_F (mA)	P_{el} (W)	$R_{th,p\text{-}c}$ (K/W)
DK2	36.0	41.6	13	700	9.45	3.8
DK6	42.9	49.6	13	700	9.45	4.8
IMS1	28.2	32.6	13	700	9.45	2.6
IMS3	26.6	30.8	13	700	9.45	2.3

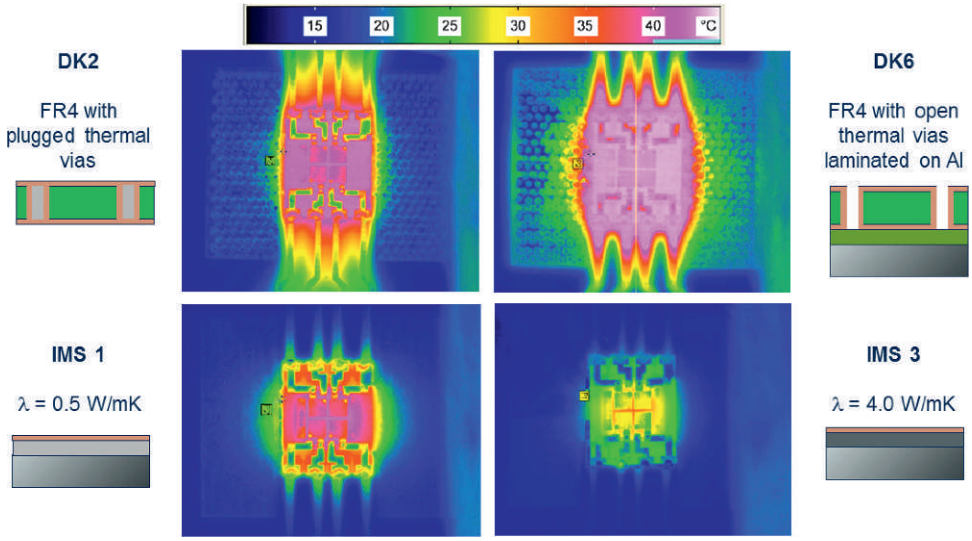


Fig. 5. Comparison of results obtained from IR thermography measurements.

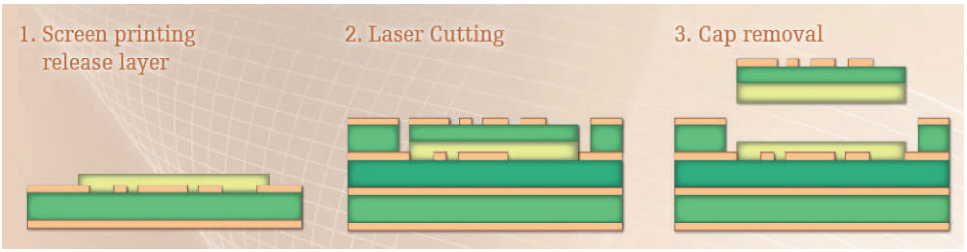


Fig. 6. Schematic process flow of cavity formation.

various methods and technologies) has long been applied to achieve a number of design and/or application linked results.

In this section the advantages of PCBs with special cavities with regard to advanced thermal management performance are presented.

B. Cavity Formation

Cavities are widely used in PCBs for different applications. Usually, these cavities are formed by the lamination of precut laminates and no-flow prepregs. The production method of PCBs with cavities presented in this paper is based on patented technology [5] that enables the removal of multiple layers at varying depths. The specific depth is achieved by the application of a paste on the release layer with subsequent relamination of the entire board. A laser cutting process then trims and cuts at the predetermined shape to separate the relaminated layers from the release layer. This process sequence now offers a very accurate (in *xy* and *z* axes) cavity formation process while keeping the state-of the-art design rules as the boards are flat until the end of production. The final steps are cap removal and paste stripping (Fig. 6). What remains is the solder footprint pattern. Diverse surface finishes and also the application of a solder mask can be employed in the cavities.

In order to achieve an optimal thermal performance, the cavity formation process of Fig. 6 is modified, so that all dielectric layers are removed and only the bottom copper foil remains. The high power chip is directly attached to the cavity at the bottom copper layer of the cavity. In this configuration, a very short thermal path with the lowest possible thermal resistance [i.e., eq. (3)] between the component and the heat sink is formed. It consists of only the adhesive or solder layer of the component-PCB connection, the bottom copper layer of the PCB, and the thermal interface material between the PCB and the heat sink (Fig. 7).

Surface finishes such as ENIPIG are applied on all layers, and the electrical interconnection is accomplished with wire bonding onto pads on the top or medium layer (Fig. 7 and 8). For light applications, the cavity walls can be coated with highly reflective material as well (Fig. 9).

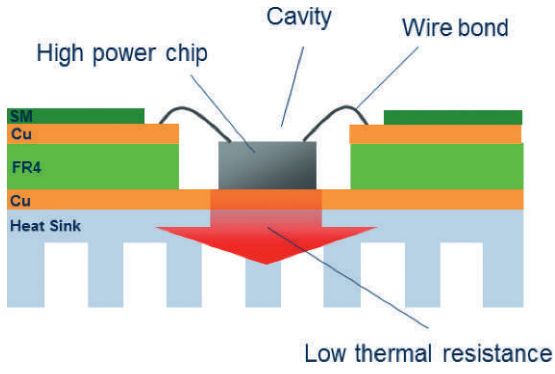


Fig. 7. Chip in cavity buildup with optimized thermal path.

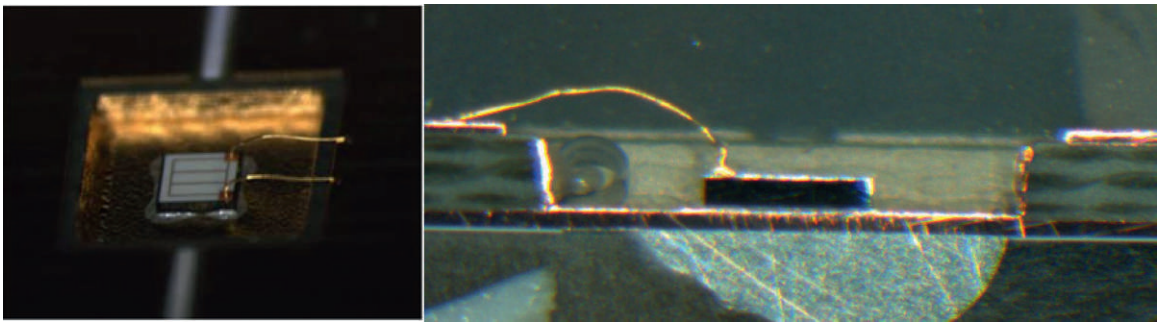


Fig. 8. Chip in cavity bonded to the upper layer.

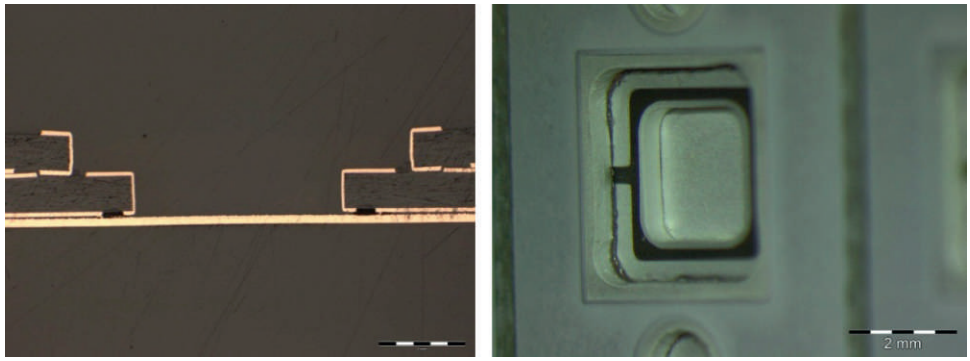


Fig. 9. Cavity in cavity board with high reflective cavity walls.

Apart from the excellent thermal behavior, this cavity board also shows additional advantages: It serves as package, which protects the component and in combination with an additional cavity (cavity in cavity, Fig. 9) it also protects the wire bonds. All together, the concept results in a miniaturization in the z direction and finally in a reliable chip-package solution that supports long-term stability of LED-based luminaires.

C. Thermal Simulation

It is difficult to compare the overall thermal performance of different packaging concepts purely on the basis of single point temperature measurements. A deeper understanding of the particular advantages and bottlenecks of particular setup features is gained by thorough thermal simulations. In the following, we compare three different packaging concepts using the same LED chip and the same operating conditions (i.e., forward current, $I_F = 300$ mA). These blue-light emitting LEDs were assumed to produce a power loss of $P_{loss} = 660$ mW, while the color conversion to white light is related to additional losses due to Stokes shift and absorption in the glob top for a total amount of 160 mW. Although this value might appear small, it should be noted that these optical losses are set free in a silicone matrix with low thermal conductivity. This kind of loss causes by far the highest temperature values inside the LED setup. We considered the spatial distribution of these losses (an exponential approximation of the decrease of the loss intensity with increasing distance to the LED surface) with an onion shell model [6]. The test assembly is assumed to be mounted on a heat sink with a constant temperature of 25°C. Thus, at the assembly's bottom face, Neumann boundary conditions were considered: $T_C = 25$°C. Further boundary conditions on the remaining surfaces were considered as natural convection and radiation assuming an emissivity of 1. Three-dimensional steady-state thermal simulations with the finite element method using a Multiphysics software package with materials data were made for all setups of the considered packaging concepts as shown in Fig. 10.

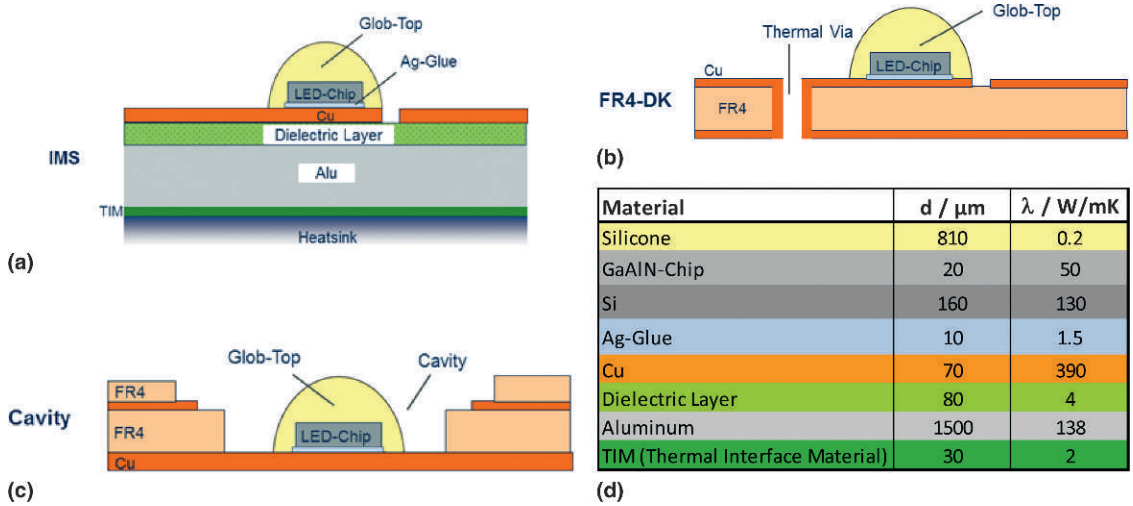
Fig. 11 depicts the thermal model of an FR4-DK setup as shown in Fig. 10b. In order to reduce the necessary node number without loss of accuracy, the hollow thermal vias were replaced by cylinders filled with a substitute material of which the thermal conductivity in the perpendicular direction is equivalent to the hollow cylinder shaped copper vias with a wall thickness of 25 μm (Fig. 11b). In this way, a virtual thermal conductivity λ_{sub} of the via can be calculated on the basis of the thermal conductivity λ_{Cu} of copper, the cross sections of the copper walls A_{Cu}, and of air (DK6) or epoxy (DK2) in real vias [7]:

$$\lambda_{sub} = 4\frac{\lambda_{Cu}A_{Cu}}{d^2\pi} \tag{4}$$

where d is the drilling diameter and the thermal conductivity of air or epoxy is neglected in comparison with λ_{Cu}.

D. Results

The thermal simulation revealed that under normal operation conditions all three investigated packaging concepts allow the LED-chip surface temperature to remain at moderate levels between 27.5°C (LED-in-cavity concept) and 45.5°C (FR4-DK concept) and that very high temperature



Material	d / µm	λ / W/mK
Silicone	810	0.2
GaAlN-Chip	20	50
Si	160	130
Ag-Glue	10	1.5
Cu	70	390
Dielectric Layer	80	4
Aluminum	1500	138
TIM (Thermal Interface Material)	30	2

(d)

Fig. 10. Buildup of: (a) IMS, (b) FR4-DK, and (c) cavity board (LED-in-cavity); (d) material parameters used for thermal simulation.

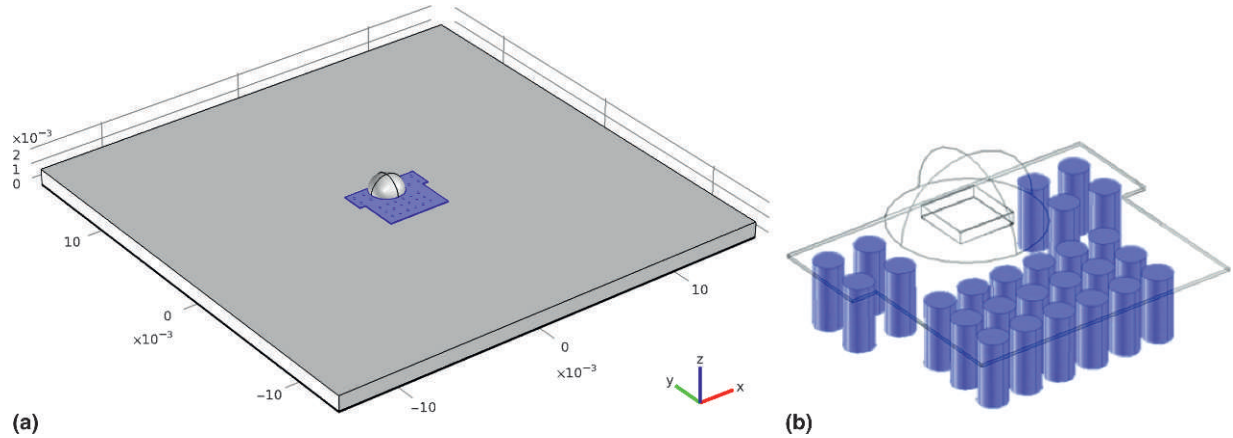


Fig. 11. Thermal model of the FR4-DK test sample: (a) entire model; (b) detailed view thermal via array.

gradients (more than 200K/mm) exist in the silicone glob top immediately above the chip surface. In all cases, the temperature maximum is found at the glob top surface (ca. 85°C at the IMS, ca. 95°C at the FR4-DK, ca. 70°C at the LED-in-cavity samples). Fig. 12 depicts the temperature distribution of an LED-in-cavity sample. For reasons of comparability, in all cases the shape of the color converter was assumed to be a spherical glob top. It should be noted that in a real case of the LED-in-cavity, the color converter does not tower above the PCB top surface. Therefore, the height of the color converter and thus the maximum temperature is even lower than considered in our simulation. The quite remarkable temperature differences inside the LED chip and color converter of the three concepts can be understood by considering the temperature course along the perpendicular symmetry axis.

In spite of a heat flux density of more than 80 W/cm^2, the LED-in-cavity setup keeps the LED chip at a temperature level below 28°C due to the 70 µm thick copper base layer and the shortest possible heat conduction path. The most significant temperature drops can be found in the thermal interface layer (TIM) between the heat sink and the copper base layer and in the adhesive layer under the LED chip (Fig. 13).

The IMS module shows an LED-chip temperature between 32°C and 34°C. The most significant temperature drop is caused by the dielectric between the copper layer and the aluminum plate. The excellent thermal conductivity of the aluminum plate and the 35 µm thick copper layer can be recognized by the almost negligible temperature change inside the layer.

The highest temperature differences between heat sink and LED chip are found in the FR4-DK samples. Due to the fact that the thermal vias are placed only in a pad range apart from the LED chip instead of beneath it, the path for a major part of the heat flux is comparatively long. This leads to LED chip temperature between 32°C and 41°C, depending on the choice of geometry variation (via count, drilling diameter, Cu thickness, etc.). In this context, the feature of the plugged via technology should be highlighted: Although the thermal conductivity of a plugged via is practically the same as the open one with same hole geometry, with plugged vias the perpendicular temperature drop across the PCB can be reduced significantly because they can be placed directly beneath the LED chip without the risk of solder soaking. The respective temperature functions along the perpendicular symmetry axis are compared with each other in Fig. 14.

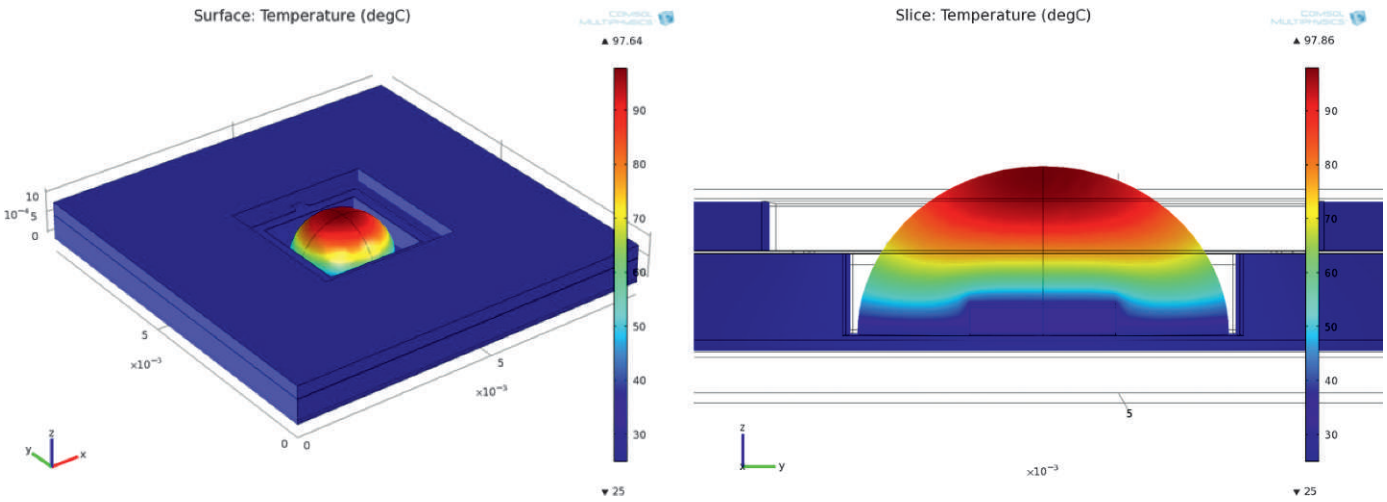


Fig. 12. Results of thermal simulations; detailed views of temperature distribution in vicinity of the LED.

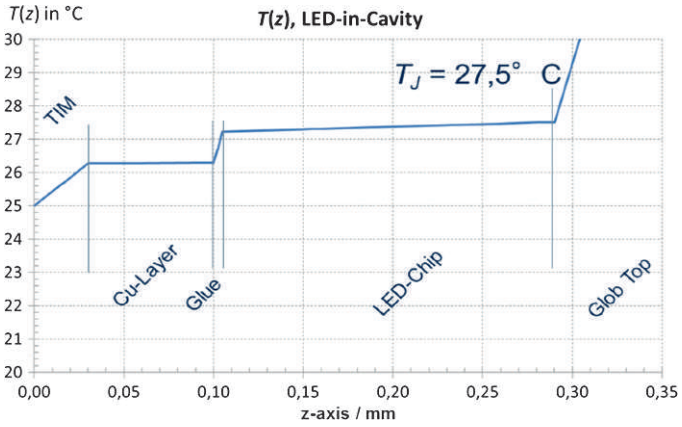


Fig. 13. Results: Temperature profile along the symmetry axis in out-of-plane direction (z axis) of an LED-in-cavity setup.

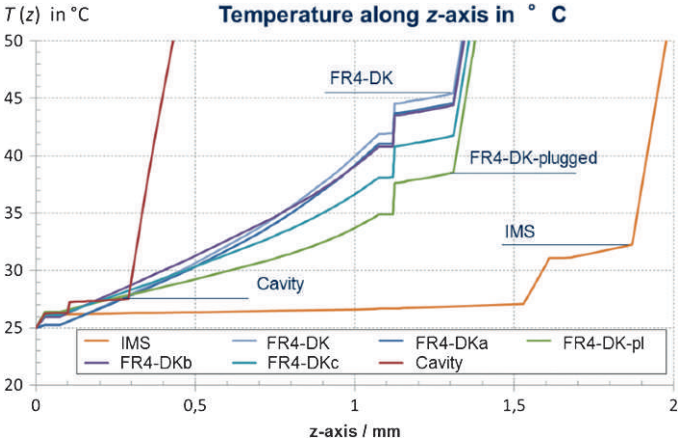


Fig. 14. Comparison of the results of the different PCB technologies.

Using the average temperature of the LED chip surface as the junction temperature and the heat sink temperature as the ambient temperature, we defined the junction-to-ambient thermal resistance and used this measure as the most representative comparison for all investigated setups (Fig. 15). The by far lowest thermal resistance can be seen at the LED-in-cavity setups, followed by the IMS variants. However, it must be said that an insulation layer between the heat sink and the semiconductor is frequently unavoidable. An insulating layer between the copper layer and the heat sink is also possible for the LED-in-cavity solution but would also increase the thermal resistance. Conventional FR4 PCBs with thermally optimized via technology have higher thermal resistances but proved to be attractive and cost-effective variants, at least for the midpower range.

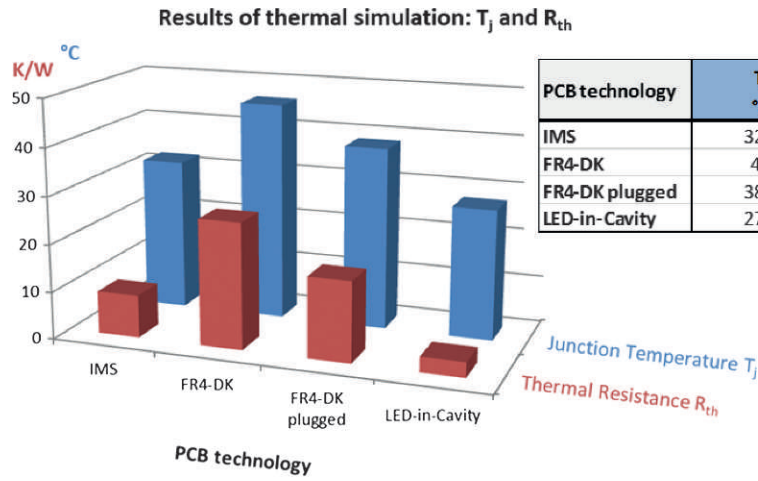
Advanced Thermal Management Solutions: Cu-Filled Thermal Vias

A. Introduction

Thermal vias have been employed for a long time to improve the heat transfer between the two sides of the PCB and to couple heat spreading copper areas. Because of the fact that thermal vias are normally hollow cylinders, solder can be soaked by the vias as mentioned above, and therefore, components are frequently not directly placed on top of the via array. Exceptions are large high power components where enough solder can be applied without the risk of critical voids forming underneath the component. This problem can be fully avoided if vias are fully filled with copper using a reverse plating process [8]. This can also help to increase the heat transfer area dramatically as demonstrated by the following simple consideration. By comparing the cross section of a hollow via A_{hollow} with the one of a filled via A_{filled}, an average copper cross section ratio β can be calculated as follows:

$$A_{\text{hollow}} = \frac{d^2 - (d-2a)^2}{4}\pi, A_{\text{filled}} = \frac{d^2}{4}\pi, \beta = \frac{A_{\text{filled}}}{A_{\text{hollow}}} = \frac{1}{4}\cdot\frac{d^2}{ad - a^2} \tag{5}$$

where d denotes the via diameter and a the via copper plating thickness. For example, for a via with $d = 200$ µm and $a = 30$ µµm, $\beta = 1.96$, which clearly shows that by using



PCB technology	T_j °C	$R_{th,j\text{-}amb}$ K/W
IMS	32.1	9
FR4-DK	46	26.5
FR4-DK plugged	38.4	16.9
LED-in-Cavity	27.5	3.2

Fig. 15. Comparison of the results of the different PCB technologies.

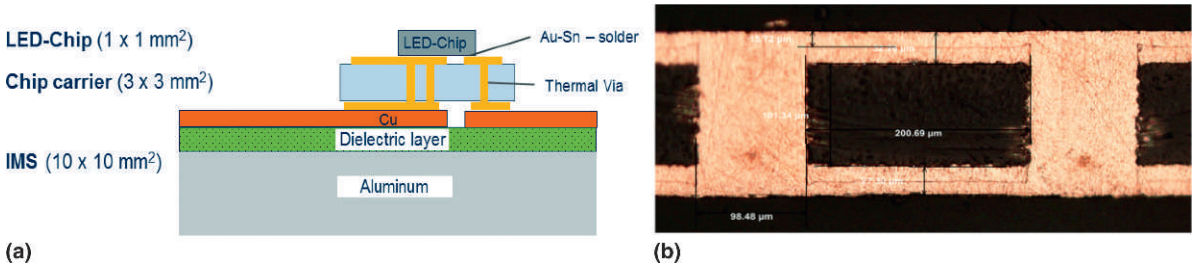


Fig. 16. (a) Chip carrier module buildup; (b) cross section of chip carrier.

filled vias, the thermal resistance between the top and bottom side can be cut in half.

B. Module Buildup and Thermal Simulations

For an investigation of the effectiveness of the filled-via approach, a setup according to Fig. 16a is considered. An LED chip of 300 µm thickness and 1×1 mm^2 lateral dimensions is soldered by Au80Sn-solder onto a bismaleimide triazine (BT) submount (3×3 mm^2) that is copper coated (35 µm) on both sides forming the thermally relevant structure of the LED submount. Filled vias ($d = 200$ µm, $N = 20$) connect top and bottom side of the submount (Fig. 16b). This submount is soldered with Sn96Ag solder onto an IMS-carrier (10×10 mm^2) acting as heat spreader and heat sink interface. The solder layers were not modeled (omitted) because the temperature drop caused by the heat flow would be less than 50 mK. The aluminum part of the IMS was replaced by a constant temperature boundary condition. Table II lists the thermal properties of the materials inside the model.

Table II
Material Properties of Components Used for Finite Element Model

Component	Material	Thermal conductivity λ (W/mK)
LED	Sapphire	36
Traces and vias of PCB	Copper	390
Dielectric of PCB	BT	0.12
Solder	Sn96Ag	Not modeled ($\Delta T < 50$ mK)
Dielectric on heat sink	Transtherm T2022	0.6
Dielectric of IMS	Filled epoxy	1.0 (thickness = 100 µm)

C. Results

The simulation results show that it is highly beneficial to use filled vias to reduce the resistance of the thermal path, as shown in Fig. 17 and Table III. The component can be placed directly on top of the vias without any problems due to insufficient solder (e.g., because of solder sucked up by the copper clad via hole). However, experience gained from manufacturing makes it clear that via-filling is not always perfect and dimples on the surface can occur. Such an air void inside the solder layer beneath the chip is shown in Fig. 18. The meaning of the solder defect due to the dimple formation in the galvanic process mechanical reliability will be investigated in further studies. However, thermal simulation proved that they are insignificant for thermal resistance. Also, optimization of via geometry and placement will be conducted, as well as the influence of copper thickness of the top layer that contributes the most to initial heat spreading of the chip's power loss.

Summary

Several different concepts for thermal management solutions on PCBs for high power applications were shown in this paper. Benefits of state-of-the-art concepts, such as insulated metal substrates and open or plugged thermal vias were

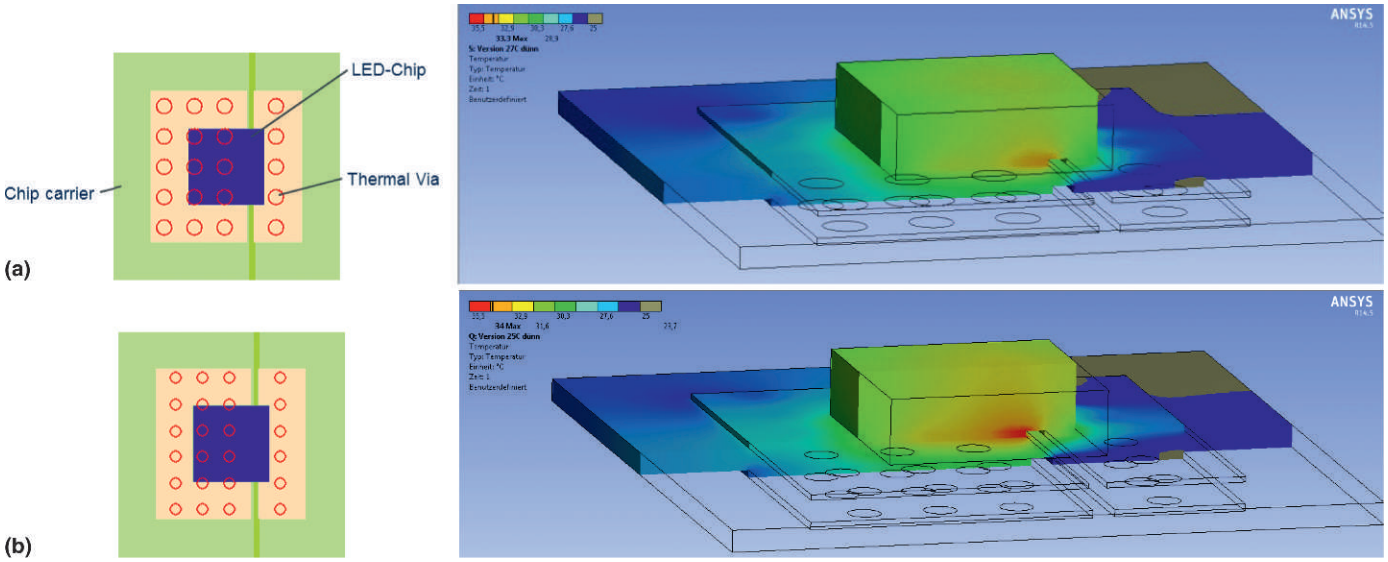


Fig. 17. Chip carrier design and first results of thermal simulation: (a) 20 vias, $d = 200$ µm; (b) 24 vias, $d = 150$ µm.

Table III
Maximum Temperature and Thermal Resistance with Different Thermal Via Setups

Variant	Via diameter (µm)	Number of vias		Effective via cross section (mm^2)		Maximum temperature (°C)	Thermal resistance (K/W)
		All	Under chip	All	Under chip		
Fig. 17a	0.2	20	5.9	0.5	0.19	33.3	10.9
Fig. 17b	0.15	24	5	0.42	0.09	34	11.6

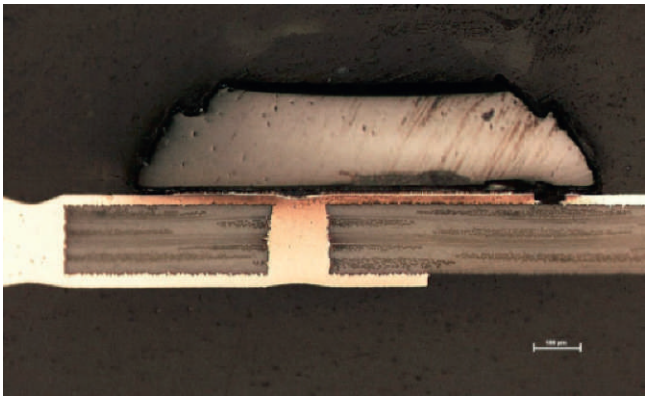


Fig. 18. Chip carrier with dimple inside via.

illustrated by comparing the thermal performance of high-power LED modules built up with different concepts. Particularly interesting thermal management solutions were the plugged thermal vias and the insulated metal substrates, as they allow short heat conduction paths to be realized.

Apart from these well-established variants, some new concepts were presented. Cavity boards (boards with local depth reduction) show thermal advantages due to a reduced thermal path along the z axis through the board.

Thermal simulations of cavity boards attached with high power LEDs show excellent cooling performance. In comparison with the simulation results of state-of-the-art concepts, the cavity board approach shows by far the lowest thermal resistance of the board system and therefore also guarantees the lowest junction temperature for the attached high power component. The realization of test vehicles of these concepts is planned to verify the simulation data by thermal measurements on these test boards.

Furthermore, the thermal advantages of copper-filled thermal vias in chip carrier boards were presented. The first results of thermal simulations were shown and discussed. Further simulations and measurements on test vehicles are ongoing, and the results of these thermal investigations are also planned to be published in the near future.

Acknowledgments

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