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Heterogeneous Integration of a 300-mm Silicon Photonics-CMOS Wafer Stack by Direct Oxide Bonding and Via-Last 3-D Interconnection

Colin McDonough,[1,*] Doug La Tulipe,[1] Dan Pascual,[1] Paul Tariello,[1] John Mucci,[1] Matt Smalley,[1] Anh Nguyen,[1] Tuan Vo,[1] Corbet Johnson,[1] Phung Nguyen,[1] Jeremiah Hebding,[1] Gerald Leake,[1] Michele Moresco,[2] Erman Timurdogan,[2] Vladimir Stojanović,[3] Michael R. Watts,[2] and Douglas Coolbaugh[1]

***Abstract*—A fully functional Si photonics and 65-nm complementary metal-oxide semiconductor (CMOS) heterogeneous three-dimensional (3-D) integration is demonstrated for the first time in a 300-mm production environment. Direct oxide wafer bonding was developed to eliminate voids between silicon on insulator photonics and bulk Si CMOS wafers. A via-last, Cu through-oxide via 3-D integration was developed for low capacitance electrical connections with no impact on the CMOS performance. The 3-D yield approaching 100% was demonstrated on >20,000 via chains.**

***Keywords*—3-D-IC, direct oxide bonding, heterogeneous integration, silicon photonics, through-oxide via (TOV)**

Introduction

Silicon photonics and three-dimensional (3-D) integration are emerging technologies enabling higher-performance computing devices. Several of the key benefits of using photonic components compared with traditional electrical interconnects are lower power dissipation, lower latencies, and higher bandwidth. Furthermore, silicon photonics is fully compatible with current complementary metal-oxide semiconductor (CMOS) technologies, which allows for a direct transition into integrated circuit (IC) manufacturing [1-4]. The 3-D IC technology makes possible the heterogeneous integration of Si photonics with traditional CMOS technologies by wafer (or die) stacking [5-9].

Heterogeneous wafer stacking is accomplished by direct oxide wafer bonding and 3-D interconnects known as through oxide vias (TOVs). Direct oxide wafer bonding enables a robust physical system for downstream processing and high throughput for manufacturability. Furthermore, TOVs integrated in a via-last scheme are critical for Si photonics because of their lower via capacitance, measured at 1.45 fF per via for this process, compared with traditional through silicon vias (TSVs) resulting in >30 fF per via [10]. The main challenges for implementing this via-last integration approach are the preparation steps used for bonding and robust backside processes for TOVs.

Surface preparation is critical for high-strength, void-free direct oxide bonding [11-14]. It requires a clean, atomically smooth surface. However, the topography introduced by fully patterned wafers leads to bonding voids. Voids at the bond interface are detrimental to reliability, yield, and throughput. Since the photonic integration requires observation of the silicon on insulator (SOI) layer for characterization, backside substrate thinning is essential, and voids pose a challenge for this process. Therefore, topography needs to be minimized to prevent void nucleation and propagation during the bonding process.

Via-last integration provides unique challenges for patterning and metallization relative to traditional back-end-of-line (BEOL) processes. Thus, the key consideration is developing robust metal connections to multiple levels through the 3-D stack. Therefore, optimization of processes related to metallization was critical to reach high yield.

In this article, a fully functional, 300-mm wafer-level heterogeneous Si photonics-CMOS platform based on 65-nm CMOS technology is demonstrated under a controlled manufacturing environment for the first time. Fig. 1 provides an illustration of this integration approach. Electro-optic functionality of this platform is demonstrated for a full chip-to-chip photonic link in [8] and for an on-chip photonic link in [9].

Characterization Details

Characterization was critical for evaluating surface preparation techniques for direct oxide wafer bonding. Prior to bonding, spectroscopic ellipsometry was performed on a KLA-Tencor SPECTRA F5X-200 to measure the film thickness and uniformity for long-range variability. Atomic force microscopy (AFM) with a Veeco InSight 3-DAFM was used to measure surface roughness to quantify short-range surface variation. Values were compared with the reported values in literature. Finally, pattern-induced topography variations were measured using high-resolution profilometry (HRP) with a KLA-Tencor HRP-340. The quality of the bond was determined by analyzing the interface between the wafers for void formation using scanning acoustic microscopy (SAM) on a Sonix Vision.

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[1]Colleges of Nanoscale Science and Engineering, SUNY Polytechnic Institute, Albany, New York

[2]Massachusetts Institute of Technology, Cambridge, Massachusetts

[3]University of California, Berkeley, Berkeley, California

*Corresponding author; email: cmcdonough@sunypoly.edu

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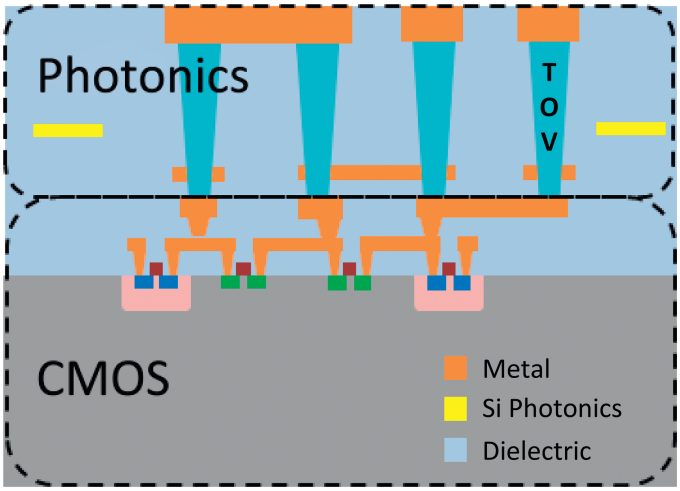

Fig. 1. Illustration of the 3-D wafer stack developed. A Si photonics wafer is bonded to a 65-nm CMOS wafer. Note: not to scale.

Characterization of the TOV and backside metal levels was performed using scanning electron microscopy (SEM), and cross-sectional analysis and electrical characterization were performed using focused ion beam (FIB) and inline testing (ILT), respectively. SEM imaging using an Applied Materials SEMVision G2 was performed after TOV etching and postetch cleans to examine cleaning effectiveness. ILT using a TEL Precio Prober and Agilent 4073 Parametric Tester was performed after the last backside metal level for electrical characterization of the 3-D process and effect on the CMOS circuits. In particular, 3-D via chains were used to monitor 3-D yield, and ring oscillator performance (prebonding versus post-3-D processing) monitored the effect of the 3-D process on the CMOS yield. Finally, an FEI Helios NanoLab 1200AT was used to analyze etch profiles and metallization.

Development Approach and Results

A. Direct Oxide Wafer Bonding

Developing a robust direct oxide bonding process for integrated wafers requires minimizing surface topography and creating particle-free, hydrophilic surfaces. The nature of oxide-oxide direct wafer bonding relies on the hydrogen bond formation that results from water adsorption at the oxide surface. When put into contact, the wafers are held together by a network of hydrogen bonds formed between the molecules of the hydrated surface. It has been shown that a higher effective bonding energy and higher percentage of contact area of two wafers are achieved with smaller surface topography [11]. Surface variations, particles, or hydrophobic spots prevent hydrogen bond formation local to the surface defect. Specifically, these defects become sites for void nucleation whereby air is trapped during the bonding process. They decrease the bond strength and compromise reliability for downstream processes. Therefore, a smooth, particle-free, and hydrophilic surface is critical for bond formation [12, 13]. Consequently, a proprietary surface treatment scheme was developed to remove particulates and create a hydrophilic surface while minimizing surface topography.

Topography is introduced on multiple length scales and degrades surface contact between wafers during bonding. Long-range topography results from wafer-scale nonuniformity, such as film thickness variations. On the opposite side of the spectrum, short-range topography on the order of nanometers is mainly a result of surface roughness. Finally, the midrange length scale is dominated by pattern-induced topography. It is the main source of microvoid nucleation, which becomes critical from reliability and yield standpoints.

Long-range topography was minimized through chemical mechanical planarization (CMP). Within-wafer nonuniformity (WIWNU) is a key metric for evaluating surface nonuniformity across the wafer. WIWNU was calculated from film thickness measurements taken over 65 points across the wafer surface. Before CMP, WIWNU is 5.0%, which is an expected value from a single-wafer BEOL oxide deposition tool. After CMP, WIWNU decreases to 2.8%. Decreasing long-range topography is beneficial for improving long-range wafer contact area for bonding.

Surface roughness is found to have a direct impact on bond energy [11]. Reported values of root-mean-square (RMS) surface roughness for successful direct oxide bonding fall within 0.1-0.5 nm [11-15]. A representative AFM scan taken after final surface preparation and prior to bonding is shown in Fig. 2. RMS surface roughness of 0.1 nm was measured for a $10 \times 10\text{-}\mu m^2$ scan area. This compares favorably with the reported values that achieved high bond strength.

One of the most critical aspects of bonding fully integrated wafers is reduction of pattern-induced topography. It is measured using HRP and is typically on the order of 1,000 Å (Fig. 3)). In some cases, asperities have been observed on the order of several thousand angstroms, as shown in Fig. 3a. This amount of topography has led to pattern-specific, microvoid

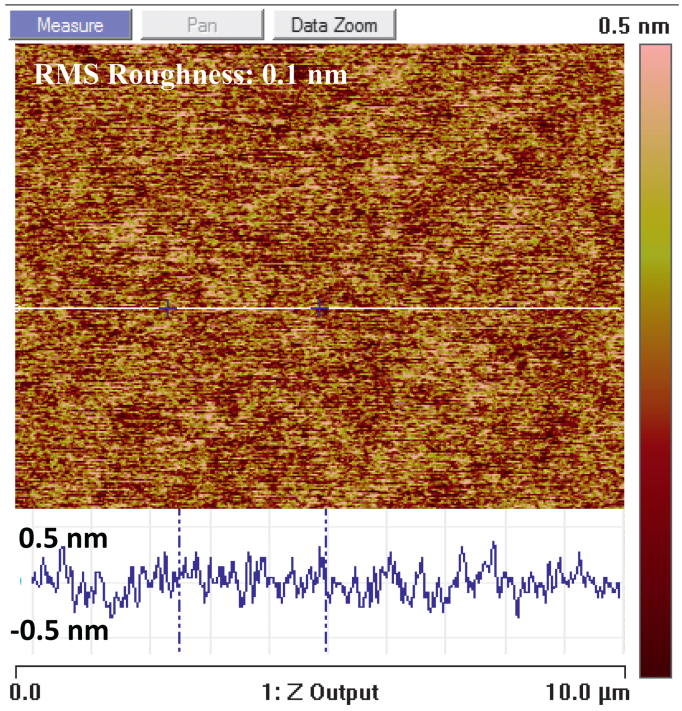

Fig. 2. AFM prior to bonding with RMS surface roughness of 0.1 nm.

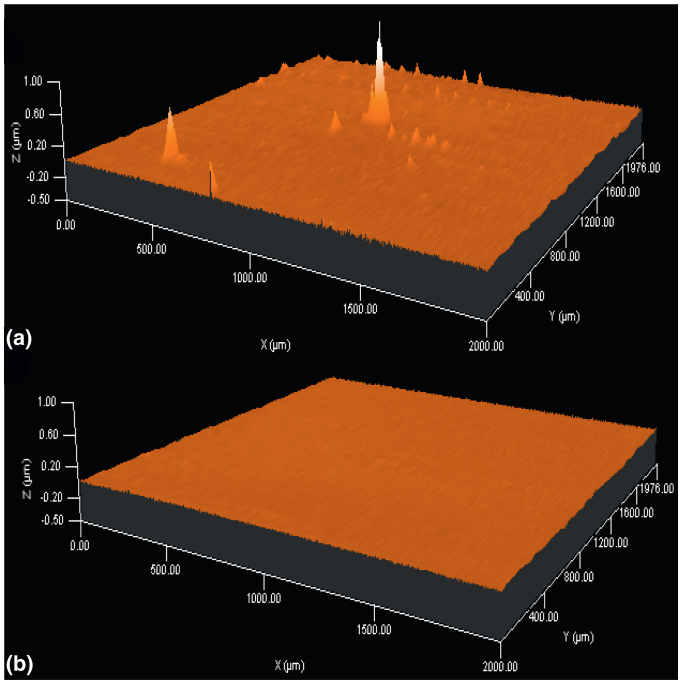

Fig. 3. Representative HRP scans (a) prior to reducing incoming, localized topography and (b) after multistep surface preparation for bonding. Regular, pattern-specific topographical features, as well as large outlier asperities, are represented in (a).

nucleation during bonding. Subsequent backside processing can lead to bubble formation that can compromise mechanical reliability of the bond and degrade yield. In extreme cases, wafers crack or break, most notably during aggressive processes related to bulk Si thinning. By implementing a proprietary, multistep process, topography was reduced to <500 Å. Comparing representative HRP scans (Figs. 3a and 3b) before and after this multistep process, it was clear that microscale topography was significantly reduced.

After wafer bonding, the interfaces were characterized by SAM imaging to inspect for void formation. Fig. 4 displays SAM images comparing Wafer 1, which did not receive proprietary surface preparation (Fig. 4b) to Wafer 2, which did (Fig. 4d). Individual die from within the full wafer scans are shown in Figs. 4a and 4c, respectively. Voids at the interface appear as bright spots, as seen in Figs. 4a and 4b. The large voids observed at the center and lower left quadrant of the wafer (Fig. 4b) are characteristic of particles at the bond interface. These are removed when the surface is properly prepared for bonding (Fig. 4d). Furthermore, when pattern-induced topography is not minimized, microvoids nucleate at those specific patterns, as seen in Fig. 4a, which are eliminated when topography is minimized prior to bonding, as seen in Fig. 4c.

A comparison of the percentage of void area for these two wafers is reported in Table I. The percentage of void area is calculated with respect to the total wafer area for a full 300-mm wafer as well as a representative die within each wafer. The total

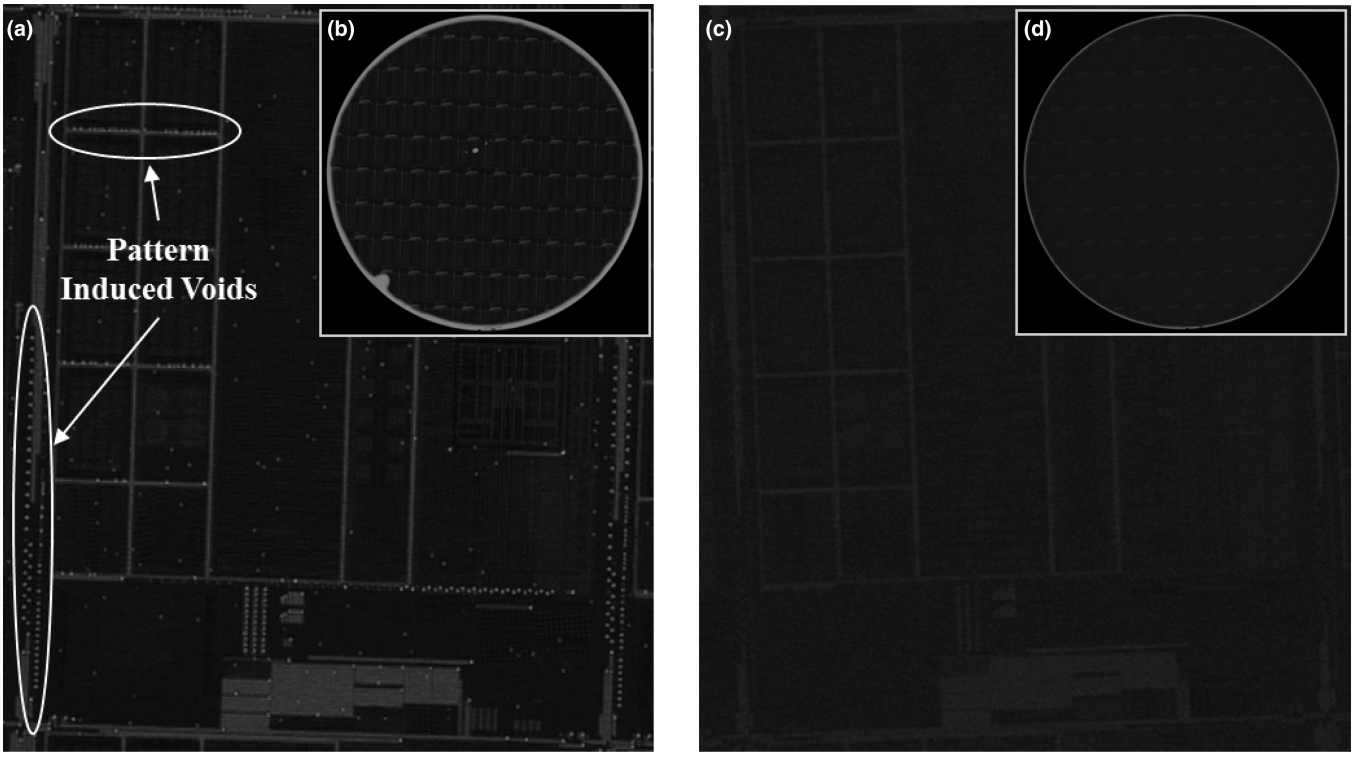

Fig. 4. SAM images of fully integrated, bonded wafers: without (a, b) and with (c, d) proprietary surface preparation. Full wafer scans are displayed as insets (b) and (d) for Wafers 1 and 2, respectively. Single die within the full scans are shown in (a) and (c). The pattern-induced microvoids are readily observed in the nonoptimized preparation scheme in (a).

Table 1
Void Area % and Total Number of Voids for Wafer 1 versus Wafer 2 Bonding Preparation

	Wafer 1		Wafer 2	
Area	% Voids	No. of voids	% Voids	No. of voids
Wafer	0.13	1,536	0.01	198
1 die	0.29	77	0.00	0

number of voids observed is also included. Because of resolution limitations, the smallest detectable void size is approximately 30 μm. The proprietary surface treatment reduces the number of detectable voids by an order of magnitude and the void area percentage by 92%. The voids observed on Wafer 2 were located at the wafer edge and not in the product area. Thus, void-free bonding is demonstrated in the patterned regions of the wafer when the proprietary surface treatment described above is used.

Although analysis of bonding voids is a good indicator of bond quality, a key test of robustness of the bond interface is wafer survival through Si thinning, which is typically an aggressive process. For example, Wafer 1 had significant chipping and crack propagation during Si thinning, which prevented it from further processing. Wafer 2, on the other hand, had no observable defects and did not develop any reliability issues during downstream processing, which confirmed the robustness of the surface preparation and subsequent wafer bond process.

B. Backside Processing and TOV

Backside processing refers to all post wafer-bond processing. A generic, backside via-last integration consists of removing the bulk Si photonics substrate, patterning the TOV to provide connection between the SOI photonics and bulk CMOS wafers, and patterning a backside metal level. Bulk Si thinning is achieved through a multistep process that has been optimized to reduce mechanical stress on the bonded wafer pair. It stops selectively on the buried oxide (BOx) of the photonics wafer to prevent damaging of the SOI devices. The TOV is etched through the entire photonics stack with an aspect ratio on the order of ∼4:1. While not as aggressive as a traditional TSV (aspect ratio of ∼10:1 or higher), this does pose more challenge than a standard BEOL via for metallization.

Electrical connection between the bonded wafers relies on the Cu TOV connecting the sidewall of the last photonics metal level and top of the last CMOS metal level. This proves challenging from both reactive ion etch (RIE) and metallization standpoints. The electrical connection at the sidewall of the photonics wafer is especially sensitive to the TOV RIE and post-RIE clean processes. Contamination at the interconnect interfaces can lead to higher resistances or create open circuits, thus degrading yield. Therefore, proprietary RIE and post-RIE cleaning processes were developed to minimize overetching of the photonics metal level and to clean up excess polymer and sputtered metal. Excess polymer buildup and sputtered metal prevent complete metal liner coverage or result in metal voids. This leads to high resistance, or, in the worst case, open circuit

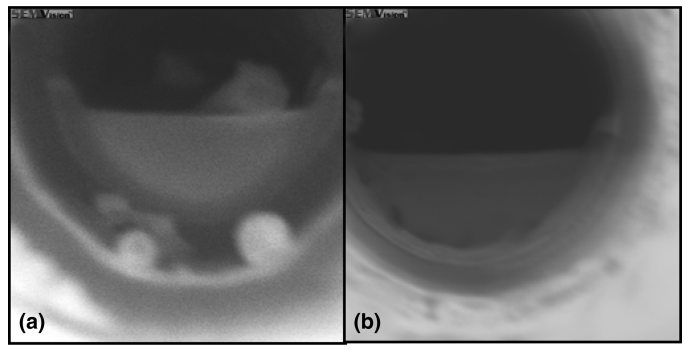

Fig. 5. Top-down SEM images looking down a TOV (a) after RIE and (b) after post-RIE cleans.

connections. Fig. 5 compares representative top-down SEM images of the inside of a TOV before and after cleaning. After RIE, residual polymer and sputtered metal are observed at the bottom of the TOV and on the sidewall (Fig. 5a). After applying our proprietary TOV cleaning treatment, the buildup is removed, as seen in Fig. 5b. As observed, the TOV RIE and post-RIE cleaning processes reduced polymer build-up and metal sputtering that are potential electrical yield detractors.

A cross-section of the completed backside 3-D stack is displayed in Fig. 6. The topmost CMOS and photonics wafer metal levels, TOV, and backside metal levels are labeled, and the region where the Si photonic devices are located has been highlighted for reference. It is observed from the cross-section that all metal levels are structurally connected.

Electrical testing confirms that the TOV makes reliable connection between the photonics and CMOS wafers. The 3-D yield approached 100% for >20,000 vias. Fig. 7 displays ring oscillator delay for the CMOS wafer before bonding and after backside 3-D processing. Ring oscillators are sensitive to process variations that can affect CMOS performance; therefore, ring oscillator stage delay was measured before and after 3-D processing to monitor how the 3-D process affects CMOS performance. The 3-D process showed a 0.2% increase in the stage delay, which is within the 95% confidence interval as determined by a paired *t* test; therefore, there is no statistically significant variation in ring oscillator delay for the bonded

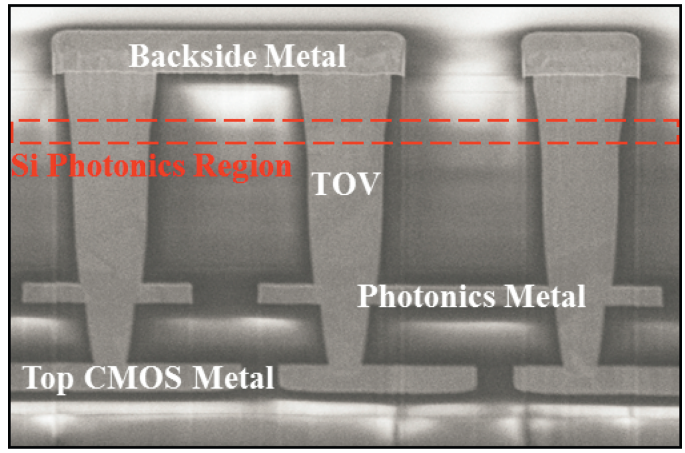

Fig. 6. FIB-SEM image of a TOV chain in a completed 3-D heterogeneously integrated Si photonics and 65-nm CMOS wafer.

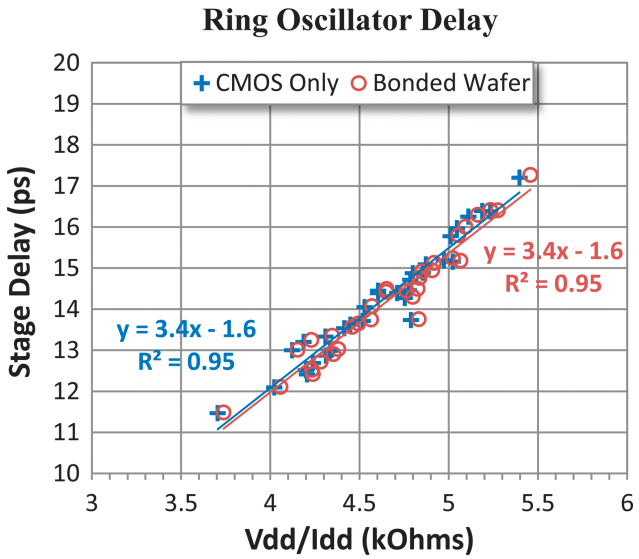

Fig. 7. Comparison of ring oscillator delay before and after the bonding process.

wafer. It can be concluded that the direct oxide wafer bonding and backside 3-D processes developed for this work do not significantly affect CMOS device performance. This is expected because thermal budgets are comparable to traditional BEOL processes.

Finally, TOV chain resistance variability for two TOV metal liner processes is displayed in Table II as percent SD for multiple via chain lengths. The standard liner process yields high variability in the TOV resistances. This appears to be independent of via chain length. On the other hand, the new liner process clearly displays better resistance stability, where the resistances measured for the new process fall within 5% of target for all via chain lengths. These key electrical metrics confirm successful integration of a 300-mm Si photonics-CMOS wafer stack.

Discussion

The main focus of this work was to develop and demonstrate a manufacturable Si photonics-CMOS wafer stack in a 300-mm manufacturing environment. To this effect, processes must be compatible with existing production technologies, and the end result must be a high-yielding product. The approach taken was a via-last 3-D integration utilizing a direct oxide wafer bonding process. This assured compatibility with existing production technologies. Two major concerns with wafer bonding are reliability of the bonding process and the impact of 3-D processing on CMOS performance. The two criteria of success for manufacturability, therefore, were mechanical stability of the wafer bond interface and electrical performance of the 3-D wafer stack at production end-of-line.

Table 2
Effect of Different Liner Processes on TOV Resistance Variability

	% SD	
No. of TOVs in chain	Standard liner	New liner
420	200	3.97
840	60.7	4.70
1,000	45.2	4.60
10,000	35.6	4.53
20,000	158	4.60

The literature has shown that a primary factor in high-strength, direct oxide wafer bonding is minimizing surface topography. Thus, a portion of this work was focused primarily on developing a proprietary surface preparation scheme for minimizing wafer topography prior to direct oxide wafer bonding. Void formation is related to surface preparation, in particular topography. Therefore, reducing topography, and voids, at the bond interface corresponds to higher bond strength (all other factors being the same).

Voids at the bond interface were characterized by SAM. Ideally, a void-free bond interface is desired. However, SAM has resolution limits on the order of 10^1 μm, and SAM used in this work had a resolution limit of ~30 μm. Voids of this size are readily detectable in postanalysis and were eliminated from the patterned regions using the surface preparation treatment developed here. Some voids were detected at the wafer edge, as described in the literature previously [15], due to the nature of the bonding process. Further development can eliminate these edge voids completely, but they were not found to be detrimental to the current work. Voids below the resolution limit of the SAM were most likely to be localized to smaller patterned features. The impact of such voids was not determined in this work, because they do not appear to have a significant impact on yield as observed here. Further work could be done for stress testing devices to investigate whether such small voids contribute to failure modes.

The impact of voids relates to bond strength, but also as defect sites that can cause yield loss: either entire wafers or within wafer. Voids can cause such defects as bubbles, delamination, cracking, and chipping. All of these have been observed in downstream processing on wafers that had known voids after bonding. The severity of these defects varies case by case. In the worst case, wafers break, which is problematic for manufacturing metrics. However, in all cases, there is considerable risk in continuing to process such wafers.

Interconnect yield and the effect of the 3-D process on CMOS performance were the main concerns with via-last integration. Stable interconnection is required for high yield and performance. Development of proprietary processes was critical for this work. A new metal liner process (Table II) significantly improved TOV resistance variability for up to >20,000 vias. This was most likely due to enhanced coverage reliability in the overall metal structure. The standard liner process may have had inconsistent coverage, which would affect TOV metallization. This, in turn, would have contributed to the random variability in the TOV resistance.

Finally, all 3-D processes were BEOL compatible to minimize the probability of affecting CMOS performance. However, it was unknown what the effect would be due to wafer bonding, Si thinning, or 3-D processing. Ring oscillators are sensitive to process variations that degrade performance (i.e., delay). The difference in delay of the bonded wafer versus the individual CMOS wafer was 0.2%. In addition, the slopes of the curves (i.e., capacitance) are the same, which further supports the claim

that via-last 3-D integration did not degrade the 65-nm CMOS device performance.

Conclusions

A first fully integrated Si photonics and 65-nm technology CMOS wafer has been demonstrated in a 300-mm wafer manufacturing environment. The surface preparation and direct bonding approach developed demonstrated highly repeatable, void-free bonding for fully patterned photonics and CMOS wafers.

A robust metal liner process has shown improvements in TOV resistance stability, and optimization of TOV patterning and metallization has yield approaching 100% of via chains up to 20,000 vias. Furthermore, it is demonstrated that oxide wafer bonding and subsequent 3-D IC processing did not degrade electrical performance of the CMOS devices in the substrate.

Acknowledgments

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