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Fan-Out Wafer-Level Packaging (FOWLP) of Large Chip with Multiple Redistribution Layers (RDLs)

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***Abstract*—This study is for fan-out wafer-level packaging with chip-first (die face-up) formation. Chips with Cu contact-pads on the front side and a die attach film on the backside are picked and placed face-up on a temporary-glass-wafer carrier with a thin layer of light-to-heat conversion material. It is followed by compression molding with an epoxy molding compound (EMC) and a post-mold cure on the reconstituted wafer carrier and then backgrinding the molded EMC to expose the Cu contact-pads of the chips. The next step is to build up the redistribution layers (RDLs) from the Cu contact-pads and then mount the solder balls. This is followed by the debonding of the carrier with a laser and then the dicing of the whole reconstituted wafer into individual packages. A 300-mm reconstituted wafer with a package/die ratio = 1.8 and a die-top EMC cap = 100 μm has also been fabricated (a total of 325 test packages on the reconstituted wafer). This test package has three RDLs; the line width/spacing of the first RDL is 5 μm/5 μm, of the second RDL is 10 μm/10 μm, and of the third RDL is 15 μm/15 μm. The dielectric layer of the RDLs is fabricated with a photosensitive polyimide and the conductor layer of the RDLs is fabricated by electrochemical Cu deposition (ECD).**

***Keywords*—FOWLP, chip first, face-up, reconstituted wafer, redistribution layer**

Introduction

In general, the value propositions of fan-out wafer-level packaging (FOWLP) are smaller form factor, higher performance, cost-effective solution, and easier for 2.5D/3-D integration. The first FOWLP US patent was filed by Infineon on October 31, 2001 [1, 2]. The first technical articles were also published by Infineon and their industry partners: Nagase, Nitto Denko, and Yamada [3, 4]. At that time (2006), they called it embedded wafer level ball (eWLB) grid array.

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In most FOWLPs such as eWLB by Infineon [3, 4] and STATS ChipPAC [5, 6], and TSMC's integrated fan out (InFO) [7, 8], the chip(s) is (are) embedded in an epoxy molding compound (EMC). In addition, in some fan-out panel-level packaging (FOPLP) such as those being studied by SPIL [9, 10] and Fraunhofer IZM [11, 12], the chip(s) is (are) embedded in an EMC. Other companies such as TI's MicroSiP [13] and Unimicron's Embedded Active Substrate [14] are embedding chips in a laminate organic substrate. In general, chips that are embedded in a laminated organic substrate cannot be larger than 5×5 mm^2 because of the thermal expansion mismatch between the silicon chip (2.5×10^{-6}/°C) and the organic substrate (15×10^{-6}/°C –to 18×10^{-6}/°C).

On June 28, 2013, Maxim Integrated filed a patent [15] for an invention, "fan-out and heterogeneous packaging of electronic components," proposing to embed the chip(s) in a silicon substrate [16]. Again, in general, the size of the chip cannot be larger than 4×4 mm^2 (or the size of the silicon package cannot be larger than 5×5 mm^2). This is because of the thermal expansion mismatch between the silicon (package) substrate (not the chip) and the Printed Circuit Board (PCB) (18×10^{-6}/°C).

George Institute of Technology (2017) provided an alternative to EMC, organic laminate, and silicon by presenting the very first demonstration of chips embedded in a glass substrate [17]. This adds a new direction in fan-out packaging.

There are at least three different processing methods in FOW/PLP [18], namely, chip-first and die face-down such as the eWLB, chip-first and die face-up such as the InFO, and chip-last such as the redistribution layer (RDL)-first by NEC Electronics Corporation (now Renesas Electronics Corporation) [19, 20]. In this study, the chips are embedded in an EMC. The packaging assembly method is by chip-first and die face-up FOWLP processing [7, 8, 18, 21] as shown in Fig. 1. The uniqueness of this process is to fabricate Cu contact-pads on the device wafer. These Cu contact-pads are for building the RDLs after post-mold cure (PMC) of the EMC and backgrinding of the EMC [21]. Three RDLs are built.

In this study, the feasibility of the design, materials, process, and fabrication of a fan-out wafer-level package is demonstrated. Images of the fabricated structures and cross sections are also provided and discussed.

Test Chip

A. Layout of the Test Chip

The dimensions of the test chip are 10 mm × 10 mm × 150 μm. There are 544 peripheral pads (two rows) on a 150-μm

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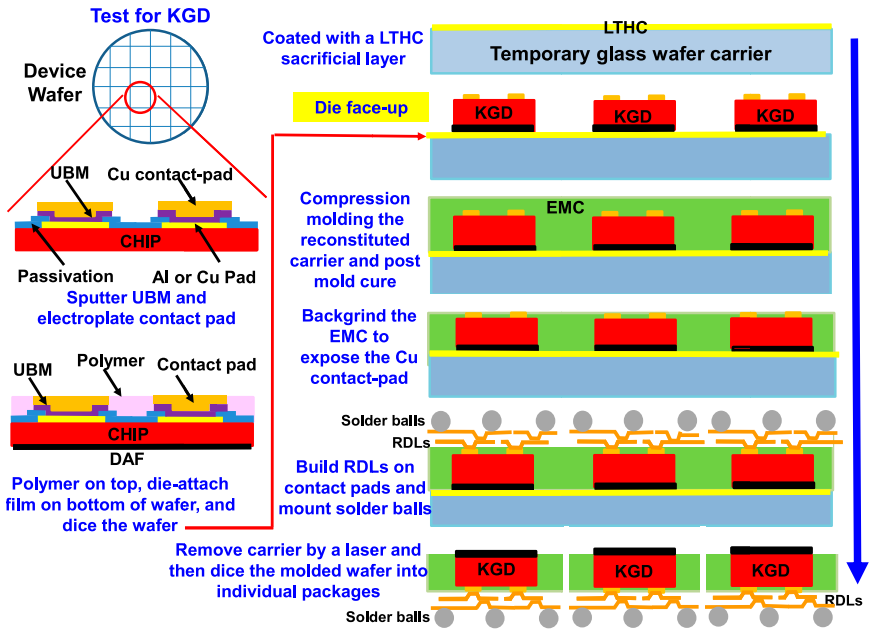

Fig. 1. Key process steps of the chip-first and die face-up FOWLP.

pitch staggered as shown in Fig. 2a. There are 1,444 inner pads on a 200-μm pitch. Thus, there are 1,988 total pads on the test chip. The pad geometry and material are shown in Fig. 3. It can be seen that the polyimide (PI) opening of the Al pad is 40 μm in diameter and is 5 μm thick. (Later on, because of the Cu smear under backgrinding of the EMC to expose the Cu contact-pad, the thickness of the PI was increased to as tall as the Cu contact-pad). The SiO_2 passivation opening of the Al pad is 50×50 μm^2 and the size of the Al pad is 70×70 μm^2. The Cu contact-pad is 60 μm in diameter and is 25 μm tall from the Al pad.

B. Test Chip Sample

For the device wafer, after the test of Known Good Die (KGDs), a Ti/Cu as a bottom layer of under bump metallurgy (UBM) is sputtered using physical vapor deposition (PVD) on the Al (or Cu) pad, and a Cu contact-pad is electroplated on the UBM. It is followed by spin coating a polymer, e.g., PI, on the front side of the device wafer. The backside of the device wafer is laminated (at ~70°C) with a (~20 μm) die attach film (DAF) by Hitachi. The device wafer is then diced into individual KGDs.

Fig. 2b–d shows the top view of the fabricated test chip sample. Fig. 3 shows a typical cross-sectional view of the test chip. It can be seen that the actual dimensions such as the chip thickness, Cu contact-pad thickness and diameter, and PI thickness are reasonably close to the designed dimensions.

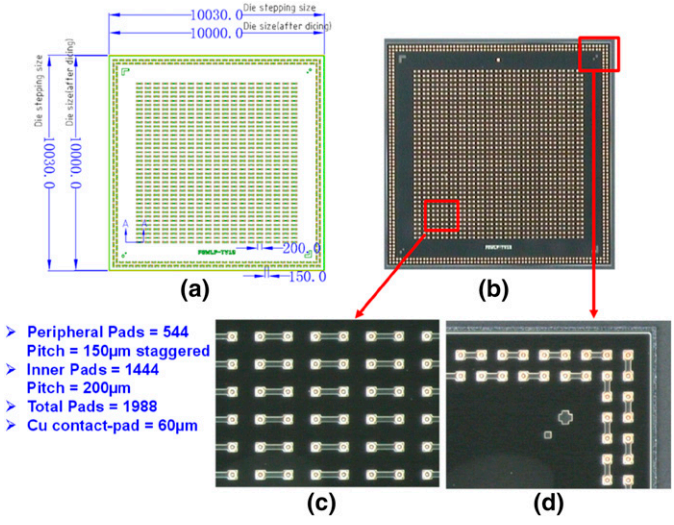

Fig. 2. Test chip dimensions and fabricated test chip.

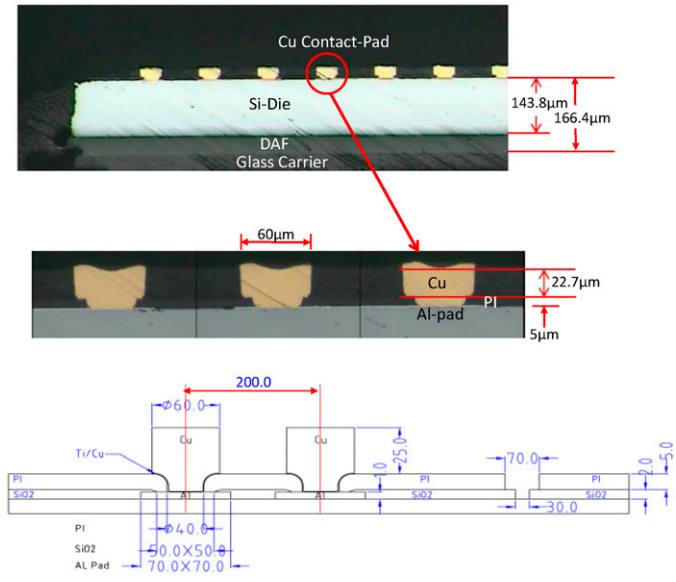

Fig. 3. Cross-sectional view of test chip (PI = 5 μm).

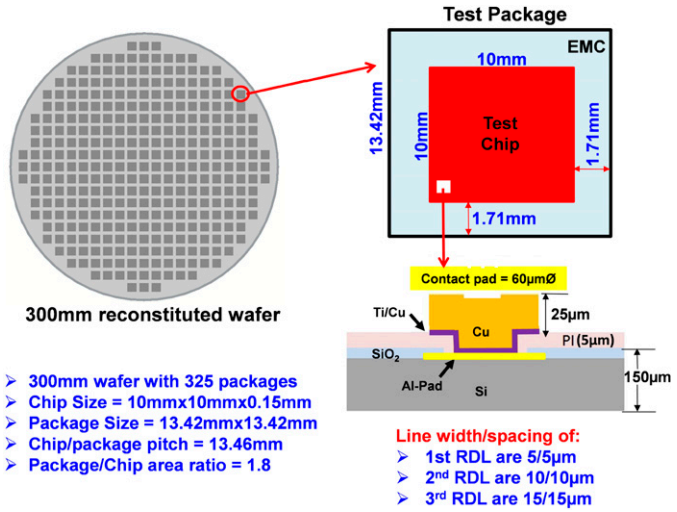

Fig. 4. Test package dimensions and test packages on reconstituted wafer.

Test Package

A. Layout of the Test Package

The dimensions of the FOWLP test package are 13.42 × 13.42 mm^2, as shown in Fig. 4. The test chip (10 × 10 mm^2) will be picked and placed on a 300-mm reconstituted wafer with a pitch = 13.46 mm. (A total of 325 test packages). Thus, the package/chip area ratio is 1.8 and the test package is 1.71 mm all around larger than the test chip. There are three RDLs of the test package. The dimensions of the line-width and spacing for the first RDL are 5 μm/5 μm, the second RDL are 10 μm/10 μm, and the third RDL are 15 μm/15 μm.

Fig. 5 shows the schematic of the cross-sectional view of the test package. It can be seen that there are 3 RDLs. Via (V_{C1}), through the first dielectric layer (DL1), connecting the Cu contact-pad of the test chip to the first RDL (RDL1) is 20 μm in diameter. The pad diameter on RDL1 is 55 μm, which is connected to RDL2 through via (V_{12}) with a diameter of 35 μm. Similarly, the pad diameter on RDL2 is 65 μm, which is connected to RDL3 through V_{23} with a diameter of 45 μm. Finally, 220 μm pads are formed on the bottom side of RDL3 and a V_{3P} with a diameter of 160 μm is formed through the passivation (DL4), a UBM and a 180-μm-diameter Cu contact-pad is formed for solder ball mounting. Fig. 6 shows the other case with UBM-less/Cu-pad for solder ball.

Fig. 7 shows the partial daisy chain design of the RDLs of the test package. Basically, there are three objectives of the layout of the daisy-chain of the RDLs: (1) to capture the delamination of the daisy-chain trace; (2) to capture the failure of the daisy-chain trace through the vias; and (3) to identify the failure of the solder joint (after they are assembled on the PCB), during drop and thermal-cycling tests.

B. Chip-First and Die Face-Up FOWLP Processing

Fig. 1 shows the chip-first and die face-up FOWLP processing flow. It starts off by coating the front side of a 300-mm temporary glass carrier (reconstituted) wafer with a very thin (~1 μm) light-to-heat conversion (LTHC) layer by 3M. The glass carrier thickness is 1 mm and its thermal expansion coefficient (TEC) is 7.6 × 10^{-6}/°C. The singulated KGDs are picked and placed (with a small force ≤ 2 kg and a temperature of 120°C for both bond-head and bond-stage) face-up on the LTHC layer of the reconstituted wafer as shown in Fig. 8a. This is performed by the NUCLEUS. Then, the DAF is cured at ~125°C for 1 h. It is followed by EMC dispensing, compression molding (125°C for 10 min), and finally post-mold curing at 150°C for ≥ 1 h, as shown in Fig. 8b. Compression molding is performed by the ORCAS.

Fig. 9a shows the top-side of the molded test packages on the glass reconstituted wafer with the LTHC layer. To see the chips,

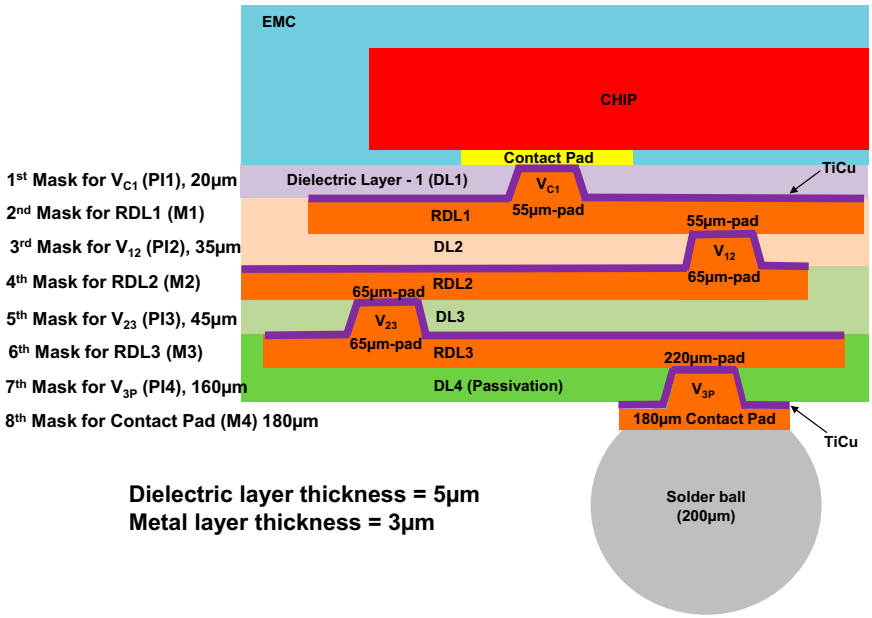

Fig. 5. Schematic of the cross-sectional view of the test package. (Conventional UBM/Cu-pad for solder ball).

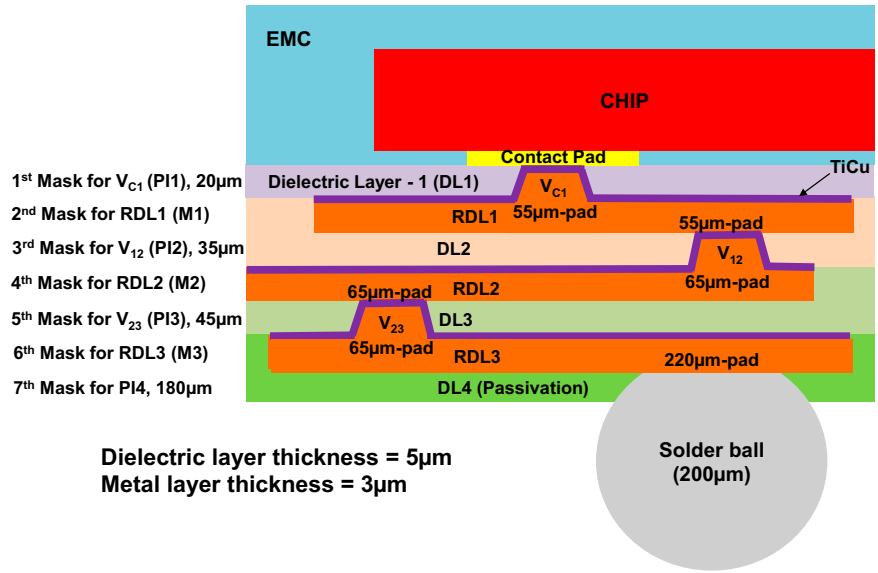

Fig. 6. Schematic of the cross-sectional view of the test package. (UBM-less/Cu-pad for solder ball).

some of the reconstituted carrier wafers are without the LTHC layer such as the one shown in Fig. 9b. It can be seen that there are 325 chips ($10 \times 10 \times 0.15$ mm^3) and molded test packages ($13.42 \times 13.42 \times 0.25$ mm^3). The package/chip area ratio is 1.8. Because the compression molding is by a keep-out zone method, the actual molded area is 3-5 mm (in diameter) smaller than the 300-mm reconstituted wafer.

The EMC is a liquid-like material (Nagase R4507) and its material properties are shown in Table I. It can be observed that the filler content is 85%. The average size of the filler is 8 µm and the maximum size of the filler is 25 µm. The flexural modulus of the EMC is 19 GPa and the viscosity is 250 Pa·s. The transition temperature (*Tg*) is 150°C.

The total thickness variations (TTVs) of a few typical molded reconstituted wafers are shown in Table II. This is a measurement of eight points around the peripheral and one point at the center of the reconstituted wafer. It can be seen from Table II that the TTV is about 10 µm.

Fig. 10 shows the warpage measurement contours (by the shadow moiré method) of a typical molded reconstituted wafer. It can be seen that the maximum warpage of the whole reconstituted wafer is 355.4 µm.

C. Cu Reveal (Backgrinding of the EMC to Expose the Cu Contact-Pads)

To fabricate the RDLs, the over molded EMC above the Cu contact-pad has to be removed (Cu revealing). DISCO's backgrinding machine is used to remove the EMC. During backgrinding, some of the areas have Cu smearing, as shown in Fig. 11. Because of the Cu smearing, the stepper will not work and the RDLs cannot be fabricated.

Another test chip has been fabricated. This time the polymer is much taller (~30 µm vs. 5 µm the first time shown in Fig. 4) and covered the Cu contact-pad as shown in Fig. 12. After pick and place, EMC dispensing, compression molding, PMC, and backgrinding, the resulting surface of the reconstituted structure is shown in Fig. 13. It can be seen that because of the polymer, there is no Cu smearing and the Cu contact-pad is ready for the fabrication of the RDLs.

D. Fabrication of the RDLs

The key process steps of fabricating the RDLs of the FOWLP (Fig. 5, with conventional UBM/Cu pad) are briefly discussed as follows (Fig. 14). First of all, the wafers are ultrasonic cleaned.

- Step 1: Spin-coat the photosensitive PI on the reconstituted wafer. Apply a stepper (every four test packages as a unit)

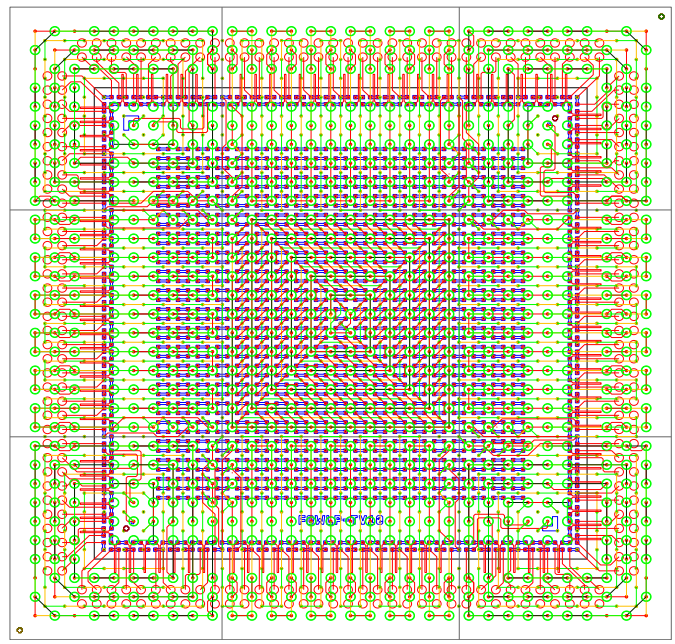

Fig. 7. Daisy-chain layout of the test package.

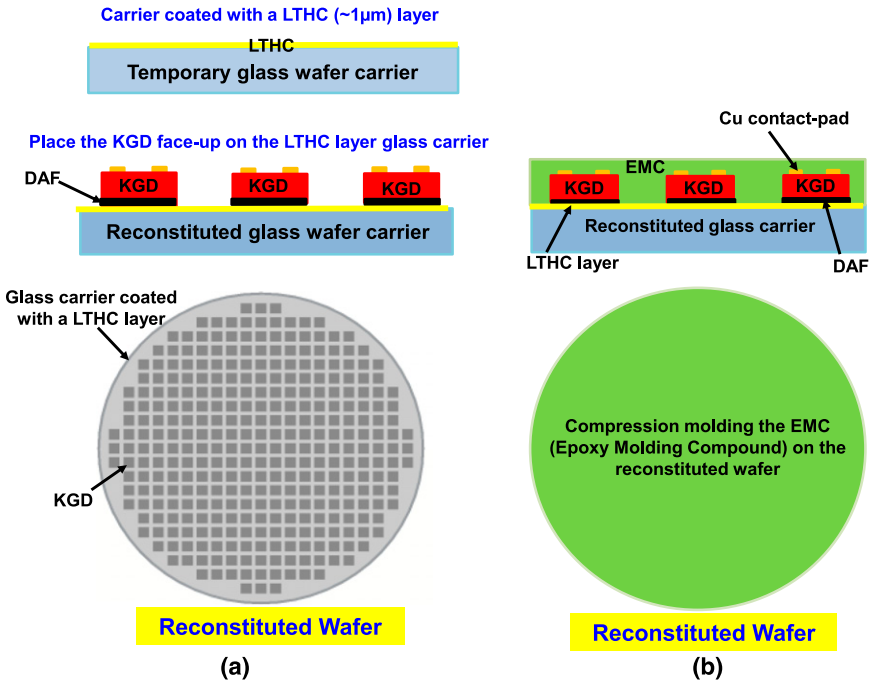

Fig. 8. (a) Picking and placing the test chip with DAF on the reconstituted carrier wafer with an LTHC layer. (b) Molding the EMC using the compression method.

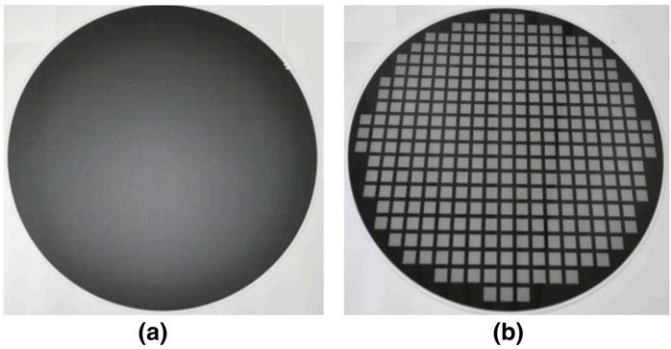

Fig. 9. (a) Top view of a molded reconstituted wafer. (b) Bottom view of a molded reconstituted wafer without the LTHC layer so we can see the test chips.

Table I
Material Properties of the EMC

Item	Unit	R4507
Filler content	%	85
Filler to cut	μm	25
Filler average size	μm	8
Specific gravity		1.96
Viscosity	Pa.s	250
Flexural modulus	GPa	19
Tg (DMA)	°C	150
CTE1	ppm/K	10
CTE2	ppm/K	41
Application		Fan-out
Special feature		Fine filler

and then use photolithography techniques to align, expose, and develop the vias of the PI. Finally, cure the PI at 200°C for 1 h. This will form a 4- to 5-μm-thick PI layer (PI development).

- Step 2: Sputter Ti and Cu by PVD (175-200°C) over the entire wafer.
- Step 3: Apply a photoresist and a stepper and then use photolithography techniques to open the redistribution traces locations.
- Step 4: Electroplate the Cu by electrochemical Cu deposition (ECD) (room temperature) on Ti/Cu in photoresist openings.
- Step 5: Strip off the photoresist.
- Step 6: Etch off the Ti/Cu. (RDL1 is obtained.)
- Step 7: Repeat Step 1 through Step 6 to obtain RDL2 and RDL3.
- Step 8: Same as Step 1 (for UBM).
- Step 9: Apply a photoresist and a stepper and then use photolithography techniques to open the vias on the photoresist for the desired bump pads.
- Step 10: Sputter Ti and Cu over the entire wafer.

Table II
TTV of Typical Molded Reconstituted Wafers

Position	Wafer-1	Wafer-2	Wafer-3
1	1,301	1,301	1,299
2	1,307	1,307	1,300
3	1,308	1,308	1,303
4	1,305	1,310	1,305
5	1,310	1,312	1,309
6	1,307	1,312	1,307
7	1,305	1,312	1,310
8	1,306	1,302	1,307
9	1,309	1,310	1,306
Range	9 μm	11 μm	11 μm

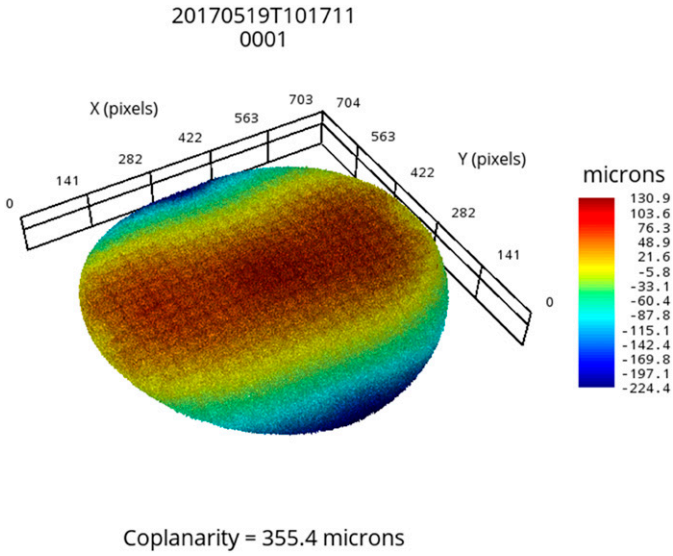

Fig. 10. Warpage measurement result of a typical molded reconstituted wafer.

- Step 11: Apply a photoresist and a stepper and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.
- Step 12: Electroplate the Cu pad.
- Step 13: Strip off the photoresist.
- Step 14: Etch off the Ti/Cu. It is ready for solder ball mounting.

The process steps for fabricating the RDLs for Fig. 6 with UBM-less Cu-pad are the same (from Step 1 through Step 7) as those for Fig. 5 with conventional UBM/Cu-pad, except Step 8 (same as Step 1) is for PI development as shown in Fig. 15. It is ready for solder ball mounting. Step 9 through Step 14 are not needed.

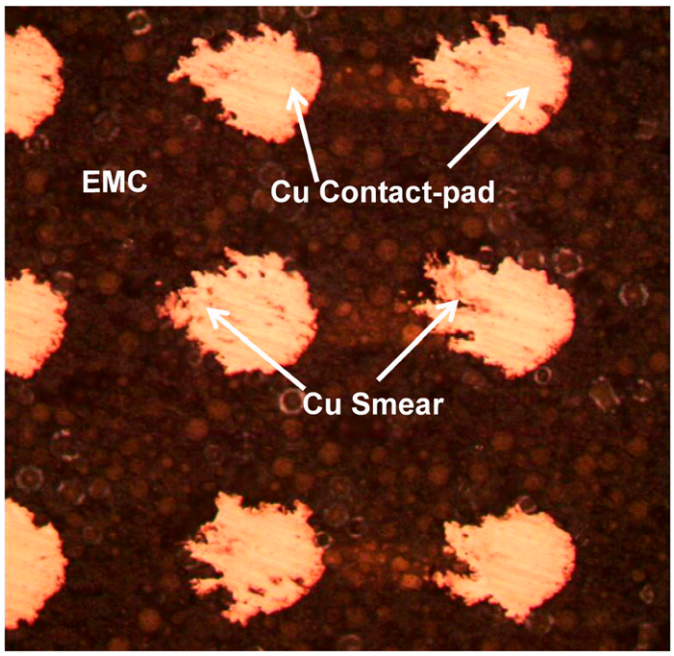

Fig. 11. Cu smear during backgrinding of the EMC.

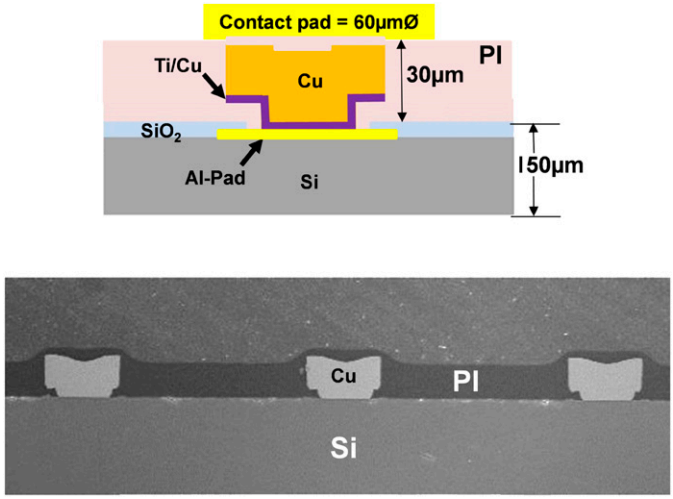

Fig. 12. Test chip with tall polymer (PI ~ 30 μm) to cover the Cu contact-pad and chip surface.

Based on the design, the RDL1 line width/spacing is 5 μm/5 μm. However, based on the top view and cross-sectional measurements, the actual fabricated line width/spacing is (on average) 4.68 μm/5.30 μm (Fig. 16). It can be seen that the line width is smaller than it should be, whereas the line spacing is larger than the design values. These errors could be due to (a) the small feature size of line width/spacing, (b) the photoresist opening, and (c) the seed layer (Ti) etching.

On the other hand, for RDL2, the fabricated line width/spacing is very close to the design values (10 μm/10 μm) as shown in Fig. 17. This could be due to the large design values of the line width/spacing.

E. Solder Ball Mounting

The key process steps of solder ball mounting are as follows:

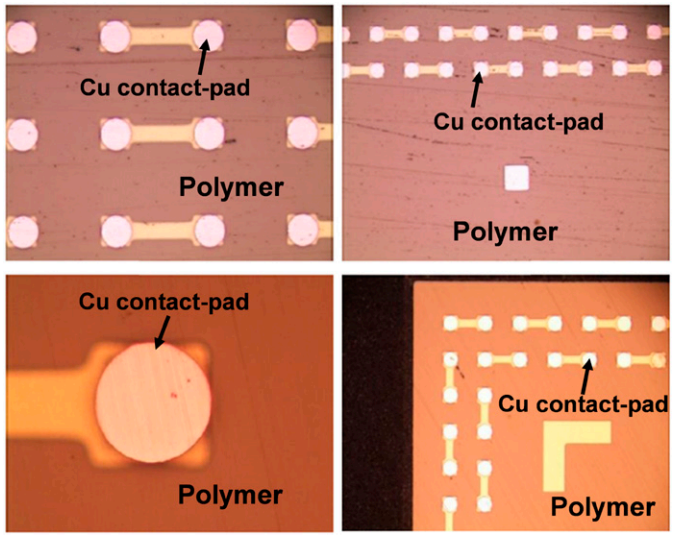

Fig. 13. After backgrinding the EMC to expose the Cu contact-pads (Cu revealing).

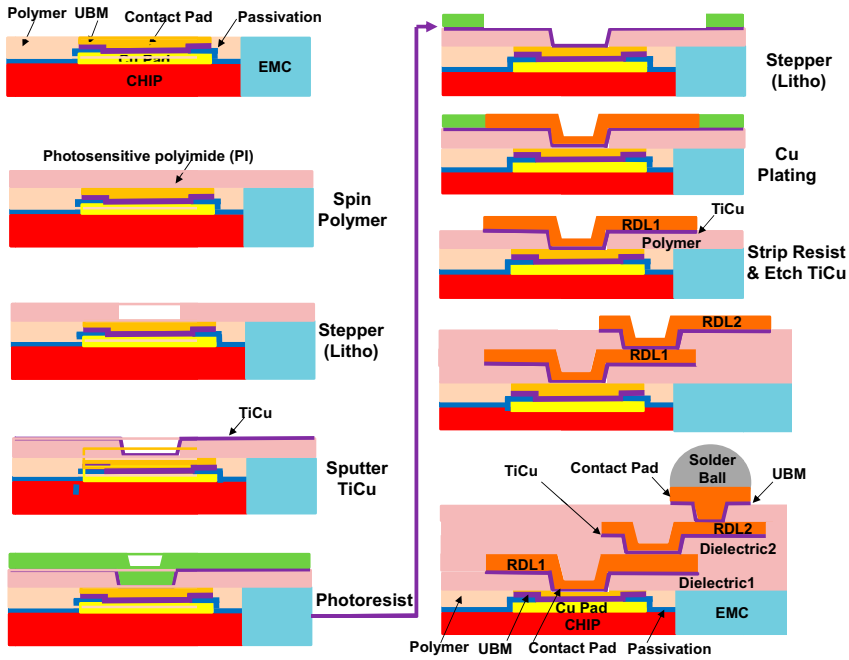

Fig. 14. Key process steps in fabricating the RDLs of FOWLP with conventional UBM/Cu-pad for solder ball.

Step 1: Load the reconstituted wafer to the chuck table.
Step 2: Alignment.
Step 3: Apply flux with the flux stencil.
Step 4: Alignment.
Step 5: Mount the solder ball with the ball stencil.
Step 6: Solder reflow.
Step 7: Clean the reconstituted wafer.

The solder (Sn3wt%Ag0.5wt%Cu) balls (200 μm diameter) used are from Indium. The peak temperature for solder reflow is 245°C. Fig. 18 shows the reflowed reconstituted wafer, individual package, and close-up view of solder balls on the package. A cross section of the FOWLP is shown in Fig. 19 for the UBM-less case (Fig. 6).

F. Debonding

The debonding of the glass carrier is by scanning a laser from the glass carrier side. When the LTHC layer "sees" the laser light, it converts into powders and the glass carrier is easily removed. It is followed by chemical cleaning. The DAF remains on the backside of the chip.

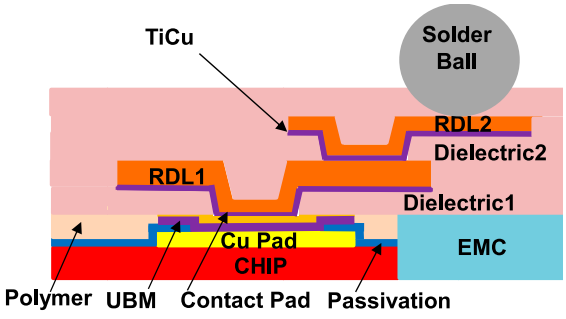

Fig. 15. RDLs with UBM-less/Cu-pad.

Conclusions

The feasibility of the design, materials, process, and fabrication of a test chip and test package by using the embedded FOWLP technology with the chip-first and die face-up method has been demonstrated in this study. Cross-sectional images of the test chip and package have been provided and discussed. Some important results and recommendations are summarized in the following.

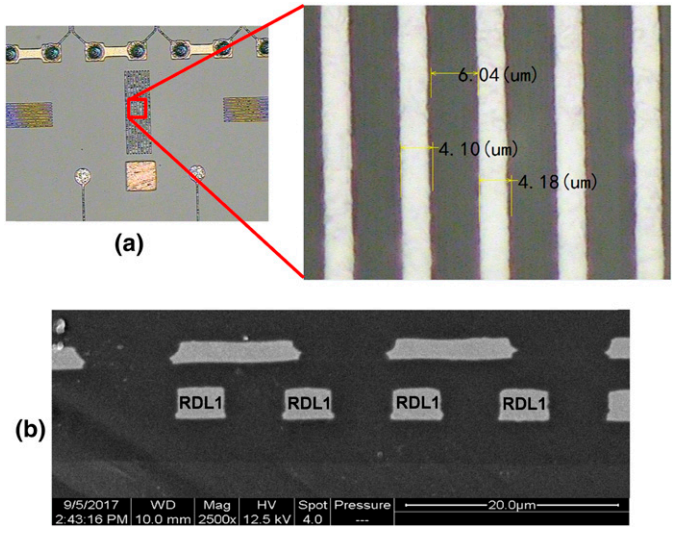

Fig. 16. Images of RDL1 (5 μm/5 μm line width/spacing). (a) Top view. (b) Cross-sectional view.

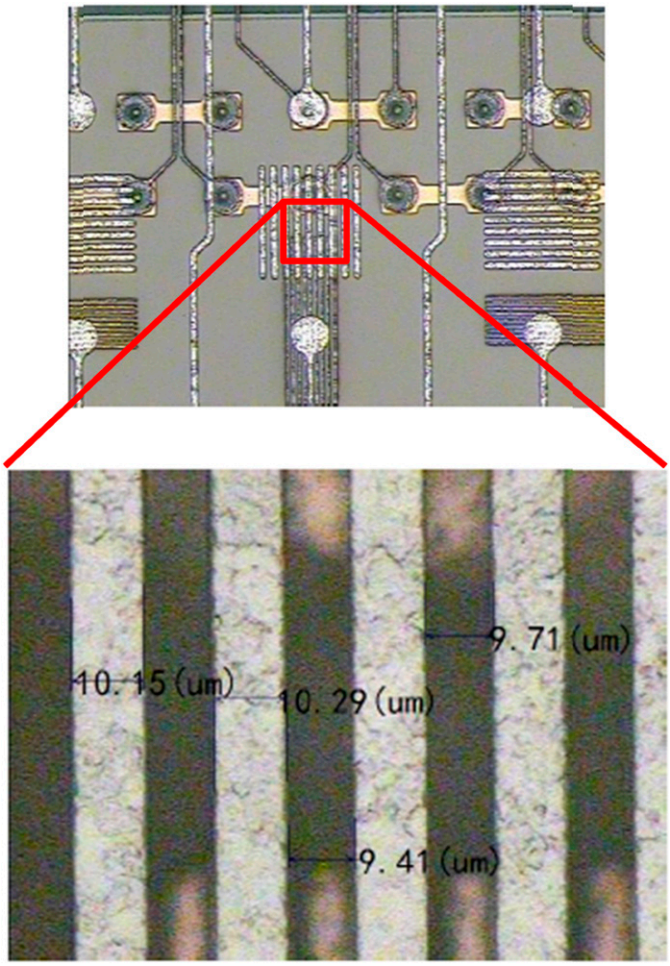

Fig. 17. Image of RDL2 (10 μm/10 μm line width/spacing).

- A test chip (10 mm × 10 mm × 150 μm) has been designed and fabricated. This chip has two staggered peripheral pads on a 150-μm pitch and central area-array pads on a 200 μm pitch. Every two pads are connected with a Cu trace. The cross section of the pads consists of the Si, Al, Ti/Cu, and Cu contact-pads (which is for building the RDLs of the test package).
- A PI is spun coat on top of the test chip wafer with two different kinds of thickness. One is 5 μm from the passivation and the other is 30 μm, just covering the Cu contact-pads.
- During Cu revealing (backgrinding of the EMC to expose the Cu contact-pads), there are Cu smears for the short (5 μm) PI and there no Cu smear for the tall (~30 μm) PI.
- A test package, 13.42 × 13.42 mm^2 (with a package/chip ratio = 1.8 and a chip-top EMC cap = 100 μm), has been designed and fabricated. These packages are on a 300-mm reconstituted glass carrier of 1 mm thickness and TEC = 7.6×10^{-6}/°C. The pick and place of the chips on the carrier is performed by using a high-precision bonder (NUCLEUS) and the compression molding of the EMC is carried out by using a high-coplanarity accuracy machine (ORCAS).
- This test package has three RDLs: the line width/spacing of the first RDL is 5 μm/5 μm, of the second RDL is 10 μm/10 μm, and of the third RDL is 15 μm/15 μm. The dielectric layer of the RDLs is fabricated by a photosensitive PI and the conductor layer of the RDLs is fabricated by ECD. Each two pads on the RDLs are connected with a Cu trace so as to provide a daisy-chain connection when the test package is connected to the test chip.

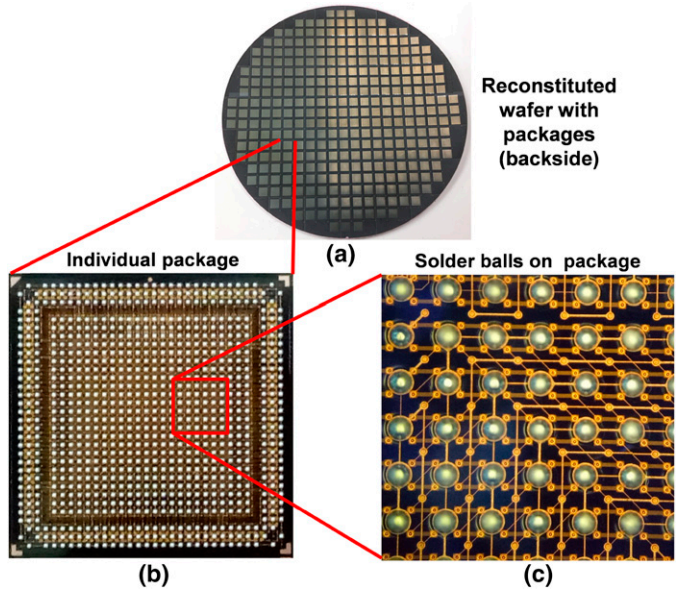

Fig. 18. (a) Images of the fabricated reconstituted wafer. (b) Individual package. (c) Close-up view of the solder balls.

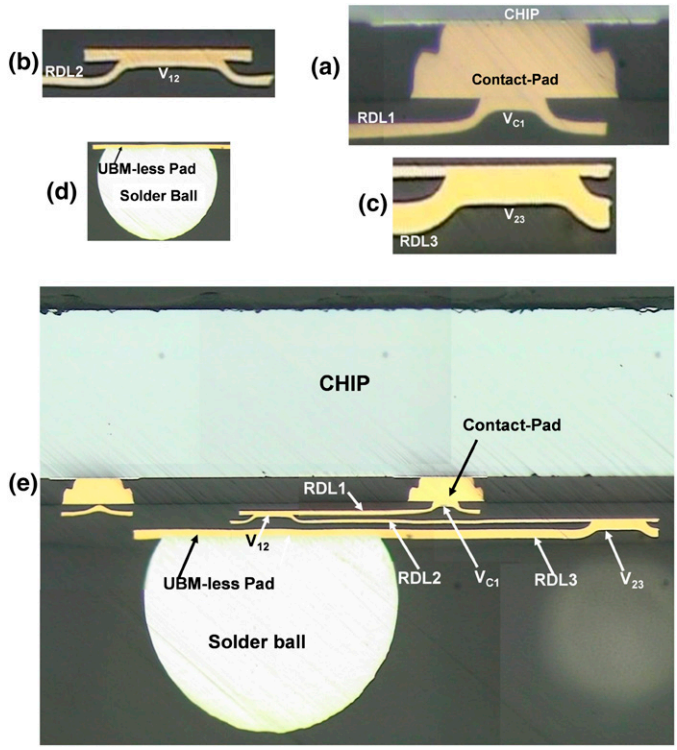

Fig. 19. Cross-sectional image of the assembled fan-out wafer-level package with three RDLs. (a) Chip, Vc_1, and RDL1. (b) V_{12} and RDL2. (c) V_{23} and RDL3. (d) RDL3, UBM-less pad, and solder ball. (e) A combination of (a–d).

- For RDL1, the fabricated line width/spacing (4.68 μm/5.30 μm) is not quite the designed value (5 μm/5 μm.) These errors could be due to (a) the small feature size of line width/spacing, (b) the photoresist opening, and (c) the seed layer (Ti) etching.
- For RDL2 and RDL3, respectively, the fabricated line width/spacing is very close to their designed values (10 μm/10 μm and 15 μm/15 μm, respectively).
- This test package has two different kinds of methods to connect the solder balls to PCB: one is the conventional (UBM/Cu-pad) method and the other is the less-process and lower cost (UBM-less and Cu-pad) method.

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