# Thermal Interface Materials and Cooling Technologies in Microelectronic Packaging—A Critical Review

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Abstract—The ever increasing demand for fast computing has led to heterogeneous integration of packages as can be seen in the latest Xeon family segments in the market. Microprocessors are now adjacent to memory chips, transceivers, field-programmable gate arrays, and even other microprocessors within a single substrate. These complex designs have instigated an increase in cooling demand for microprocessors, and hence, there has been an increased focus within the semiconductor industry on developing advance thermal solutions. From the packaging level, thermal interface materials (TIMs) play a key role in thermally connecting various components within the package and helps reduce the thermal resistance between the die surfaces and integrated heat spreaders. From the system level, cooling technology is critical to attain the desired overall thermal dissipation and performance. In this review, progress made in the area of TIMs and system cooling solutions are presented. The focus is on the evolution of TIMs and cooling technologies and their challenges in the integrated circuit packaging. Merits and demerits of various TIM materials available in the commercial market are also discussed. The article will be concluded with some directions for the future that would be potentially very beneficial.

Keywords—Adhesion, cooling solution, integrated heat spreader, microelectronic packaging, thermal interface material

#### Introduction

As the products in the microelectronics industry continue to get complex with increased feature and function integration using multichip packages (MCPs), the packaging technology faces new challenges with regard to thermal cooling [1-3]. In addition to that, with Moore's law, there is an increase in the core power density to increase microprocessor performance. Increase in speed and functionality of high performance microprocessors and application-specific integrated circuits results in increased inputs/outputs (I/Os) and power dissipation. The International Technology Roadmap for Semiconductors and the International Electronics Manufacturing Initiative predicts that the absolute power levels in microelectronic devices will continue to increase above and beyond 100 W depending on the application [4, 5]. Flip chip (FC) packaging technology is commonly

The manuscript was received on March 7, 2018; revision received on May 4, 2018; accepted on May 4, 2018

used to address the high I/O counts. This method exposes the backside of the semiconductor die for heat dissipation. A high thermal conductivity integrated heat spreader (IHS) or lid significantly larger than the Si die is typically attached to the back of the die along with a thermal interface material (TIM<sub>1</sub>) dispensed or placed between the die and heat spreader [6-10]. The next level cooling hardware used is typically a finned heat sink sandwiched to the IHS using TIM<sub>2</sub> as shown in Fig. 1. With the continual increase in cooling demand for microprocessors, there has been an increased focus within the microelectronics industry on developing thermal solutions [11-17].

The main function of the IHS or lid in a FC packaging is to spread and dissipate the heat generated in the microprocessor [17]. The quantitative method of measuring this performance is by means of a resistance value known as resistance junction to case ( $R_{\rm jc}$ ), and it is the sum of individual thermal resistance across all interfaces and materials in the IHS stack as shown in Fig. 2 [18]. TIM<sub>1</sub> conducts the die heat to the heat spreader to control the junction temperature ( $T_{\rm j}$ ), enabling higher product performance and superior reliability.  $R_{\rm jc}$ , is calculated using eq. (1) as follows:

$$R_{\rm ic} = (T_{\rm i} - T_{\rm c}) / \text{TDP} \times A_{\rm die}, \tag{1}$$

where  $T_{\rm j}$  is the maximum junction temperature,  $T_{\rm c}$  is the case or IHS temperature, TDP is the thermal demand power applied on the semiconductor chip, and  $A_{\rm die}$  is the active area of the semiconductor chip. Equation (1) can also be rewritten as

$$R_{\rm jc} = \left(\Psi_{\rm jc}\right)_{\rm uniform\,power} \times A_{\rm die}.$$
 (2)

Thermal impedance in a package  $R_{\rm jc}$  is defined as the package thermal resistance under uniform heat dissipation times the area of the die  $A_{\rm die}$ . Nonuniformity in heat dissipation has a large impact on the junction temperature and, therefore, TDP. Nonuniformity causes increase in the package thermal resistance as represented by the following equations:

$$\Psi_{\rm jc} = \left(T_{\rm j} - T_{\rm c}\right) / \rm TDP, \tag{3}$$

$$\Psi_{\rm ca} = (T_{\rm c} - T_{\rm a})/{\rm TDP},\tag{4}$$

$$\Psi_{jc} + \Psi_{ca} = \Psi_{ja} = (T_j - T_a)/TDP, \qquad (5)$$

where  $T_{\rm a}$  is the ambient temperature,  $\Psi_{\rm jc}$  is the package thermal resistance,  $\Psi_{\rm ca}$  is the system thermal resistance, and  $\Psi_{\rm ja}$  is the overall thermal resistance.

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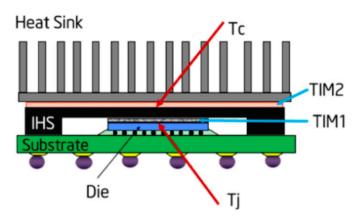


Fig. 1. Cross section schematics of an integrated circuit FC package.

The thermal efficiency and reliability of TIM<sub>1</sub> and TIM<sub>2</sub> define the performance of a microelectronic package and its long lasting characteristics depend a lot on the interfacial adhesion between the layers [19, 20]. In this review, focus will be on the thermal management of integrated circuit packaging. The review is divided into two sections excluding the Introduction. Thermal interface materials provide a comprehensive review of the package-level thermals which includes the TIM and its evolution. System-level cooling solutions will provide an overview of the system-level thermals consisting of cooling solutions and its role on thermal dissipation.

### THERMAL INTERFACE MATERIALS

#### A. Polymer-Based Thermal Interface Materials

Polymer thermal interface material (PTIM) technologies developed to date can be divided into several classes of materials by their characteristics, including pads, adhesives, phase change materials (PCM), greases, and gels [21-30]. Each class has their own benefits and drawbacks which are discussed in the following text and summarized in Table I.

Elastomer thermal pads, which are also known as gap-filler pads, are used to improve heat dissipation across large gaps, by establishing a conductive heat transfer path between the mating surfaces. Thermal pads are typically  $200-1,000 \mu m$  thick and are

popular for cooling multiple low-power devices, such as chipsets and mobile processors. A manual or automatic pick and place process is used to apply elastomer thermal pads in high-volume manufacturing. The pad consists of an elastomer comprising filler materials ranging from ceramics to boron nitride (BN) with various thermal performances. Metal particles are seldom used because of the risk of electrical shorts. For this application, the pads must be compliant and compressible to ensure that the pads can absorb the variation of gap heights and assembly tolerance. The tradeoff is that increasing filler loading for the purpose of increasing thermal conductivity results in hardening the pad which reduces compliance and increases contact thermal resistance. The thermal performance of elastomeric pads highly depends on the contact pressure at the mated surfaces. Typical failure mechanisms are increased thermal resistance due to inadequate pressure or loss of contact at one or more surfaces. Nevertheless, the advantages and disadvantages discussed previously determine that elastomer thermal pads are most suitable for relatively lowpower devices.

The mainstream thermal adhesives are metal-filled epoxies. They are highly conductive adhesive materials that thermally cure into highly crosslinked materials. High-end epoxy thermal adhesives can achieve bulk thermal conductivities of 10-20 W/mK. Because it is in a low viscosity paste form before curing, the thermal adhesive is able to wet the mating surface well and form a low-contact resistance interface. Once cured, the epoxy thermal adhesives transition into a thermoset plastic with the tensile modulus in the magnitude of giga Pascals. The high-modulus nature of cured-epoxy thermal adhesives prevents pump-out failure mechanism (to be discussed in the grease section); however, it increases the thermal-mechanical induced package stress significantly compared with other classes of TIMs, which leads to higher delamination or die crack risk. As a result, metal filled epoxies are almost exclusively used in lower package stress application such as die attach and package reliability with metal filled epoxies as die attach adhesive is highly sensitive to die size.

Phase change materials are a class of materials that undergo transition from a solid to a liquid phase when subject to heat. These materials are in a solid state at room temperature and are in a viscous liquid state at device operating temperatures. When

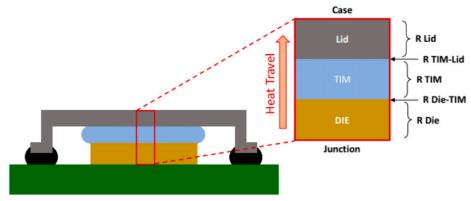


Fig. 2. Illustration of the resistance path of an integrated circuit FC package at the TIM<sub>1</sub> package level.

Table I Summary of PTIM

Class [with thermal resistance (°C cm²/W)] [61]	Typical composition	Benefit	Drawback
Pad (>.2)	Ceramic filler (Al <sub>2</sub> O <sub>3</sub> , BN, etc.), cured silicone, and polyurethane elastomer	Easy to handle/apply, conforms to die gap height variation for a MCP package	Very high contact resistance, usually requires high pressure during application
Adhesive (~.051)	Ag filler and epoxy resin	High thermal conductivity, wets surface before cure, and doesn't pump-out	Need curing process, high delamination risk in high stress application
Phase change material (~.13)	Ceramic filler (Al <sub>2</sub> O <sub>3</sub> , BN, etc.), polyolefin/wax, and acrylic/ polyolefin resin	Wets surface after phase change, no curing is needed, low delamination risk, and has self-healing properties	Low thermal conductivity
Grease (~.12)	Metal/Ceramic filler (Al, Al <sub>2</sub> O <sub>3</sub> , ZnO, etc.) and silicone oil	High thermal conductivity, wets surface, no curing is needed, low delamination risk, and is low cost	Has potential pump-out risk, can dry out, potential filler/oil separation risk
Gel (~.081)	Metal/Ceramic filler (Al, Al <sub>2</sub> O <sub>3</sub> , ZnO, etc.) and curable silicone oil	High thermal conductivity, wets surface before curing, and has low pump-out and delamination risk	Need curing process and is challenging to balance its mechanical property

in the liquid state, PCMs readily conform to surface irregularity and provide low thermal interfacial resistance. Because the phase change in PCM is an endothermic transition, PCMs with enough mass could effectively delay sharp device temperature rise, which makes PCM ideal for mobile devices typically working in burst mode. PCMs offer ease of handling and processing because of their availability in a film form and the lack of post dispense processing (e.g., no cure). Some manufacturers offer dispensable or printable PCMs in paste form as well, which usually require a less desirable bake step to drive out solvents before attaching the lid or heat sink. From a formulation perspective, the resin and filler combinations that have been used in PCMs limit their capability to achieve high bulk thermal conductivities (>10 W/mK).

Thermal greases are typically mixtures of incurable silicone oils and fillers. Silicone oil is a polydimethylsiloxane polymer with low to medium molecular weight that is unable to crosslink. Fillers mainly comprise a mixture of metal fillers (Al, etc.) and ceramic fillers (Al<sub>2</sub>O<sub>3</sub>, ZnO, etc.). Thermal greases as a class of materials offer several advantages including good wetting to the mating surfaces, easy to dispense, no thermal curing, low cost, and able to achieve high bulk thermal conductivity compared with other classes of materials. Although thermal greases could provide excellent end-of-line thermal performance, they suffer from degradation of thermal performance during temperature cycling testing. Extensive analyses of the failure mechanism showed that, under the cyclical stresses encountered during temperature cycling, greases migrate out from between the interfaces by a phenomenon known as "pump-out" as shown in Fig. 3 [31]. The extensive thermo-mechanical stresses exerted at the interface during temperature cycling are due to package warpage movement under the lid when the temperature changes. Because the pump-out phenomenon is inherent to the noncuring nature of thermal greases dictated by the used formulation chemistry, all typical greases are subject to pump-out. The advantages of thermal greases make them widely adopted in TIM<sub>2</sub> application, but its reliability disadvantage greatly limits its usage in TIM<sub>1</sub> application.

Thermal gel materials were developed for overcoming the drawback of pump-out in thermal greases by replacing the silicone oil in thermal grease with a cross linkable silicone resin.

Before curing, thermal gels behave similarly to thermal greases, and thermal curing is performed after lid attachment. Therefore, thermal gels could provide good contact resistance by excellent wetting to mating surfaces and resist pump-out failure during reliability testing because of stronger mechanical integrity resulting from crosslinking. Two types of crosslinking mechanisms are typically found in silicone thermal gels: free radical chemistry and hydrosilylation chemistry. Free radical chemistry involves silicone polymers with vinyl groups as crosslinking sites and free radical catalysts (peroxides, etc.). In hydrosilylation chemistry, silicone polymers with vinyl groups function as base polymers, whereas silicone polymers with Si-H groups function as cross linkers and platinum containing catalysts, such as Karstedt catalyst, function as polymerization catalysts. Both chemistries need heat to trigger the polymerization and inhibitors are usually added into the formulation to control curing onset temperature for shelf life consideration. Hydrosilylation chemistry is more advanced and preferred to free radical chemistry because of many advantages. First, hydrosilylation chemistry is semiquantitative or even quantitative chemistry, therefore it provides more control to the degree of crosslinking compared with free radical chemistry. Second, hydrosilylation chemistry generates much less volatiles than free radical chemistry does, which greatly reduces voiding risk in TIM. Because it combines the benefit of thermal greases and the benefit of cured material, thermal gels are the dominant polymeric TIM<sub>1</sub> for high-end devices such as personal computers and server centeral processing units. Formulation of successful thermal gels is complicated as it requires delicate balance of their mechanical properties. Storage shear modulus G' and its relation to loss shear modulus G" were found to be a critical parameter for thermal performance of thermal gels [32, 33] because they reflect the degree of crosslinking inside a cured thermal gel material [34]. High G' and high G'/G" lead to higher contact resistance and higher delamination risk, whereas low G' and low G'/G" lead to higher pump-out risk as shown in Fig. 4. The optimal G' and G'/G" of thermal gels also show dependence on package warpage behavior. Manufacturing highquality thermal gels is a nontrivial task as well because the mechanical properties of cured thermal gels are highly sensitive to the stoichiometry of vinyl groups and Si-H groups, which in



Fig. 3. Images of thermal greases after temperature cycling and disassembly of the package. The image on the left shows evidence of pump-out, whereas the image on the right shows no evidence of pump-out (adapted from [31]).

this case both exist in the form of polymers where dispersity is expected to be significant. Only a limited number of suppliers with strong technical and manufacturing competency are able to provide thermal gels with consistent performance. This contributes to the fact that thermal gels usually demand higher price than thermal greases that cannot be supported solely by raw material cost difference.

#### B. Solder Based Thermal Interface Materials

Because of the necessity for improved device and system performance, materials with higher bulk thermal conductivity and lower interfacial resistance in spite of high cost are required while maintaining low package stress and low processing temperature. One approach to improving the thermal conductivity of TIMs is to use materials that transfer heat by conduction rather than percolation. Percolation, used widely in electrical engineering, is a phenomenon that refers to a completely random distribution of a material with high thermal conductivity in a matrix of low conductivity medium. It is the passage of an influence through an irregularly structured medium where the influence can pass through some regions more easily than others

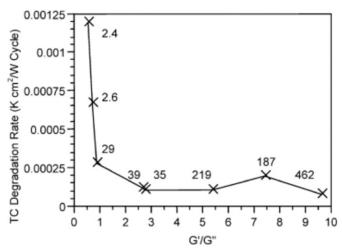


Fig. 4. Correlation of modulus with degradation rate of gel TIMs in temperature cycling. The numbers are value of G' for each data point (adapted from [331))

and in some regions not at all [35, 36]. Solders are examples of such a material. Solders with high liquidus temperatures have historically been used to remove heat from some power supply modules [37]. To achieve good wetting and bonding, the solder is typically heated higher than its liquidus temperature for bonding; therefore, the liquidus temperature of the solder is an important parameter for processing. To be useful for microelectronic devices, solders with melting points higher than the operating temperature (about 90°C) yet lower than the maximum processing temperature (about 260°C) are required. Table II presents the thermal conductivities and liquidus temperatures of a variety of solders. Solders are available with thermal conductivities ranging from 19 to 86 W/mK, which is significantly higher thermal conductivity than the best polymeric TIMs. The major technical challenges of integrating solder based TIMs are poor wetting of the Si surface on bare die and high package stress due to high modulus.

Pure indium stands out from solder material candidates because of several highlights in its properties. First, pure indium has the highest thermal conductivity of 86 W/mK. Second, its melting point of 157°C falls into the middle of the process window. Third, indium is the softest metal with the lowest yield stress of 2.5 MPa. Therefore, despite its 10 GPa modulus, indium experiences plastic strain and conforms to package warpage behavior without causing high package stress. Deppisch et al. [38, 39] performed an in-depth investigation into the challenges and solution paths of applying indium as a TIM<sub>1</sub> material. Great effort was spent toward optimizing the surface finish of die backside metallization and the lid surface to provide good wetting and a robust joint. A schematic of the indium TIM microstructural development pre- and post-assembly is shown in Fig. 5. Excessively thick gold layers are not preferred because of the brittle nature of In-Au intermetallic compounds and cost consideration. A very thin gold layer is not practical because of the limitation of the gold plating process on the lid. A lower indium preform thickness is preferred for better thermal performance, whereas higher indium preform thickness can survive the temperature cycle reliability testing better. Optimizations of indium flux dispense and reflow profiles is equally critical to successful application, as they directly affect post assembly voiding and, thus, thermal performance. Based on the previous discussion, it is evident that the implementation of indium as TIM<sub>1</sub> needs extensive engineering.

Solder	Liquidus (°C)	Solidus (°C)	Bulk thermal conductivity (W/mK)	Tensile yield stress (MPa)
48Sn52In	118	118	34	13
42Sn58Bi	139	139	19	49
100In	157	157	86	2.5
63Sn37Pb	183	183	50	27
100Sn	232	232	73	30

Table II Properties of Various Solder Based TIM Candidates

#### C. Advanced Thermal Interface Materials

#### 1) THERMAL PADS BASED ON ALIGNED GRAPHITE TECHNOLOGY

There has been on-going interest in using graphite as filler in TIM. Graphite has >300 W/mK in-plane thermal conductivity; however, its out-of-plane thermal conductivity is very poor. Simply mixing graphite with other components of TIM results in random orientation of graphite fillers, leading to limited gain in thermal performance. Recently, thermal pads have been developed by Hitachi Chemical with prealigned graphite filler [40]. Controlled orientation of graphite fillers is achieved by extruding graphite fillers with a matrix material such as acrylics and polybutadienes. The highly thermally conductive x-y plane of graphite fillers is oriented in the thickness direction of the thermal pads as shown in Fig. 6, which provides efficient heat transfer in the thickness direction through the thermal pad. The typical thermal conductivity these thermal pads can achieve is >20 W/mK in the thickness direction at a reasonable pressure of 20 psi or higher.

Thermal pads with aligned graphite fillers excel in thermal conductivity; however, they usually lack in contact thermal resistance compared with thermal greases and gels. Two approaches are typically applied to improve their contact thermal

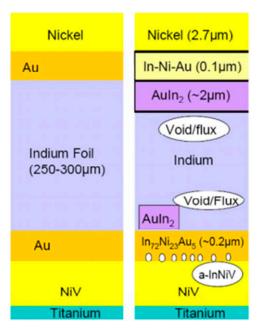


Fig. 5. Pre- and postassembly microstructures of indium TIM and interfaces with die and lid (adapted from [38]).

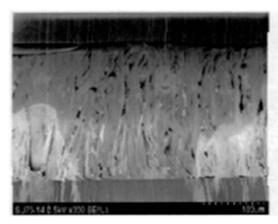
resistance: increasing application pressure and improving material compressibility. The quality of the interface and, thus, contact thermal resistance is highly sensitive to pressure for thermal pads with aligned graphite fillers. As a result, minimum pressure is required to achieve expected thermal performance. Making the material more compressible helps improve contact thermal resistance, because a more compressible material will better conform to surface irregularities under the same pressure. Increasing compressibility is helpful for gap pad application as it can better absorb die or component height variation.

Lots of effort has been spent in improving the reliability of thermal pads with aligned graphite fillers. The graphite fillers are more resilient to environmental stress (temperature cycling, bake, humidity, etc.) than the matrix is. These thermal pads are susceptible to humidity and bake conditions, caused by significant degradation in contact thermal resistance. In addition, the polybutadiene or polyacrylate in the matrix is susceptible to heat and humidity and leads to hardening of thermal pad, which is one major root cause for higher contact thermal resistance. Replacing polybutadiene or polyacrylate with a soft elastomer addresses some reliability problems.

#### SINTERING TECHNOLOGY

The idea of using metal nanoparticle sintering to achieve high thermal conductivity has been applied in epoxy thermal adhesives for die attach paste application [41-43]. The sintering of Ag nanoparticles forms a metallic network connecting the die and metal lead frame, providing an efficient thermal dissipation pathway in die attach application as shown in Fig. 7. Die attach paste with Ag nanoparticles can sinter at as low as 160°C, which provides a friendly process window. Because Ag nanoparticles could aggregate and form initial sintering at even room temperature, an organic dispersant is needed on the surface of the metal nanoparticles for stabilization and this dispersant decomposes at 160°C to promote sintering as shown in Fig. 8. Solvents and epoxy resins are also included in the formulation for dispense/print performance and reliability consideration. Gold or silver plating is usually required on the die and substrate sides for better thermal performance and adhesion. After the sintering of the die attach paste, a continuous metal layer is formed between the die and substrate, providing thermal conductivity in the scale of 100 W/mK.

Several challenges exist when extending sintering technology from die attach paste into TIM<sub>1</sub> application. First, die attach paste with epoxy resin and sintering fillers typically has modulus in the GPa range after sintering or curing. Although it can sufficiently manage the thermal-mechanical stress during a reliability test of a small size die in die attach application, it is too





Graphite fillers aligned in z-direction in organic matrix

Fig. 6. Graphite orientation inside thermal pads (adapted from [40]).

high for relatively large die size in TIM<sub>1</sub> application. Second, silicone resin may provide a path to lower modulus for better stress management; however, the Ag nanoparticles can poison the catalyst in silicone resin resulting in incurable material. Curing of the epoxy or silicone polymer in matrix could inhibit the sintering of Ag nanoparticles if the timing of curing and sintering is not carefully controlled. Although a higher degree of sintering provides higher thermal conductivity, it also increases the modulus and delamination risks. Successful formulation of TIM<sub>1</sub> based on sintering technology needs to address the aforementioned challenges.

#### System-Level Cooling Solutions

As we continue to evolve in a data consumer society, the amount of data generated increases exponentially as shown in Fig. 9, generating a higher demand for computing power at the local level, e.g., cell-phones, laptops, and internet of things devices, to the global level, e.g., server farms, cloud storage systems and data mining facilities. As the data storing, transference, and processing increases, there is a higher need for cooling the electronic equipment that powers them. In the previous sections, we described the package-level thermal cooling solutions. In this section, we will provide a general

overview of the most common system-level cooling solutions and new alternatives.

The thermal performance of a system is determined by the package and the external system-level cooling solutions used as shown in Table III. When a package requirement is defined, it has to be weighed against the external cooling solution requirement, i.e., it has to be co-designed [44-46]. It is of no use if the package has a negligible thermal resistance if the external cooling solution cannot properly dissipate the heat generated by the device and vice versa. When selecting and/or developing an external cooling solution, several factors must be taken into account: maximum heat dissipation, geometrical/physical constrains, cost, power consumption, noise, reliability, and additional/incremental risks because of specific solution vs required application.

One of the first factors to be considered during system-level cooling solution development is the minimum and maximum heat dissipation required for the system. In many systems, the amount of heat that needs to be removed from the active devices is so large that it limits the possible heat dissipation solutions that can be used to only the high-end options, e.g., liquid cooling. In general, the heat dissipation requirement has increased through time, as shown in Fig. 10. Furthermore, different segments might impose different geometrical constrains,

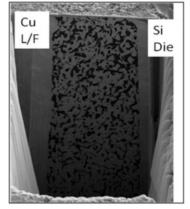


Fig. 7. Focused ion beam cut reveals Ag network connecting die and Cu lead frame formed by sintering of Ag nanoparticles in die attach paste (adapted from [42]).

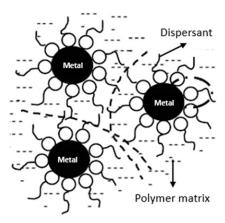


Fig. 8. Schematic illustration of key components inside epoxy die attach thermal adhesives with sinterable metal nanoparticles.

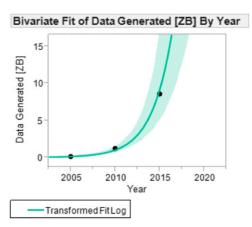


Fig. 9. Data generation trend (adapted from [44]).

e.g., the space available for heat dissipation in mobile devices is considerably smaller than the space available for desktop or server systems. In the case of servers, there might be additional physical constrains provided by the office space and racks [46]. After considering the heat dissipation required by the system, the next set of considerations is economic and environmental. One of the main challenges typically associated with the semiconductor industry is the disposal of toxic waste which is harmful to human life and stands as a road block to a green environment [47-51]. Given a certain heat dissipation reguirement, the obvious choice would be to select the cheapest solution (considering both the equipment investment and the electrical cost of running the cooling system) that can deliver the desired performance while satisfying the local environmental and human regulations, e.g., noise safety level requirements in server farms and safety of liquids used for immersion cooling.

Each market segment and application can drive a considerably different set of requirements, and careful consideration of the specific boundary conditions must be given by the thermal engineer. Although a specific thermal solution might be well suited for a specific application, it might not fare well in a different environment from a technical or human perspective. For instance, thermal solutions used in similar size ball grid array and land grid array (LGA) packages are not necessarily interchangeable because of the load requirements and the associated limitation needed for proper electrical contact of the LGA vs the load required for ball reliability. Human factors must also be considered. For instance, to cool and insulate high power electronics used in transformers it was common to immerse them in polychlorinated biphenyls, a recently banned liquid because of its toxicity, a practice that would be

unacceptable nowadays for cooling servers that need to be constantly swapped and repaired by human personnel. In the next section, current solutions for system-level thermal dissipation are described in terms of their maximum heat dissipation, geometrical/physical constrains, cost, power consumption, noise, and reliability.

#### A. Air Cooling

Air cooling (with conduction cooling between the package and the heat sink) is the most common external cooling solution nowadays. It is implemented by simply attaching an air cooled heat sink to the package mechanically with an intermediate layer of TIM<sub>2</sub>, between the package and the heat sink. The TIM between the package and the heat sink has the purpose of minimizing the interface thermal resistance between the package and the heat sink. The heat sink is typically a plated copper body with several fins on top. Several options for fin length and density are available depending on the specific application and space available in the system. In addition to the heat sink, a fan is typically added on top of the heat sink to change the system from natural convection cooling to forced convection cooling. The fan is added to improve the flow of air on top of the heat sink and reduce the air thermal boundary layer thickness that is proportional to the air thermal resistance.

Because of the use of air as a medium to conduct heat away from the system, the system is typically economic to implement but is limited by the capacity of air to conduct heat. The thermal conductivity of air is 0.1 to 0.01 times lower than the thermal conductivity of the materials in the package and, hence, the air thermal resistance can easily become the limiting resistance in the overall system thermal stack-up. To minimize the impact of thermal resistance, adequate airflow must be provided by the fan, e.g., high performance graphic cards use multiple fans to increase the airflow to the processor. In addition, because the effectivity of air cooling is directly proportional to the environmental air temperature, room temperature control might be required to ensure optimum system performance.

Additional requirements might be needed to operate air-based cooling systems depending on specific applications. In situations where a large number of systems are run together, e.g., a server farm or cryptocurrency mining center, additional considerations might be needed to ensure reliable operation such as air filtration, humidity control, and environmental temperature regulation. The additional considerations would add to the cost of running the system, but air cooling is still overall a cheaper technology than any other current alternative. The use of fans to generate forced convection has the side effect of generating noise while the fan is cooling, which gets worse as

Table III
Description of System-Level Cooling Solutions

System-level cooling	Physical constrains	Additional reliability concerns	System cost
Air cooling	Need volume immediately on top of the lid	No additional (reference solution) Reliable self-contained liquid circuit needed Possible interaction between coolant and devices Possible interaction between vapor and devices. Not demonstrated in any commercial devices	Low
Water cooling	Additional liquid pump needed		Medium
Immersion cooling	Requires colling tanks		High
Evaporative cooling	Requires vapor collection		Not Available

the power dissipation requirement grows because a higher fan speed, hence the higher noise, is required for improved thermal performance. The consequences of fan noise could range from diminished user experience, for laptops and gaming centers, to potential health concerns in the case of server farms.

#### B. Liquid Cooling

Liquid cooling is currently used mainly on systems that require high thermal dissipation. It is normally implemented by mechanically attaching a water cooled heat sink on top of the package. Just as in air cooling, in the most common implementation a TIM is placed between the package and the heat sink to minimize the interface thermal resistance between the package and the heat sink. Instead of fins, the liquid cooling heat sink has a series of micro channels that serpentine within. Cold liquid is injected from an inlet port. As the liquid travels through the micro channels it warms up, removing heat from the device. Finally, the warm liquid exits the device through an exit port to be cooled by an external refrigeration unit. Typically, the same liquid is reused through the system, forming a cooling cycle.

The liquid cooling system design can be modified in different ways that can improve the thermal dissipation performance but typically have side effects such as increasing the manufacturing complexity, and hence the cost, or reducing system reliability. An example of such modifications is the proposal of micro machining cooling channels within the silicon itself to reduce the thermal path between the active silicon and the liquid that carries the heat away. Although this proposal can indeed reduce

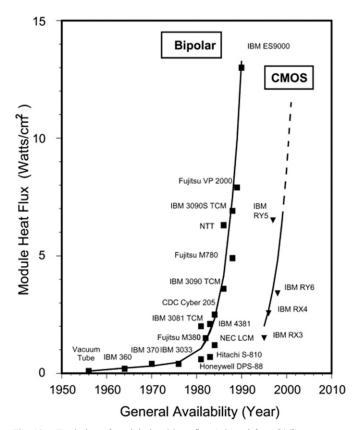


Fig. 10. Evolution of module-level heat flux (adapted from [46]).

the thermal path and minimize device thermal performance, the manufacturing of micro channels embedded in the silicon increases the manufacturing complexity, increases the likelihood of stress concentration points in the silicon that can potentially result in cracks, and can expose the silicon and copper layers to unknown chemical interactions. Currently, the bulk of the liquid cooling systems does not include embedded micro channels due to the additional risks and constrains imposed by their implementation.

Because of the use of liquid as a medium to conduct heat away from the system, the liquid cooled systems can handle higher heat dissipation rates than the air based systems. There exist different implementations of the system depending on the physical mechanism for heat removal along the microchannel. If the liquid suffers a phase change, it is known as a phase change or two-phase liquid cooling system; otherwise, it is a single phase cooling system. The maximum heat dissipation rate depends on the system being a single or two-phase heat dissipation system, as shown in Fig. 11 [46, 52]. Two-phase systems can handle higher dissipation rates than single dissipation systems at the same mass flow rate because of the higher enthalpy change during the coolant phase transition, but they have drawbacks too. In two-phase systems maximum heat removal happens only along the microchannel zones where phase change happens actively; once the flow is mainly a gas and the phase change rate decreases, the heat dissipation rate drops drastically which can produce local and system-level instabilities in the heat flow

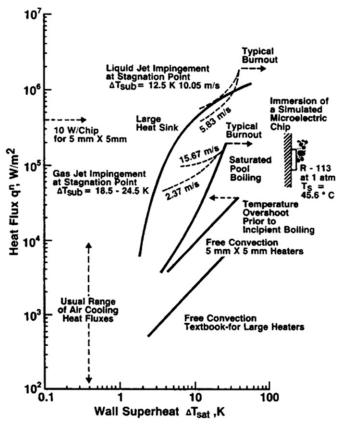


Fig. 11. Heat flux ranges for direct liquid immersion cooling (adapted from [46, 52]).

rates. Furthermore, air droplets can generate a heavily irregular flow rate which would impact the consistency of the heat removal process. Finally, the creation of gas droplets in the microchannel opens the possibility of droplet collapse and cavitation; which can decrease the expected life of the heat sink.

Thermal conductivity of liquids is about 10 to 100 times higher than the thermal conductivity of air. Hence, even in single phase cooling devices, heat dissipation in liquid cooling systems can be higher than that in air cooled systems. Furthermore, liquid cooling allows for 3× denser chip packaging, which would be an important consideration in assisted driving systems and military applications that require equipment mobility. Despite this initial advantage, cooling systems are more complex than air cooling systems because of the need of a liquid pump to move the fluid throw the system. Furthermore, final customers might prefer air based systems because of the higher price of liquid cooling systems, the incremental complexity of dealing with a liquid and electronics, and the possibility of liquid interaction with other system parts (regardless of the risk being justified or not).

As the thermal dissipation demands increases because of the ever growing need for high-speed and high processing power devices, new technologies are being developed to satisfy this demand, aket and package land side, is immersed in a dielectric liquid that is recirculated in a water bath as shown in Fig. 12. Typically, as the immersion liquid is recirculated, it is also cooled to keep the liquid bath temperature. Immersion cooling offers an improvement on heat dissipation capability versus air cooled systems because of the higher thermal capacity of immersion fluids and higher mass flow rate in the immersions tanks.

The liquids used in immersion cooling have significantly improved from the early days of high power electronics. The use of toxic substances such as polychlorinated biphenyls has been progressively banned since the 70's in power electronics. Nowadays, Fluorinated liquids with low chemical interactions are typically used. In addition, to reduce the risk of health issues, low reaction liquids are used to reduce all the potential chemical interactions between the immersion liquid and the materials in the package, board, board passive components, socket, and heat sink. Despite the improvements offered by fluorinated liquids, the use of mineral oil for immersion cooling continues being popular among enthusiasts because of its comparatively low price. Although mineral oils offer a significant reduction in the cost per liter, the mineral oil can have interactions with the

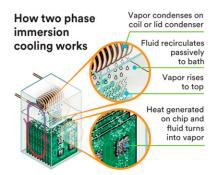


Fig. 12. Example of a two-phase immersion cooling setup (adapted from [53]). Fig. 13. Typical direct liquid-jet cooling performance (adapted from [46]).

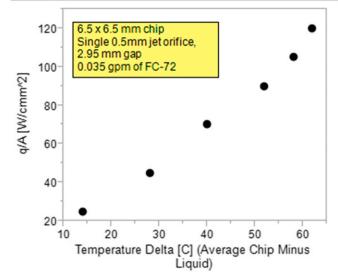
elastomeric materials in the package and careful consideration must be taken when using it. In either case, typically only air cooling is tested by large system manufacturers and immersion cooling is not an option recommended because of the possible unknown interactions between the immersion liquid and the system materials.

In general, the efficiency of immersion cooling will depend on the thermo-physical properties of the liquids used and the heat transfer mechanism: natural convection, forced convection, or boiling as described by Chu et al. [46]. As a consequence, immersion cooling can result in a wide range of thermal resistances depending on the flow velocity and heat transfer mechanism [53]. For fluorinated liquids, the thermal resistance can vary as much as two to three orders of magnitude just from impingement velocity during forced flow, e.g., for FC-77 it can range from ~0.5 to ~50 C/W [54]. The thermal performance using a direct liquid jet cooling is illustrated in Fig. 13.

#### C. New Cooling Techniques

Evaporative cooling is a new solution proposed to carry heat away in a fast fashion between the devices. In evaporative cooling, the liquid in contact with the device is constantly being evaporated to cool the device; as the liquid is evaporated, a constant flow of liquid on top of the device replaces the evaporated mass. Several proposals on how to implement such system exist, including surface tension driven flow to replace the liquid used and localized microfluidic channels to feed liquid into the system [55, 56]. Because of the higher enthalpy change required for phase transition of most liquids, this option can potentially result in high dissipation flow rates but because of potential bubble formation and cavitation, high thermal resistance points can be generated too. Although the proposal of evaporative cooling as a high dissipation solution is feasible, several package- and system-level interactions must be addressed beforehand. For instance, the gas byproducts of the evaporation

## Bivariate Fit of q/A [W/cmm^2] By Temperature Delta [C] (Average Chip Minus Liquid)



should be collected and condensed to have a fully enclosed and contained system. Alternatively, if the gasses are not collected, the environmental interactions must be considered, because even in the case of water, a low health risk fluid, it can interact with electronics reducing its expected lifetime.

#### SUMMARY AND SUGGESTIONS FOR FUTURE WORK

Evolution of the microprocessor is clearly the face of the computing revolution. For the past few decades, there has been a radical increase in computing performance and electronic products have become increasingly prevalent in all aspects of modern life. Increasing microprocessor performance is typically accompanied by increasing power and chip power density, both of which presents a massive cooling challenge. In this review article, the evolution of TIMs including polymer based TIM, solder based TIM, and the system-level thermal solutions and designs are summarized.

The microprocessor, which has most visibly exploited the benefits of Moore's law, has helped defined thermal management issues and solution strategies. It is interesting to note that the thermal management was discussed rhetorically while defining Moore's law when there were only a few thousand components in a single silicon chip [57]. Today, it is possible to cool a microprocessor with more than a billion transistors, an accomplishment that is the result of significant innovations in thermal management [58]. Historically, the major technical challenge associated with microprocessor thermal management has been the need to cool a significant TDP, nonuniformly distributed over a semiconductor chip, while maintaining a temperature difference defined by the die hot spot temperature on one end and system ambient temperature on the other. These days, MCPs, cost of materials, size of the package and reliability requirements also play a major role. Effective interactions between silicon technology, novel packaging process with variety of TIMs, and system-level design changes have led to innovations that continue to optimize the tradeoffs between performance and cost, and have led to our success to date. Moving forward, the challenge will continue to ensure availability of thermal solution technologies so that thermal management is not a limiter to performance. Industrial and academic researchers have correspondingly increased their focus on

elucidating the problem and developing innovative solutions in packaging materials and system-level designs. Examples of some of the current packaging materials and system thermal solutions are provided in detail in this article to depict a clear picture of the state-of-the-art thermal management.

Brief discussions of some of the future trends that are being developed by academic and industrial researchers to meet thermal demands are described in the following paragraph. Current commercial TIMs are capable of providing low thermal resistance between .03 and .1°C cm<sup>2</sup>/W immediately during assembly [59] but tend to degrade over a period of time when exposed to real-use conditions. The dynamic warpage of the package and the physical limitations of the materials play a key role in dictating the level of degradation. Use of nanoparticles and nanotubes is one research area that can be explored at the package level. Currently, research is focused on minimizing the thermal resistance of the TIM by increasing the conductivity of the TIM and lowering the particle size and bond line thickness. Also, there have been continuous efforts on improving the adhesion phenomena of the TIMs during reliability testing. IHS modification is another area which is under active evaluation for improved thermal performance. Nonconventional solids, such as graphite, carbon fiber, alloy formulations, and diamond are also being studied. Thermal conductivity for these solids is greater than the commercially used aluminum or copper IHS. The major problems with these new materials are cost and handling/forming. Graphite, carbon composites, or diamond materials are typically more expensive than copper. Heat pipes, vapor chambers, thermosiphons, etc., may all provide efficient heat dissipation [60]. Considering the spectrum of thermal technologies under evaluation, there is focus on improving the thermal resistance of TIMs and IHS on one end and developing exotic technologies such as nanofluidenhanced liquid cooling and solid state refrigeration on the other [61-65]. A good modeling assessment for the contact resistance between the particle-rich TIM material and its interaction with Silicon, IHS, and the substrate is still lacking from the published literature. Mechanical modeling incorporating the material characteristics and packaging assembly process will also be needed in the future to understand and improve the interfacial adhesion.

Nomenclature					
Adie:	Area of a semiconductor chip	G':	Storage shear modulus		
Ag:	Silver	G'':	Loss shear modulus		
Al:	Aluminum	HVM:	High volume manufacturing		
$Al_2O_3$ :	Aluminum oxide	IHS:	Integrated heat spreader		
BGA:	Ball grid array	IMC:	Intermetallic compound		
Bi:	Bismuth	In:	Indium		
BLT:	Bond line thickness	I/O:	Input output		
BN:	Boron nitride	IOT:	Internet of things		
BSM:	Back side metallization	ITRS:	International road map for semiconductors		
CPU:	Central processing unit	k <sub>TIM</sub> :	Thermal conductivity of the thermal in-		
DIW:	De-ionized water	11111	terface material		
FC:	Flip chip	LGA:	Land grid array		
FIB:	Focused ion beam	MCP:	Multi chip package		

Pb: Lead ZnO: Zinc oxide PC: Personal computer  $\Psi_{ja}$ : Overall thermal resistance Phase change material Package thermal resistance PCM:  $\Psi_{jc}$ :  $\Psi_{ca}$ : PDMS: Poly di methyl siloxane System thermal resistance PTIM: Polymer thermal interface material Micrometre μm: W/mK: Thermal impedance at junction to IHS Watt per metre kelvin R<sub>ic</sub>: °C: Degree celsius STIM: Solder thermal interface material MPa: Mega pascal Sn: Tin GPa: Giga pascal TIM: Thermal interface material Psi: Pounds per square inch  $W/m^2$ : TIM<sub>1</sub>: Die to IHS thermal interface material layer Watt per square metre TIM2: IHS to heat sink thermal interface material m/s: Metre per second Standard atmosphere units atm: T<sub>a</sub>: Ambient air temperature K: Kelvin TDP: Millimetre Thermal design power mm:  $T_c$ : Integrated heat spreader or case temperature C/W: Degree celsius per watt  $T_j$ : °Ccm<sup>2</sup>/W: Maximum junction temperature Degree celsius times square centimetre per

#### REFERENCES

Heat sink temperature

T<sub>sink</sub>:

- L.A. Polka, H. Kalyanam, G. Hu, and S. Krishnamoorthy, "Package technology to address the memory bandwidth challenge for Tera-scale computing," *Intel Technology Journal*, Vol. 11, pp. 197-205, 2007.
- [2] Developments and trends in thermal management technologies-A Mission to the USA report of a DTI global watch mission, http://www-eng.lbl.gov/ ~ecanderssen/STAR/Beam%20Pipe%20Info/Thermal%2520Management. pdf 2006.
- [3] Y. Li, R.W. Johnson, P. Thompson, T. Hooghan, and J. Libres, "Reliability of flip chip packages with high thermal conductivity heat spreader attach," Proceedings of the 58th IEEE Electronic Components and Technology Conference, pp. 2011-2017, Lake Buena Vista, FL, May 27-30, 2008.
- [4] International Technology Roadmap for Semiconductors, [Online] http:// www.itrs2.net/.
- [5] International Electronics Manufacturing Initiative, [Online] http://www.inemi.org/.
- [6] S.J. Dent, L.J. Larson, R.T. Nelson, and D.C. Rash, "Semiconductor package and method of preparing the same," US Patent 6940177, 2005.
- [7] S.F. De Cecco and G.W. Cheshire, "Cooling assembly using heat spreader," US Patent 9318410, 2016.
- [8] A.B. Chong, "Multi-chip packaging (MCP) or not MCP," Proceedings of the International MultiConference of Engineers and Computer Scientists (IMECS), Vol. 2, pp. 1-4, Hong Kong, March 14-16, 2012.
- [9] R. Mahajan, C.P. Chiu, and G. Chrysler, "Cooling a microprocessor chip," Proceedings of the IEEE, Vol. 94, pp. 1476-1486, 2006.
- [10] D.P.R. Thanu, R. Danaei, A. Bermudez, S. Chan, and S. Prstic, "Fundamental study of polymer to metal bonding in integrated circuit packaging," ASME InterPACK, pp. 1-9, San Francisco, CA, August 28-30, 2018
- [11] I. Sauciuc, R. Prasher, J.Y. Chang, H. Erturk, G. Chrysler, C.P. Chiu, and R. Mahajan, "Thermal performance and key challenges for future CPU cooling technologies," Proceedings of IPACK2005, ASME Inter-PACK'05, San Francisco, CA, July 17-22, 2005.
- [12] R. Prasher, "Thermal interface materials: historical perspective, status, and future directions," *Proceedings of the IEEE*, Vol. 94, pp. 1571-1586, 2006.
- [13] C. Deppisch, T. Fitzgerald, A. Raman, F. Hua, C. Zhang, P. Liu, and M. Miller, "The material optimization and reliability characterization of an indium-solder thermal interface material for CPU packaging," *JOM*, Vol. 58, pp. 67-74, 2006.
- [14] T.S. Sean, T. Maxat, K. Mohammad, M. Raj, D. Jacquana, and K. Kee-Hean, "Indium thermal interface material development for microprocessors," Proceedings of the 25th Annual IEEE Semiconductor Thermal Measurement and Management Symposium, SEMI-THERM, pp. 186-192, San Jose, CA, March 15-19, 2009.
- [15] H. Zhang, Y.C. Mui, P.E. Tan, and S.-H. Ng, "Thermal characterizations of solid thermal interface material," Proceedings of the 10th Electronic

- Packaging and Technology Conference (EPTC), pp. 1472-1478, Singapore, December 9-12, 2008.
- [16] C. Tanawan, N.T. Hoon, S. Jinda, S.B. Margaret, and A. Sai, "Indium solder as a thermal interface material using fluxless bonding technology," Proceedings of the 25th Annual IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), pp. 180-185, San Jose, CA, March 15-19, 2009.
- [17] A.L. Moore and L. Shi, "Emerging challenges and materials for thermal management of electronics," *Materials Today*, Vol. 17, pp. 163-174, 2014.
- [18] H.K. Dhavaleswarapu, C.M. Jha, S.F. Smith, S. Kothari, B. Bicen, S.K. Saha, and A. Gupta, "Challenges and opportunities in thermal management of multi-chip packages," Proceedings of the InterPACK, Vol. 1, pp. 1-7, San Francisco, CA, July 6-9, 2015.
- [19] K.L. Mittal and T. Ahsan (Eds.), Adhesion in Microelectronics, Wiley-Scrivener, Beverly, MA, USA, 2014.
- [20] D.P.R. Thanu, A. Antoniswamy, R. Danaei, and M. Keswani, "Adhesion phenomena pertaining to thermal interface materials and solder interconnects in microelectronic packaging- a critical review," *Reviews of Adhesion and Adhesives*, Vol. 6, pp. 1-25, Scrivener Publishing, 2018.
- [21] R. Mahajan, C.P. Chiu, and R. Prasher, "Thermal interface materials: a brief review of design characteristics and materials," *Electronics Cooling*, Vol. 10, pp. 1-12, 2004.
- [22] J.P. Gwinn and R.L. Webb, "Performance and testing of thermal interface materials," *Microelectronics Journal*, Vol. 34, pp. 215-222, 2003.
- [23] G.R. Cunnington, Jr., "Thermal conductance of filled aluminum and magnesium joints in a vacuum environment," Presented at the ASME Winter Annual Meeting, New York, ASME Paper No. 64-WA/HT-40, 1964
- [24] R.C. Getty and R.E. Tatro, "Spacecraft thermal joint conduction," Presented at the Thermophysics Specialist Conference, New Orleans, LA, AIAA Paper No. 67-316, April 17-20, 1967.
- [25] E.E. Marotta and L.S. Fletcher, "Thermal contact conductance of selected polymeric materials," *Journal of Thermophysics and Heat Transfer*, Vol. 10, pp. 334-342, 1996.
- [26] L.S. Fletcher, "A review of thermal enhancement techniques for electronics systems," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. 13, pp. 1012-1021, 1990.
- [27] S.R. Mirmira, E.E. Marotta, and L.S. Fletcher, "Thermal contact conductance of adhesives for microelectronic systems," *Journal of Thermophysics and Heat Transfer*, Vol. 11, pp. 141-145, 1997.
- [28] S.R. Mirmira, E.E. Marotta, and L.S. Fletcher, "Thermal contact conductance of elastomeric gaskets," *Journal of Thermophysics and Heat Transfer*, Vol. 12, pp. 454-456, 1998.
- [29] E.E. Marotta and B. Hana, "Thermal control of interfaces for microelectronic packaging," Proceedings of the Materials Research Society

- Symposium, Vol. 515, pp. 215-225, MRS Publications, San Francisco, CA, April 13-15, 1998.
- [30] Y. Xu, X. Luo, and D.D.L. Chung, "Sodium silicate based thermal interface material for high thermal contact conductance," *Journal of Electronic Packaging*, Vol. 122, pp. 128-131, 2000.
- [31] C.-P. Chiu, B. Chandran, K. Mello, and K. Kelley, "An accelerated reliability test method to predict thermal grease pump-out in flip-chip applications," Proceedings of the IEEE Electronic Components and Technology Conference (ECTC), pp. 91-97, Orlando, FL, May 29-June 01, 2001.
- [32] J. Wang, "Shear modulus measurement for thermal interface materials in flip chip packages," *IEEE Transactions on Components and Packaging Technologies*, Vol. 29, pp. 610-617, 2006.
- [33] R.S. Prasher and J.C. Matayabas, "Thermal contact resistance of cured gel polymeric thermal interface material," *IEEE Transactions on Components* and Packaging Technologies, Vol. 27, pp. 702-709, 2004.
- [34] M. Rubinstein and R.H. Colby, *Polymer Physics*, Oxford University Press, New York, NY, 2003.
- [35] D. Stauffer and A. Aharony, *Zntroduction tu Percolation Theory*, Taylor & Francis, Washington, DC, 1992.
- [36] N.E. Cusack, The Physics of Structurally Disordered Matter: An Introduction, Adam Hilger, Bristol, UK, pp. 227, 1987.
- [37] J. Kim, J.-S. Lai, and C.E. Konrad, "Thermal interface void reduction techniques for direct-soldered power modules," Power Electronics Specialists Conference, IEEE 33rd Annual Volume 2, pp. 743-747, Cairns, Queensland, Australia, June 23-27, 2002.
- [38] C. Deppisch, T. Fitzgerald, A. Raman, F. Hua, C. Zhang, P. Liu, and M. Miller, "The material optimization and reliability characterization of an indium-solder thermal interface material for CPU packaging," *Journal of the Minerals Metals & Materials Society*, Vol. 58, pp. 67-74, 2006.
- [39] F. Hua, C. Deppisch, and T. Fitzgerald, "Indium as thermal interface material for high power devices," *Advanced Microelectronics*, Vol. 33, pp. 16-17, 2006.
- [40] I. Sauciuc, R. Yamamoto, J.C. Viskota, T. Yoshikawa, S. Jain, M. Yajima, N. Labanok, and C.A. Kusia, "Carbon based thermal interface material for high performance cooling applications," 14th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), pp. 426-434, Orlando, FL, May 27-30, 2014.
- [41] S.K. Siow, "Mechanical properties of nano-silver joints as die attach materials," *Journal of Alloys and Compounds*, Vol. 514, pp. 6-19, 2012.
- [42] K.S. Siow, "Sintered silver (Ag) as lead-free die attach materials," 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT), pp. 1-6, Ipoh, Perak, Malaysia, November 6-8, 2012.
- [43] K.S. Siow, "Are sintered silver joints ready for use as interconnect material in microelectronic packaging," *Journal of Electronic Materials*, Vol. 43, pp. 947-961, 2014.
- [44] S.V. Garimella, T. Persoons, J.A. Weibel, and V. Getkin, "Electronics thermal management in information and communication technologies: challenges and future directions," *IEEE Transactions on Components*, *Packaging, and Manufacturing Technology*, Vol. 7, pp. 1191-1201, 2017.
- [45] S. S. Kang, "Advanced cooling for power electronics," CIPS, Nuremberg, Germany, March 6-8, 2012.
- [46] C.R. Chu, R.E. Simons, M.J. Ellsworth, R.R. Schmidt, and V. Cozzolino, "Review of cooling technologies for computer products," *IEEE Transactions on Device and Materials Reliability*, Vol. 4, pp. 568-585, 2004.
- [47] D.P.R. Thanu, "Use of dilute hydrofluoric acid and deep eutectic solvent systems for back end of line cleaning in integrated circuit fabrication," PhD dissertation, Materials Science and Engineering, University of Arizona, Tucson, AZ, 2011.

- [48] D.P.R. Thanu, S. Raghavan, and M. Keswani, "Use of urea-choline chloride eutectic solvent for back end of line cleaning applications," *Electrochemical and Solid-State Letters*, Vol. 14, pp. 358-361, 2011.
- [49] D.P.R. Thanu, N. Venkataraman, S. Raghavan, and O. Mahdavi, "Dilute HF solutions for copper cleaning during BEOL processes: effect of aeration on selectivity and copper corrosion," ECS Transactions, Vol. 25, pp. 109-116, 2009.
- [50] D.P.R. Thanu, S. Raghavan, and M. Keswani, "Effect of water addition to choline chloride-urea deep eutectic solvent (DES) on the removal of postetch residues formed on copper," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 25, pp. 516-522, 2012.
- [51] D.P.R. Thanu, S. Raghavan, and M. Keswani, "Post plasma etch residue removal in dilute HF solutions," *Journal of the Electrochemical Society*, Vol. 158, pp. 814-820, 2011.
- [52] A.E. Bergles and A. Bar-Cohen, Direct Liquid Cooling of Microelectronic Components, Advances in Thermal Modeling of Electronic Components and Systems, Vol. 2, pp. 233-342, Bar-Cohen and Kraus Ed., ASME Press, New York 1990
- [53] 3M, "Two phase immersion cooling," [Online]. https://www.3m.com/3M/en\_US/novec-us/applications/immersion-cooling, 2018.
- [54] F.P. Incropera, "Liquid immersion cooling of electronic components," Heat Transfer in Electronic and Microelectronic Equipment, A.E. Bergles, Ed., Hemisphere Publishing Corp., pp. 407-444, NY, 1990.
- [55] Z. Lu, Design and Modeling of a High Flux Cooling Device Based on Thin Film Evaporation from Thin Nanoporous Membranes, Massachusetts Institute of Technology, Cambridge, MA, 2014.
- [56] L. Zhengmao, T.R. Salamon, S. Narayanan, K.R. Bagnall, D.F. Hanks, S.D. Antao, B. Barabadi, J. Sircar, M.E. Simon, and E.N. Wang, "Design and modeling of membrane-based evaporative cooling devices for thermal management of high heat fluxes," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 6, pp. 1056-1065, 2016.
- [57] G. Moore, "Cramming more components onto integrated circuits," *Electronics (Basel)*, Vol. 38, pp. 114-117, 1965.
- [58] S. Naffziger, B. Stackhouse, and T. Grutkowski, "The implementation of a 2-core multi-threaded Itanium family processor," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, Vol. 592, pp. 182-183, 2005.
- [59] E. Samson, S. Machiroutu, J.-Y. Chang, I. Santos, J. Hermarding, A. Dani, R. Prasher, D. Song, and D. Puffo, "Interface material and a thermal management technique in second-generation platforms built on Intel Centrino Mobile Technology," *Intel Technology Journal*, Vol. 9, pp. 75-86, 2005.
- [60] Y. Joshi, "Microfabrication alliance for innovative cooling of microelectronics," Presented at the DARPA HERETIC Principle Investigator's Meeting, Heat Removal by Thermo-Intergrated Circuits, Atlanta, GA, 2001.
- [61] R. Prasher, P. Bhattacharya, and P. Phelan, "Thermal conductivity of nanoscale colloidal solutions (nanofluids)," *Physical Review Letters*, Vol. 94, No. 2, pp. 025901-1-025901-4, 2005.
- [62] G. Upadhya, P. Zhou, J. Hom, K. Goodson, and M. Munch, "Electrokinetic microchannel cooling system for servers," Proceedings of the Intersociety Conference on Thermal and Thermomechanical Phenomena, pp. 367-371, Las Vegas, NV, June 1-4, 2004.
- [63] S. Garimella and C. Sobhan, "Transport in micro-channels—a critical review", *Annual Review of Heat Transfer*, Vol. 13, pp. 1-50, 2003.
- 64] R. Venkatasubramanian, E. Silvola, T. Colpitts, and B. O'Quinn, "Thin-film thermo-electric devices with high room-temperature figures of merit," *Nature*, Vol. 413, pp. 597-602, 2001.
- [65] I. Sauciuc, G. Chrysler, R. Mahajan, and R. Prasher, "Spreading in the heat sink base: phase change systems or solid metals," *IEEE Transactions on Components and Packaging Technologies*, Vol. 25, pp. 621-628, 2002.