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System-on-Chip Integrated MEMS Packages for RF LNA Testing and Self-Calibration

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Abstract—**In this paper, we present MEMS-enhanced integrated package design which provides the capability to self-test and self-calibrate integrated circuit chips. We have developed a novel test technique where the test stimulus is generated by modulating the RF carrier signal with another signal mixed with additive white Gaussian noise. This novel test stimulus is provided as the input to the RF circuit and the peak-to-average ratio (PAR) is measured at the output. Simulations were carried out for fault-free and fault-induced circuit conditions, and their corresponding PARs were stored in the look-up table (LUT). Test simulations were performed and the results were compared with the look-up table to verify whether the device is fault-free. In faulty circuit conditions, calibration was performed using a tuning circuit made of MEMS switches. The entire validation of the design using the test technique and self-calibration of the RF circuit was automated using the calibration algorithm. This testing and self-calibration technique is exhaustive and efficient for present-day communication systems.**

Keywords—**Low noise amplifier (LNA), MEMS, peak-to-average ratio (PAR), RF testing, self-calibration**

Introduction

Modern communication systems require the entire radio frequency (RF) system to fit on a single chip. CMOS technology is widely used for designing the RF system as it provides the advantage of high functionality at low cost. However, as CMOS technology shrinks to nanometer dimensions, the sensitivity of process variations causes degradation in the RF performance of the circuit, making designing sensitive RF circuits extremely difficult. Moreover, the extraction of parasitics from passive devices has become increasingly difficult, due to higher operating frequency and smaller interconnect spacing. These problems lead to a significant loss in parametric yield. Hence, testing the fabricated chip for parametric variations is essential.

Once the chip is packaged to realize the device, with constant usage over a continuous period of time there is a high probability of performance variations occurring within the chip [1]. These variations can be attributed to factors such as thermal fatigue, mechanical shock, self-heating, and electromigration. In today's consumer electronics, a device is guaranteed to work over a specific period of time. But replacing RF chips that exhibit low performance after continuous usage due to various fatigue and ageing factors is not cost-effective. Hence, it is of the utmost importance to automatically detect performance variations within the device and self-calibrate it to design specification levels.

A self-calibration methodology that can address both process-related and time-degraded variations is presented in this paper. Prior work has been done to test RF chips where faulty chips are either debugged and reprocessed to nullify the defects or discarded, depending on the nature of the defects [2]. This process takes a great deal of time and effort and requires specialized equipment to precisely correct the faults on the chip. Several on-chip techniques to detect and rectify the defects have been previously proposed, but they utilize complex external hardware circuitry and are not cost-effective [3]. Hence, there is an immediate need for improved testing and on-chip calibration methodology that is simple, inexpensive, and has a high degree of accuracy.

We propose a system-on-chip (SoC) approach to design the RF, testing, and self-calibration circuits on a single chip. Our tuning circuit used for self-calibration is based on MEMS switches, which increases the complexity of fabricating multiple technologies on a single silicon substrate. We have designed our circuits to accommodate these fabrication challenges such that the MEMS switches provide a high degree of isolation without coupling with the RF signals in the LNA circuits. Fig. 1 shows the internal block diagram of the proposed testing and self-calibration approach.

This paper is organized as follows. The LNA Design and Test Stimulus Synthesis Section provides an overview of the low noise amplifier (LNA) design and the synthesis of the test stimulus. The MEMS Tuning Circuit Section provides details on the MEMS-based tuning circuit and the switch matrix used for performing self-calibration. The Calibration Algorithm Section provides the calibration algorithm to automate the testing and calibration procedure as well as the SoC approach to incorporate the RF, test, and self-calibration circuits on a single chip. The LNA Testing Simulation Results Section highlights test simulation results using the multitone stimulus test technique and generation of a look-up table (LUT).

LNA Design and Test Stimulus Synthesis

In conventional communication systems, the RF front-end receiver has various functional blocks. Among these, the most important block is the LNA. LNA is generally the first stage of

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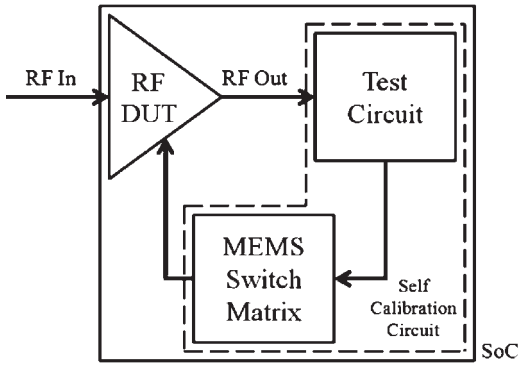

Fig. 1. System-on-chip architecture of the test and self-calibration circuitry.

the RF receiver subsystem and its functional performance is essential, because it amplifies the received low power signal by the designated amplification factor that will be provided to the next stage. Ideally, an LNA suppresses externally acquired noise and amplifies the input signal. However, in practical applications, the LNA reduces the input signal noise and adds an extremely low noise to the input signal [4]. Hence, designing the LNA is both critical and painstaking.

A narrowband LNA (N-LNA) is used as the reference RF circuit in this paper. The design requirements of the LNA focus on high gain, low noise, stability, high linearity, perfect input-output match, and low power consumption. Impedance matching is one of the most important factors considered during LNA design. The input reflection coefficient (S_{11}) determines the input match and is also related to the forward gain (S_{21}) of the LNA. Parametric variations cause a shift in the operating frequency of the LNA, thereby leading to a change in S_{11} and S_{21} parameters [5]. This leads to an impedance mismatch between the LNA and the ensuing stages of the RF receiver, resulting in an attenuation of the input signal. Designing an LNA, especially for high-frequency applications, is challenging to even the most experienced circuit designers for the following reasons [6]:

1. Selection of the transistor, which is the first and most important step in LNA design.
2. An excess of factors to be considered simultaneously: high gain, low noise figure, unconditional stability, and good input and output match at the lowest possible current levels.
3. Design challenges such as interdependence of gain, stability, noise figure, and input/output match.

In this paper, the Atmel n-channel MOSFET based on 0.18 μm CMOS technology was chosen as the transistor for the LNA [7]. The specifications of the LNA are listed in Table I.

Fig. 2 shows the circuit schematic of the LNA. Transistor $M_{\text{currMirror}}$ forms a current mirror with M_{input}. Its width is considered to be a small fraction of that of M_{input} in order to minimize the power overhead of the bias circuit [8]. The current through $M_{\text{currMirror}}$ is set by the supply voltage V_{dd} and R_1 in conjunction with the V_{gs} of $M_{\text{currMirror}}$. Resistor R_2 is chosen that is large enough for its equivalent noise current to be negligible. M_{cascode} reduces the interaction of the tuned output with the tuned input and also reduces the effect of M_{input}'s C_{gd} on the output match. The total node capacitance

Table I
LNA Specifications

Parameter	Symbol	Range
Input match	S_{11}	≤ -15 dB
Forward gain	S_{21}	≥ 8 dB
Output match	S_{22}	≤ -10 dB
Noise figure	NF	≤ 2 dB
Stability factor	K	≥ 1

at the drain of M_{cascode} resonantes with L_{d1} to increase the gain at the center frequency [9]. The input and output resonances are generally equal to each other but can drift with an offset from one another to yield a flatter and broader response, if needed. The M_{match} transistor is used to widen the gain response of the LNA around the center frequency in order to slightly decrease its sensitivity around the operating frequency range. This leads to better resistance against smaller variations in the component values of the LNA [10]. The M_{match} transistor is chosen in such a way that its base-to-emitter capacitance C_{be} is equal to the average of the gate-to-source capacitance of M_{cascode} and the gate-to-drain capacitance of M_{input}. This causes a small reduction in the drain current, leading to a decrease in LNA gain, but achieves a much smaller input reflection coefficient, making the LNA less sensitive to minor parasitic losses [6].

With continuous usage of the designed LNA over a long period of time, process-related and time-degraded variations occurs that can affect LNA parameters such as gain, noise figure, stability factor, and impedance match. The main reason behind the loss of parametric yield is the change in the component values of the LNA. The LNA is designed with a set of parametric component values, as shown in Table II.

Since the variations affect the component values, we see an offset in the values of the LNA parameters. Hence, by closely observing the parametric changes, we can trace them to identify the exact affected components. We thus have a cost-effective and accurate on-chip testing procedure to identify the parametric variations in the LNA and have provided the details to synthesize the test stimulus required for performing testing on the LNA.

To this purpose, we have developed a novel test technique to perform LNA testing, called the multitone stimulus test technique. The test stimulus is synthesized by modulating an RF signal and multitone signal with added white Gaussian noise and random phase shift among the individual tones from an AWG. The resulting test signal is obtained as shown in the block diagram in Fig. 3.

This test signal is obtained by maintaining the frequencies of the RF carrier signal and the multitone signal at the same level. The test signal is provided as an input stimulus to the LNA, and the output of the LNA is then given to a detector that records the peak and average values to obtain the PAR values. For a perfectly matched LNA, there is a set of values defined for the components in the circuit, such as the gate capacitance (C_{g}), source inductance (L_{s}), and drain capacitance (C_{d}). If these values are disturbed, the parameters of the LNA drift away from their designed values. The simulation was

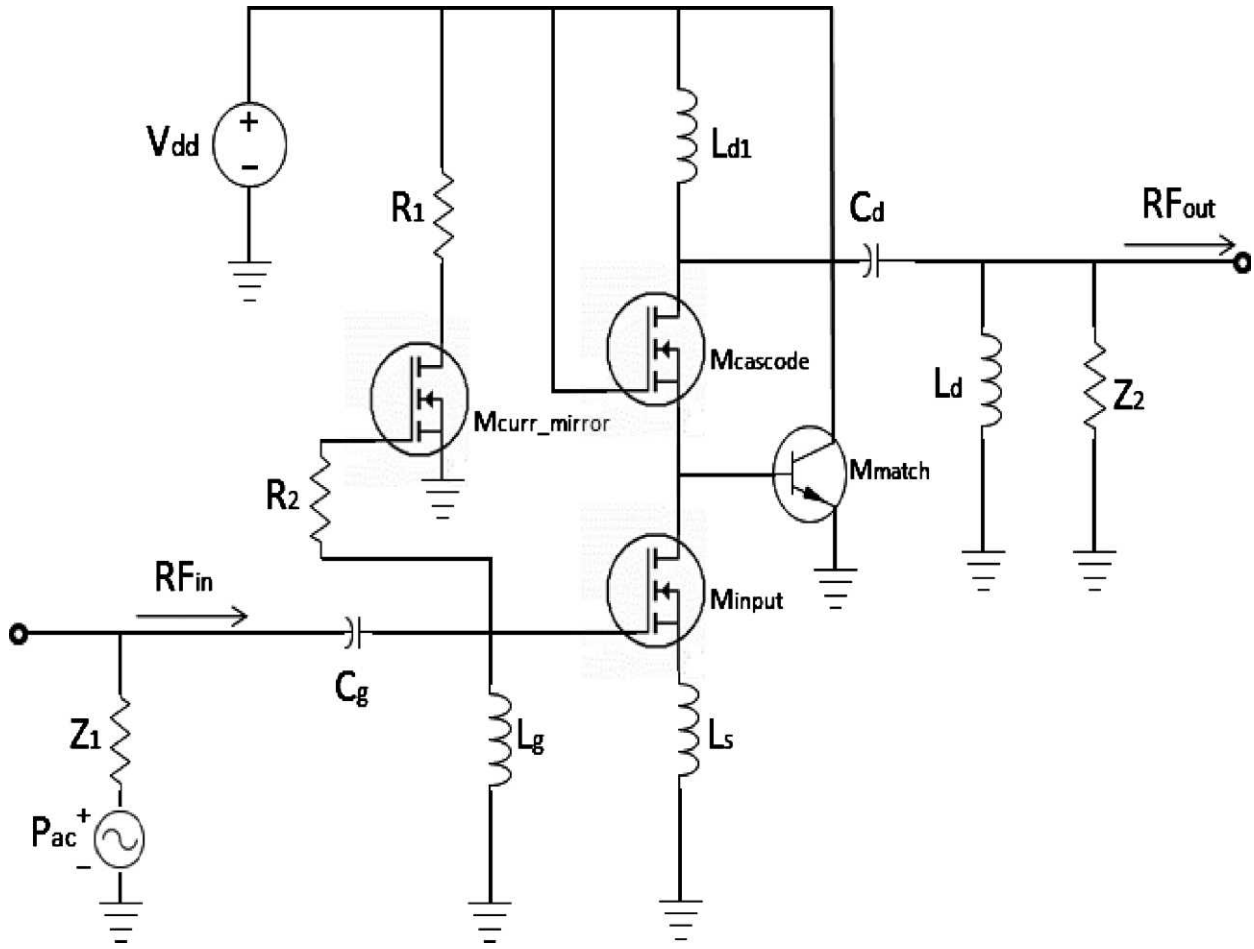

Fig. 2. Circuit schematic of 5 GHz LNA.

performed and the PAR values were observed for several fault-induced cases. There is a significant difference in the PAR values between the fault-free and the fault-induced cases. In addition, we could identify a significant difference in PAR values for individual faults and multiple faults. This allowed us to identify the specific defect(s) with high precision. Once the defect was identified, we performed calibration using the MEMS tuning circuit discussed in the following section.

Table II
LNA Component Values

Component	Value	Purpose
C_g	280 fF	Input match
L_g	2.5 nH	Input match
L_s	0.48 nH	Input match
M_{input}	$L = 0.18$ μm, $W = 4.8$ μm	Amplification
$M_{cascode}$	$L = 0.18$ μm, $W = 4.8$ μm	Amplification
R_1	1 kΩ	DC bias
R_2	50 kΩ	DC bias input reduction
$M_{currMirror}$	$L = 0.18$ μm, $W = 2.4$ μm	DC bias current mirror
C_d	340 fF	Output match
L_d	2.8 nH	Output match
L_{d1}	6.9 nH	Output match
V_{dd}	1.8 V	Power supply

MEMS Tuning Circuit

The proposed self-calibration scheme consists of a tuning circuit interfaced with the LNA by MEMS switches [13]. RF MEMS switches are used in high-frequency electronic systems because of their high electromechanical isolation. With MEMS switches, as opposed to the conventional solid state switches, the RF circuit does not leak or couple significantly

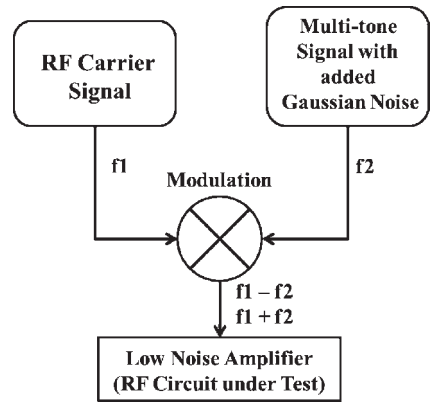

Fig. 3. Test signal synthesis [11, 12].

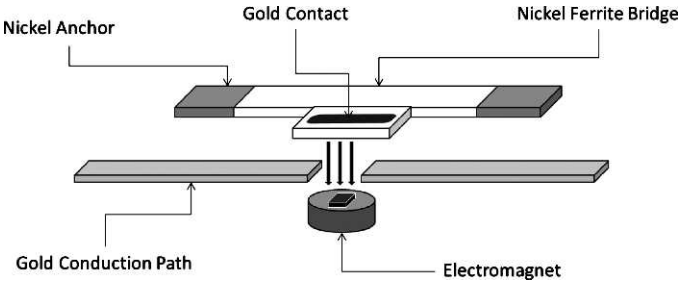

Fig. 4. Magnetic MEMS switch plan view.

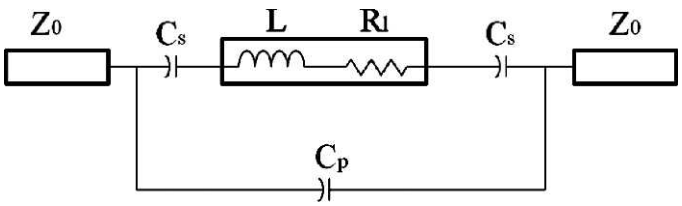

Fig. 5. Down state electrical model of the MEMS switch.

to the actuation circuit [13]. RF MEMS switches can deliver high isolation levels of about –55 dB at frequencies as high as 30 GHz [14], which makes them ideal for use. The MEMS switch designed for use in this work is magnetically actuated and has a low spring constant [15]. The design involves a bridge structure, which is preferred over the conventional cantilever beam type because of its robustness in high stress environments and overall stability [16]. The bridge structure is composed of nickel ferrite and is 1000 μm long, 200 μm wide, and 4 μm thick. It has the ability to bend in the presence of a magnetic field. The plane view of the magnetic MEMS switch is shown in Fig. 4.

An arm is connected to the bridge, which closes the circuit through a conduction path. A permanent magnet is placed outside the device structure to actuate the beam and hence close the switch by default. A coil is used to open the switch by creating a magnetic field equal and opposite to the field produced by the permanent magnet, which restores the beam due to spring force, thereby creating a dynamic equilibrium. This design method improves the total power consumption of the switch since it is coupled with the permanent magnet in a normally closed position [15].

Since the MEMS switches are a part of the complete circuit, they need to be modeled to observe their effects on the LNA's performance. For this, electrical models are developed for the MEMS switches and then analyzed. When the switch is in the ON state, this is also called the "down state" of the switch and when it is in the OFF state, this is called the "up state." Initially, the switch is in the down state when no actuation voltage is applied. In this case, the gold contact is pulled down by the permanent magnet and a physical contact is established to the conduction path. The electrical equivalent model of the MEMS switch in the down state is shown in Fig. 5. The gold conduction path is modeled as a transmission line (t-line) with impedance Z_0. The transmission line loss is given by R_{s1}, the contact resistance by R_c, and the gold contact by an inductor L in series with a resistor R_l is shown in Fig. 6.

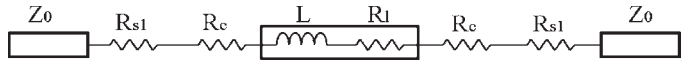

Fig. 6. Up state electrical model of the MEMS switch.

The total force exerted on the switch depends on the intensity of the magnetic field produced by the permanent magnet, the volume of the ferromagnetic material embedded on the bridge, and the spring constant of the flexible bridge [15]. The contact resistance (R_c) depends on the size of the contact area, the mechanical force applied, and the quality of the metal-to-metal contact [17]. The MEMS series switch resistance between the contact areas is dependent on its length and width and is obtained by calculating the loss of a t-line with the same dimensions as the MEMS switch; the total switch resistance is given by

$$R_s = 2 \cdot R_c + 2 \cdot R_{s1} + R_1. \quad (1)$$

In the up state, the switch can be modeled as shown in Fig. 7. In this state, capacitive effects dominate the electrical behavior of the switch. A net capacitance, also known as the up state capacitance, is present and is composed of a series capacitance (C_s) between the transmission line and the switch metal and a parasitic capacitance (C_p) between the open ends of the t-line. The total up state capacitance is given by

$$C_u = \frac{C_s}{2} + C_p. \quad (2)$$

C_s is composed of a parallel plate component ($C_{pp} = \frac{\varepsilon A}{b}$) and a fringing component that is around 30-60% of C_{pp} [18]. C_p is computed using specialized MEMS software packages such as MEMSPro, and its electrical model in the up state is shown in Fig. 5.

The tuning circuit consists of a bank of inductors and a capacitor connected to the LNA such that the input and output impedance match is returned to design-level specifications after calibration is performed. Fig. 7 shows the LNA circuit schematic with the MEMS tuning circuit.

In Fig. 7, $M[1]$, $M[2]$, $M[3]$, $M[4]$, $M[5]$, and $M[6]$ represent the MEMS switches and L_{calib1}, L_{calib2}, L_{calib3}, and C_{calib} represent the additional tuning circuit components used for self-calibration. The values of L_{calib1}, L_{calib2}, L_{calib3}, and C_{calib} are determined by taking into account the sensitivity level of the respective component they calibrate. Since these tuning components are fabricated on the die and their parametric values are nonscalable, we perform LNA calibration up to a predetermined range. The values of L_{calib1}, L_{calib2}, L_{calib3}, and C_{calib} are obtained with eqs. (3-6) with the design constraint being that the input and output match should not be disturbed.

$$L_{calib1} = \frac{3L_s}{2} \quad (3)$$

$$L_{calib2} = \frac{L_g}{2} \quad (4)$$

$$L_{calib3} = \frac{L_d}{2} \quad (5)$$

$$C_{calib} = \frac{14C_g}{5} \quad (6)$$

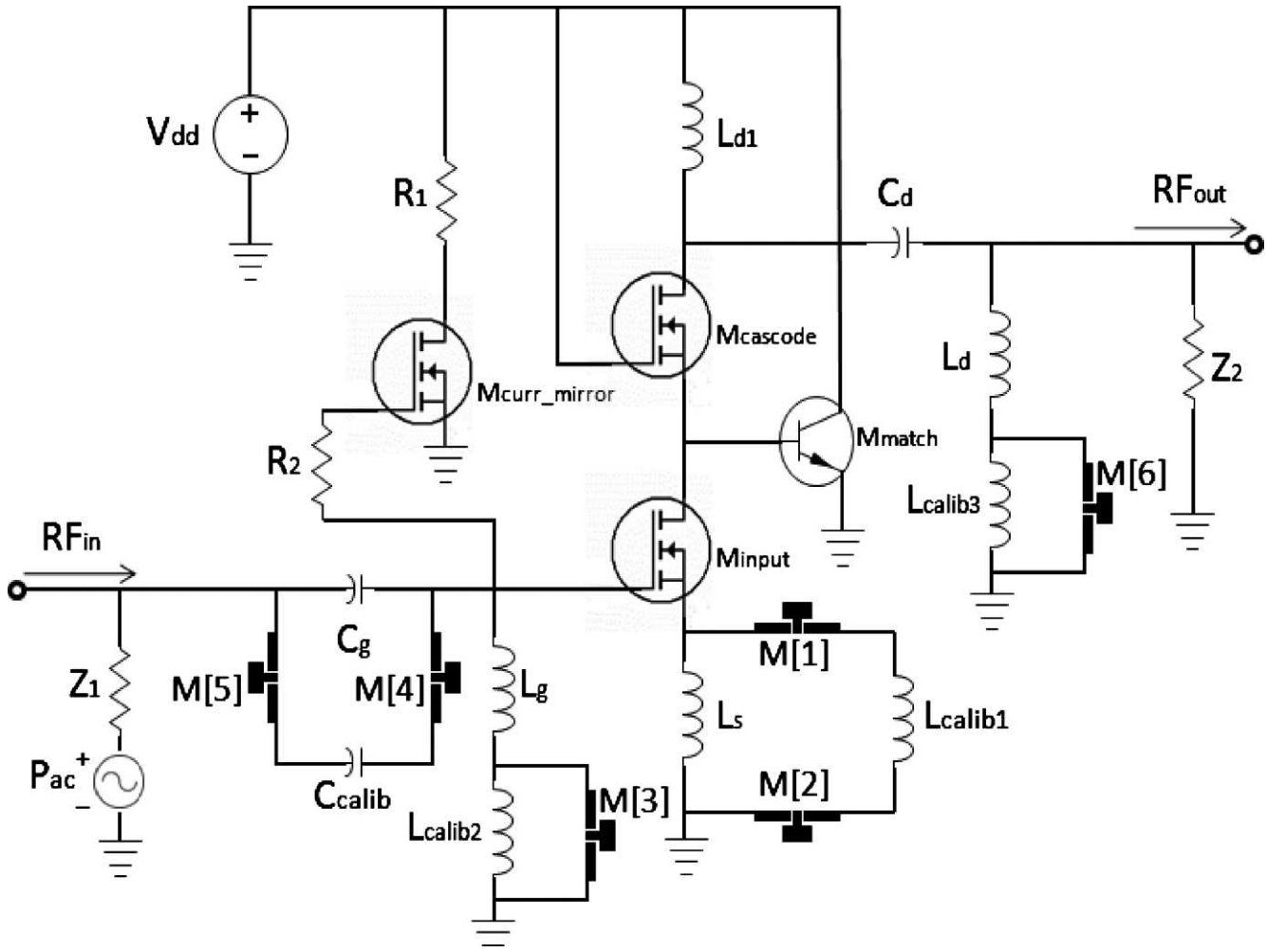

Fig. 7. LNA with MEMS tuning circuit.

Fig. 8 shows the layout of the LNA with MEMS switches in the proposed SoC approach.

To perform calibration, the MEMS switches are turned either ON or OFF to interface respective tuning circuit components with the LNA. The LNA is initially tested for fault-free cases and later by inducing faults in various components using the multitone stimulus test technique; the PAR values for each respective case are then recorded and stored in a look-up table. By comparing the PAR value of the fault-free case to the fault-induced case, we localize the fault to a respective component in the LNA circuit. Once the fault is localized, this information is carried over to determine which MEMS switches are activated by the MEMS switch matrix. The MEMS switch matrix is a (1 × 6) matrix with 0 representing the OFF state and 1 representing the ON state of the MEMS switches. The syntax of the MEMS switch matrix is M[1,*i*] where $i = 1, 2, \ldots, 6$, representing individual MEMS switches. Table III shows the look-up table with the MEMS switch matrix.

In the case of a faulty LNA, the MEMS switches to be activated to perform calibration are determined from the differential PAR values. If a MEMS switch is activated, a 1 that is equivalent to 9 V is stored; otherwise a 0 equivalent to 0 V is stored in the switch matrix.

Calibration Algorithm

The self-calibration algorithm uses an elect-and-select process. Self-calibration is performed after the testing is completed and the look-up table is populated. When the LNA is identified

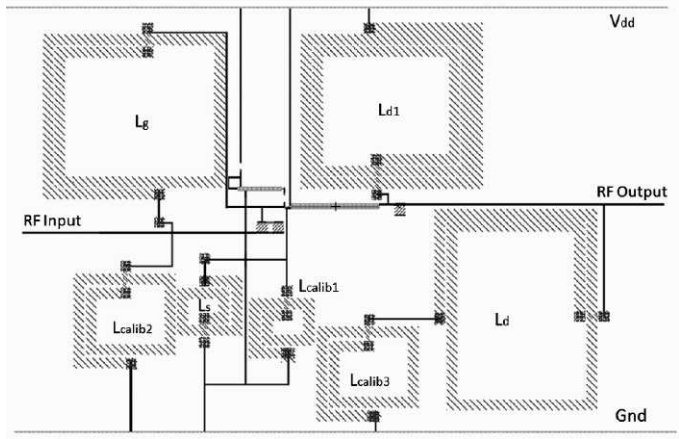

Fig. 8. Layout of the LNA with the tuning circuit.

Table III
Look-up Table

Condition	Sensitivity	Differential PAR(dB)	MEMS Switch Matrix
Fault-free	None	0	[0, 0, 0, 0, 0, 0]
C_g	20% decrease	16.2	[0, 0, 0, 1, 1, 0]
L_g	30% decrease	8.3	[0, 0, 1, 0, 0, 0]
C_g, L_g, and L_s	40% decrease, 80% decrease, and 60% increase	454	[1, 1, 1, 1, 1, 0]
C_g, L_g, and L_s	50% decrease, 20% decrease, and 70% increase	478	[1, 1, 1, 1, 1, 0]
C_g, L_g, and L_s	30% decrease, 60% decrease, and 40% increase	484	[1, 1, 1, 1, 1, 0]
C_g, L_g, L_s, and L_d	40% decrease, 20% decrease, 80% increase, and 20% decrease	246	[1, 1, 1, 1, 1, 1]
C_g, L_g, L_s, and L_d	30% decrease, 30% decrease, 60% increase, and 40% decrease	138	[1, 1, 1, 1, 1, 1]

as faulty and the corresponding PAR value is recorded, the respective MEMS switch matrix is then generated. This switch matrix is activated by controlling the supplies to the MEMS switches using the calibration algorithm. In certain cases of aliasing, the PAR value has multiple MEMS switch matrix definitions. In this case, each matrix is implemented in successive order until the right match is found. Since, in this case, a series of MEMS switch combinations is briefly elected in succession until the right combination is found and selected, this process is termed elect-and-select. Fig. 9 shows the self-calibration flowchart implementing the calibration algorithm.

LNA Testing Simulation Results

LNA testing is performed using the multitone stimulus test technique. The synthesized test stimulus is given as the input signal to the LNA, and the corresponding output PAR is computed using the following relations [11]:

$$\mathrm{PAR} = \frac{V_{\mathrm{peak}}}{V_{\mathrm{rms}}} \tag{7}$$

$$V_{\mathrm{peak}} = \max_t\{|a(t)|\} \tag{8}$$

$$V_{\mathrm{rms}} = \sqrt{\lim_{x\to N}\frac{1}{2x}\int_0^N a^2(t)dt} \tag{9}$$

The sensitivity of the test depends on the test frequency and the number of tones used. The PAR values computed are stored in the look-up table shown above. The ideal performance of the LNA is as shown in Fig. 10.

When fault-free simulation is completed, we induce various faults in the LNA and perform exhaustive fault condition simulations before recording the PAR values in the look-up table. Hardware testing of the LNA is performed after the look-up table is populated; the output is then compared with the look-up table to identify the LNA's functional performance level. Fig. 11 shows the differential PAR obtained for the various fault simulation cases.

If the LNA is faulty, based on the MEMS switch matrix, we activate the appropriate MEMS switches to perform calibration. We have performed three case studies on the LNA, which are illustrated below.

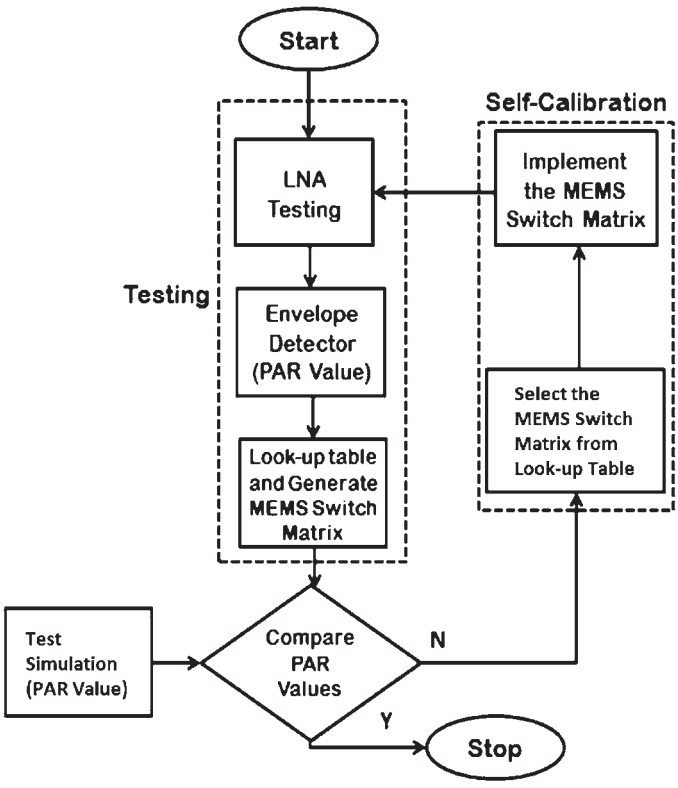

Fig. 9. Self-calibration flowchart.

A. Case 1

In this case, gate capacitor C_g is varied from design-level specifications of the LNA. This affects the parametric yield of the LNA. If a fault is induced into the LNA at C_g by reducing it by 40%, then the resultant gain and noise figure are as shown in Fig. 12a and 12b.

Fig. 12 represents the data obtained from simulation of circuits with a fault induced in the gate capacitor C_g. The gain is reduced to 6.98 dB from 8.9 dB and the noise is increased to 2.44 dB from 0.96 dB. By following the testing procedure mentioned in the MEMS Tuning Circuit Section, the respective MEMS switch matrix chosen is [0, 0, 0, 1, 1, 0]. From the switch matrix, it can be seen that switches $M[4]$ and $M[5]$ are activated. The gain response after calibration compared with fault-free LNA is shown in Fig. 12c, and the noise figure after calibration compared with fault-free LNA is shown in Fig. 12d.

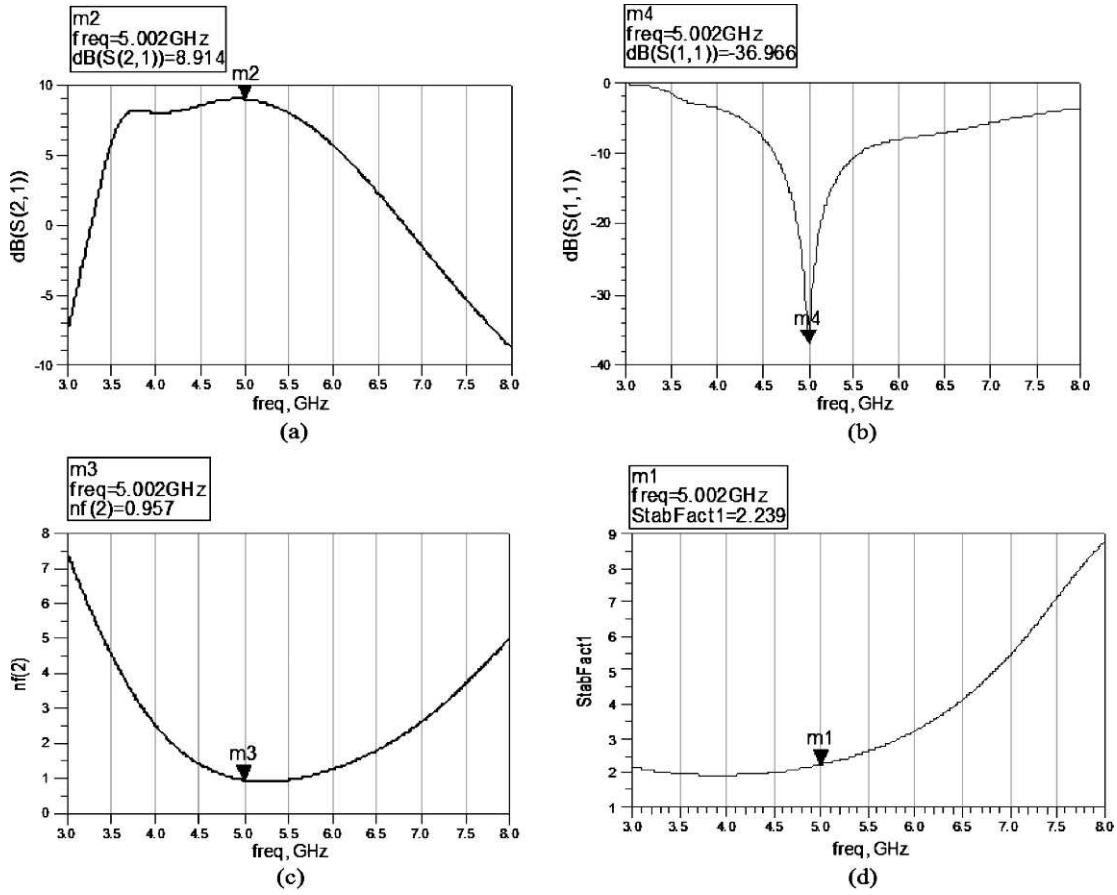

Fig. 10. (a) Transmission coefficient, (b) input reflection coefficient, (c) noise figure, and (d) stability factor.

B. Case 2

In Case 2, L_s is varied from design-level specifications of LNA, and the changes in parametric yield are analyzed. Fig. 13 represents the data obtained from the simulation of circuits with a fault induced in the source inductor L_s. If L_s increases by a factor of 1.6, then the gain drops to 6.86 dB and the noise rises to 1.14 dB. The noise is less than 1.5 dB, and thus in the acceptable range, but the gain is out of range. The respective plots are shown in Fig. 13a and 13b.

After testing, the respective MEMS switch matrix for this case is [1, 1, 0, 0, 0, 0]. Hence, switches M[1] and M[2] are activated. Fig. 13c shows the fault-free gain curve against the post-calibration gain curve. The gain curves in the fault-free state and after calibration are closely matched. A maximum difference of 1 dB is observed at 5 GHz and is well within the design specification range. The noise is also well within the acceptable range. After calibration, the noise stands at 0.88 dB, 0.5 dB less than the ideal value. Fig. 13d shows the comparison plot between fault-free and post-calibration noise figures.

C. Case 3

In Case 3, C_g decreases by 46%, L_g decreases by 40%, L_s increases by a factor of 1.45, and L_d decreases by 65%. This case is one of the worst possible faults and deteriorates LNA

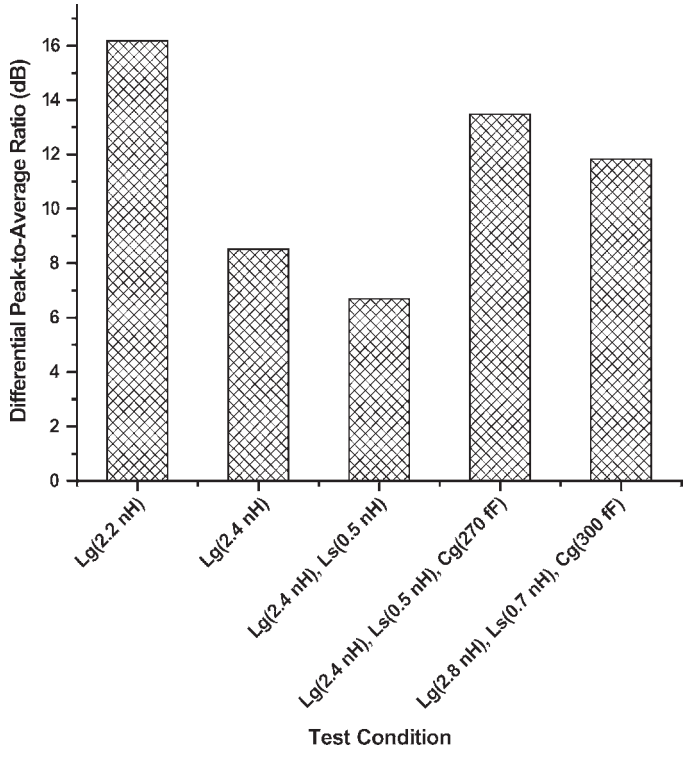

Fig. 11. Simulation of differential PAR for fault-free and fault-induced LNA.

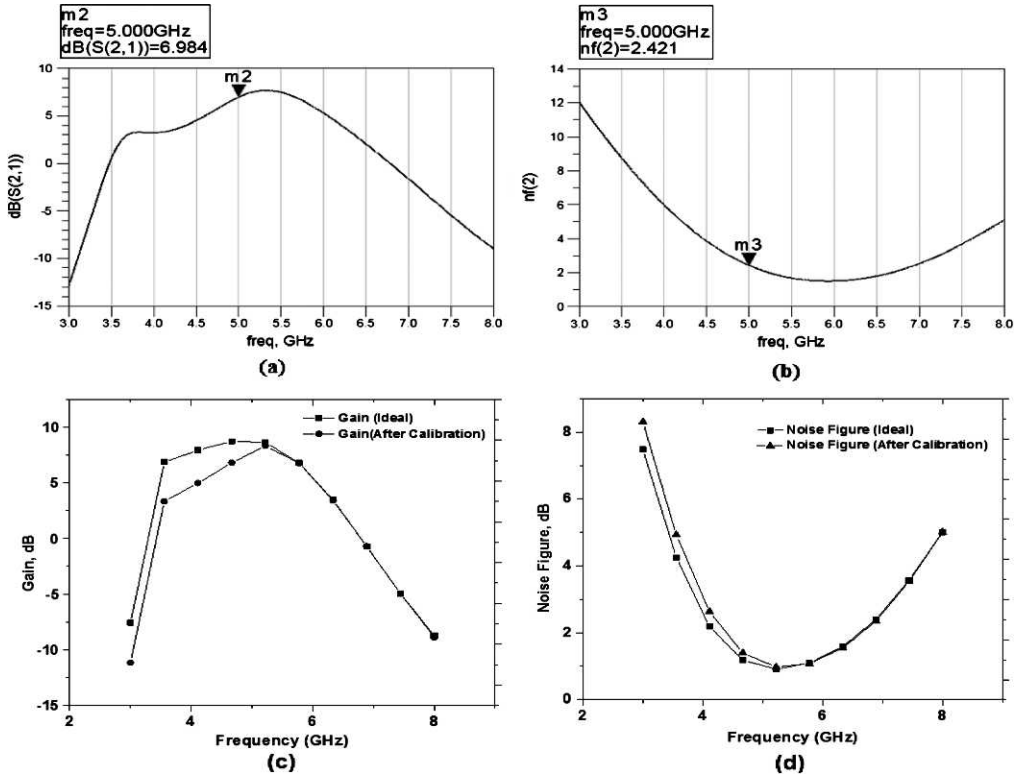

Fig. 12. (a) Transmission coefficient, (b) noise, (c) gain: fault-free versus calibrated, (d) noise: fault-free versus calibrated.

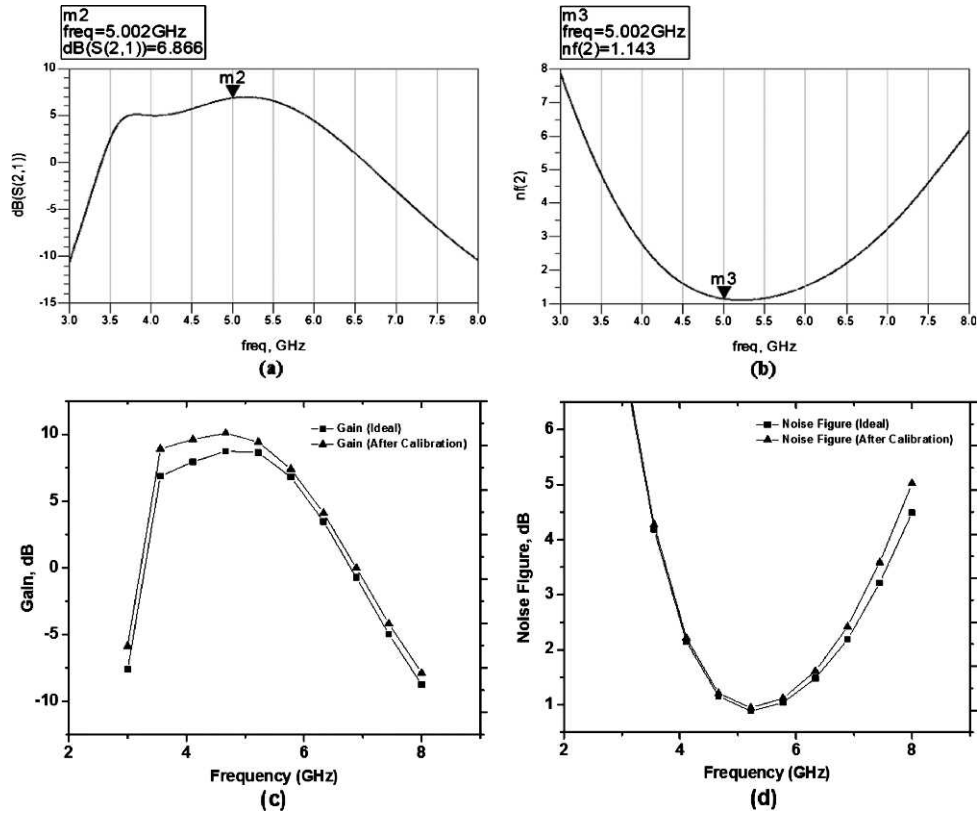

Fig. 13. (a) Transmission coefficient, (b) noise, (c) Gain: fault-free versus calibrated, (d) noise: fault-free versus calibrated.

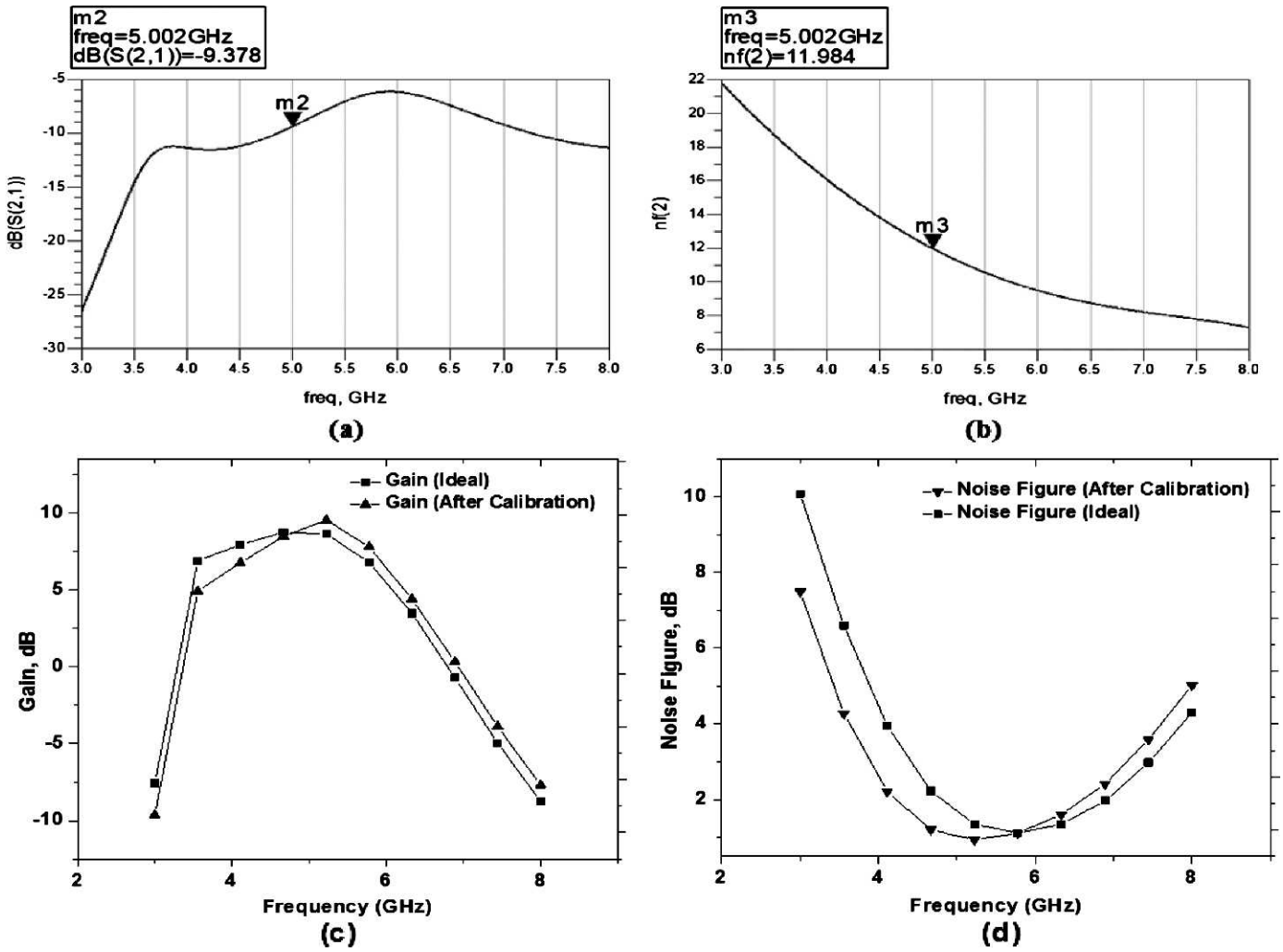

Fig. 14. (a) Transmission coefficient, (b) noise for a fault induced at C_g, L_g, L_s, and L_d, (c) gain: fault-free versus calibrated, (d) noise figure: fault-free versus calibrated.

performance to a great extent. Fig. 14 represents the data obtained from simulation of circuits with faults induced in the gate capacitor C_g, the gate inductor L_g, the source inductor L_s, and the drain inductor L_d. The gain of the LNA is reduced to -11 dB, which implies a huge impedance mismatch that results in reflecting back the entire received signal at the input of the LNA. The noise figure ascends to more than 6 dB, which corresponds to high noise levels at the output of the LNA. Both the gain and the noise are undesirable at these values. Hence, from the testing procedure, the respective MEMS switches to be activated to calibrate the LNA back to its operating region are determined. The required switch matrix looks like [1, 1, 1, 1, 1, 1], which implies that all the MEMS switches are to be activated in this case. The gain and noise after calibration are compared with their ideal counterparts and shown in Fig. 14.

After calibration, the gain of the LNA is in close agreement with the ideal gain value at 5 GHz. The calibrated value is about 0.8 dB higher than the ideal value and is acceptable. The noise, after calibration, is higher than the ideal value by almost 0.4 dB but is well within the acceptable range.

Conclusion

A novel testing and self-calibration scheme has been presented in this paper. These schemes are integrated using a SoC approach with the designed 5 GHz LNA on a single chip and help in improving its performance over process variations. The test circuitry includes an envelope detector to compute the PAR values of the RF output of the LNA. The PAR values are digitized by the analog to digital converter (ADC), and the result is compared with the look-up table stored in the DSP to test the LNA. Faulty LNAs are calibrated by generating a MEMS switch matrix from the look-up table. The use of MEMS switches in self-calibration enabled correction of gain and noise figure to their acceptable ranges of >8 dB and <2 dB, respectively. For future work, we would like to implement the MEMS-based test and self-calibration schemes proposed in this work along with the 3D-TSV stacking technique to the entire front end of the RF receiver subsystem. The stages after the LNA, like the mixer and the band-pass filter, can also utilize these techniques to reconfigure themselves and help maintain the complete RF front end in the designed operating region.

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