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Molding Flow Modeling and Experimental Study on Void Control for Flip Chip Package Panel Molding with Molded Underfill Technology

Jonathan Tamil,* Siew Hoon Ore, Kian Yeow Gan, Drake Koh, Michael Gantalao Ti In, Boon Pek Liew, Teck Wah Park, Geraldine Ng, Yong Bo Yang, Daniel Teh, Nathapong Suthiwongsunthorn, and Surasit Chungpaiboonpatana

Abstract—**Moldability is a crucial aspect of flip chip technology. It is an increasing challenge to ensure moldability with rapid advances in flip chip technology such as decreasing bump pitch and stand-off height, especially when commercial molded underfill (MUF) is used and, in particular, during panel level molding. One key challenge faced is severe void entrapment beneath the die. Typically, large DOE matrix experiments are used to address this issue, which require significant time and process resources. 3D flow simulation can be used to optimize the process to reduce defects with a smaller number of actual runs. By correlating theoretical and experimental phenomena, flow simulation enhances the understanding of the complex fluid dynamics during the molding process. 3D flow simulation can assist in widening the process window, which is limited by the inherent machine and material challenges. This can be achieved by prediction of the effect of varying design, material, and process parameters on melt front behavior and void locations. 3D mold flow simulation using Moldex3D V10 is used to optimize the MUF transfer molding on selected flip chip devices.**

This paper proposes and verifies a systematic flow simulation methodology designed to save computational resources by using a three step analysis. The initial step, simplified panel level simulation, is to optimize the process parameters to obtain a balanced melt front. Next, on the package level, we studied the effect of various parameters. This analysis provides a prediction of the void location and an insight into the appropriate parameters to minimize the void problem. The optimized parameters from the preliminary simulation were used as guidelines. For the second step, a full validation was conducted. A complete full panel-level flow model was built, where the process and design parameters adopted in the actual molding were implemented. The actual void location and size from the experiment were captured by scanning acoustic microscope (SAM) machine and parallel lapping (p-lapping). Short shots were also obtained to study the melt front behavior. The panel mold filling simulations showed good correlation with the experimental short shots and actual void locations. The prediction capability is further enhanced by zooming in to the column level, and this enhanced model was able to predict the other lower risk voids away from the main problem areas. This was correlated with actual CSAM data and p-lapping.

The 3D flow simulation enhances the understanding of causes of flow imbalance, void signature, void formation, and the effect of varying bump height, die thickness, mold cap thickness, gate height, die orientation, transfer profile, and mold temperature as potential enhancement measures. With a successful correlation between simulation and process data as shown in this paper, we have demonstrated that mold flow simulation is a reliable tool to effectively reduce the design-to-implementation cycle time, identifying potential key problems during actual fabrication and potential solutions to reduce defects.

Keywords—**flip chip, MUF, simulation, void**

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United Test and Assembly Center, Singapore
*Corresponding author; email: Jonathan_Tamil@sg.utacgroup.com

Introduction

Flip chip packages have gained significant use in production over the years because of high input/output (I/O), enhanced performance, and small form factor [1]. While flip chip technology has various advantages compared to other high-density electronic packaging approaches, challenges include ensuring moldability and minimizing defects that come along with rapid advances in flip chip technology such as decreasing bump pitch, stand-off height, thinner package profiles, and molded underfill (MUF) materials. The complexity was further exacerbated by the possible interactions between these factors and their impact on package yield, reliability, and performance.

The transfer molding process using MUF for flip chip devices was developed to create a reduction of process steps, cycle time, and cost compared with the conventional capillary underfill process. However, void entrapment [2] challenges arise as the gaps at the bumps under the die become increasingly small, resulting in significant melt front imbalance and flow resistance. Experiments involving a large DOE matrix are typically used to solve this issue. However, applying the conventional trial-and-error method to optimize this process is time-consuming and difficult because of the complex interactions between fluid flow, heat transfer, and polymerization of MUF. Hence, computer-aided-engineering (CAE) is an effective tool for analyzing the complicated physical phenomena inherent in the process of encapsulation of flip chip packages. Simulation can be used to provide further insights into the underlying physics to help address the defect concerns.

In this paper, 3D mold flow modeling of the transfer molding process with MUF using Moldex3D V10 is applied to optimize design and process parameters that can reduce device

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defects and enhance yield. The Cross Castro-Macosko model is used to define the MUF epoxy viscosity behaviors, where the rheological parameters were acquired using a parallel plate rheometer and a differential scanning caloriemeter (DSC). The test vehicle selected is a flip chip package with a bump height of 100 μm.

A systematic approach was developed to address the complex flow issues. As the full panel bumped array of flip chip devices would require high computational resources and time, an initial simplified chip level simulation is used to study the effect of various parameters. This analysis provides a prediction of the void location and an insight into the appropriate parameters to minimize the void problem. With the insights provided by the preliminary study, the full panel level study is conducted next to evaluate the impact of process and design parameters with the aim of obtaining a balanced melt front and minimizing voids.

The actual void location and size from the experiment was captured by scanning acoustic microscope (SAM) machine and short shots were obtained. The mold filling simulation showed good correlation of the mold fronts obtained by process short shots and actual void locations. With the successful validation of the simulation, the simulation matrix as shown in Fig. 1 was designed for a comprehensive assessment of the process, design, and material impact on the molding performance.

From the rheokinetic flow modeling of the MUF process, we identified the key factors and minor factors on void trapping simulation results from the extensive list of process, design, and material parameters. This paper presents the valuable insights into various factors of flip chip device moldability based on process and materials used for the device. The insights can be used as upfront guidelines to predict and reduce potential product defects and failures.

With consideration of process, materials, and design, this study explores whether mold flow simulation is an effective tool to reduce design-to-implementation cycle time with identification of potential void and melt front imbalance issues before actual fabrication. The simulation tool is used actively in conjunction with materials, process, and design inputs and considerations, to predict the trend of various factors on moldability up front to reduce the yield, cost, and cycle time as shown in Fig. 2. With the increasing range of flip chip products, we provide a comprehensive closed-loop solution including mold flow, thermal, mechanical, and electrical studies [3] addressing the rising challenges faced with greater consumer demand for smaller and thinner flip chip packages with better performance and greater functionality.

Geometry	Process	Material
•Bump pitch •Bump height •Bump diameter •Package size •Die size •Die thickness •Bump population •Die orientation	•Mold temperature •Transfer profile •Preheat time •Transfer pressure	•Reactive Viscosity •Curing Kinetics •Gel time

Fig. 1. Rheokinetic flow modeling matrix.

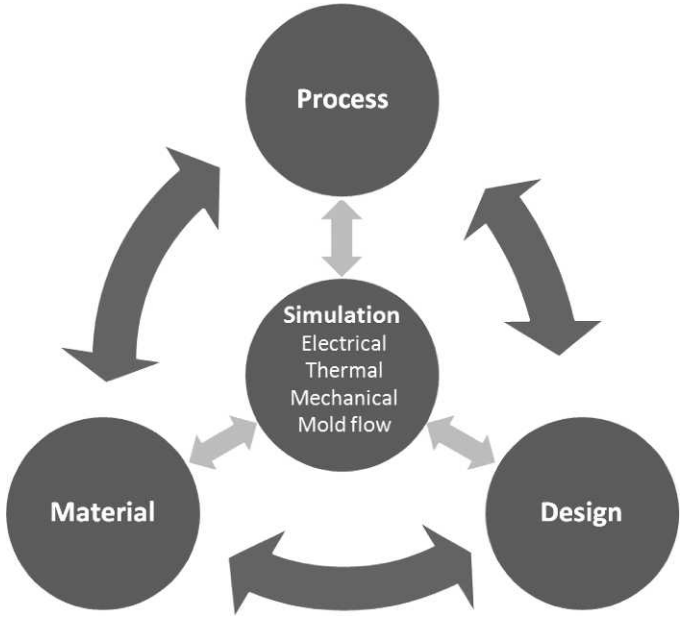


Fig. 2. Closed-loop material, process, design, and simulation to enhance flip chip product yield and reduce cycle time.

Rheokinetic Characterization of MUF

In the transfer molding process, flow and heat transfer are dynamically coupled with the curing reaction [4]. The kinetics of the curing reaction not only affects the degree of conversion of the molding compound, but also has a strong effect on the mold flow with increase in viscosity due to the curing reaction. Viscosity is also primarily influenced by temperature and shear rate. Therefore, the rheological behavior of molding compounds is of fundamental importance to model the molding process.

The MUF rheokinetic behaviors and other material properties were characterized for the flow modeling, including viscosity with varying shear rates and temperatures, curing kinetics, thermal conductivity, heat capacity, and mechanical properties. The curing kinetics were measured using DSC at different temperature ramp-up rates (5, 10, 20, 40°C/min). The experimental data of cure conversions were fitted by numerical parameters using Kamal's relation [5, 6] and the fitting parameters are summarized in Table I for MUF sample A. The experimental data and the numerical fitting line show good agreement, as shown in Figs. 3 and 4.

$$\frac{d\alpha}{dt} = (k_1 + k_2\alpha^m)(1-\alpha)^n$$

$$k_1 = A_1 \exp\left(-\frac{E_1}{RT}\right)$$

$$k_2 = A_2 \exp\left(-\frac{E_2}{RT}\right)$$

The viscosity is measured by parallel plate rheometer at different temperatures ramping rates (10, 20, 40, 60°C/min) and different shear rates (1, 2.5, 5, 10 s^{-1}), where the viscosity

Table I
Numerical Parameters Using Kamal's Relation and the Fitting Parameters for MUF Sample A

Parameter of kinetics	Unit	Value
M	N/A	5.0467 e−1
N	N/A	1.0207
A	s^{-1}	1.7751 e+3
B	s^{-1}	1.7746 e+5
T_a	K	7.0369 e+3
T_b	K	7.0372 e+3

Table II
Numerical Parameters for Cross Castro Macosko Model

	Unit	Value
n		9.683 e−2
τ^*	Dyne/cm^2	2.000 e+3
B	g/cm·sec	6.263 e−43
T_b	K	4.937 e+4
C_1		1.818
C_2		−5.521
α_g		0.25

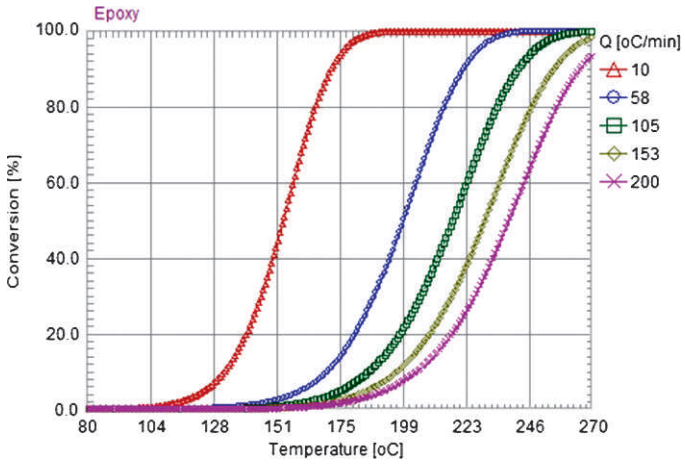


Fig. 3. Curing cinetics curves: conversion (%) vs. temperature.

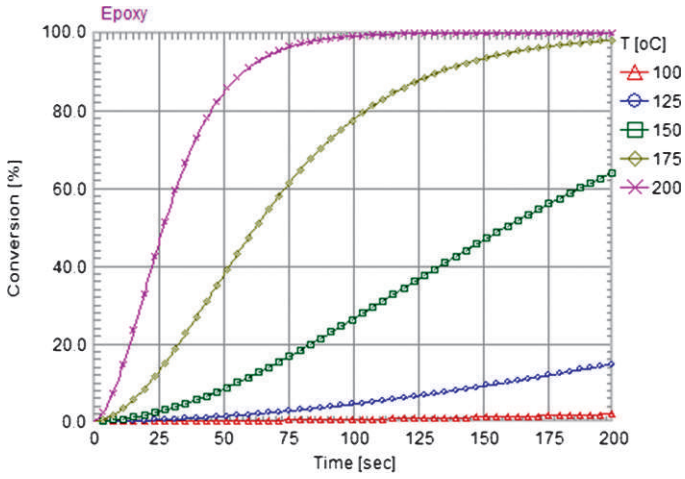


Fig. 4. Curing kinetics curves: conversion (%) vs. time.

changes with time. The measured viscosity is fitted by the Cross Castro Macosko model [7], summarized in Table II. The experimental data set and numerical fitting results with good agreement are shown in Figs. 5.

$$\eta = \frac{\eta_0}{1 + \left(\frac{\eta_0 \gamma}{\tau^*}\right)^{1-n}} \left(\frac{\alpha_g}{\alpha_g - \alpha}\right)^{c_1 + c_2 \alpha}$$

$$\eta_0 = Be^{\frac{T_b}{T}}$$

where γ is the shear rate, α is a conversion percentage, n is the power law index, η_0 is the zero shear viscosity, and τ^* is the

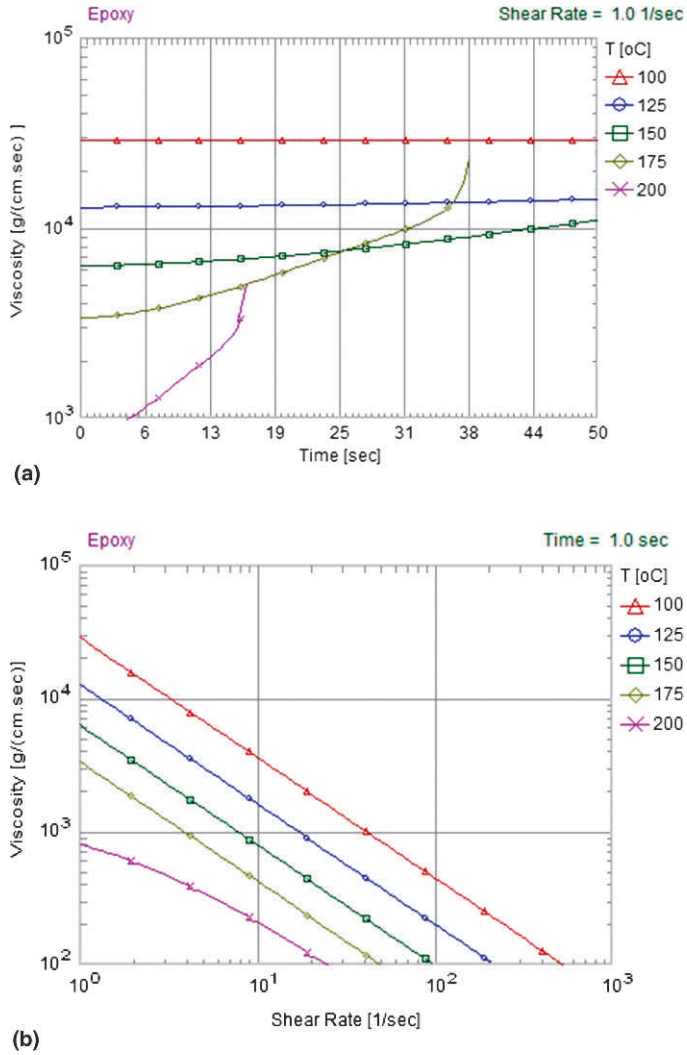


Fig. 5. Viscosity curves: (a) viscosity vs. time, (b) viscosity vs. shear rate.

parameter that describes the transition region between zero shear rate and the power law region of the viscosity curve.

MUF Flow Modeling and Experimental Benchmarking

A. Results for Flip Chip Test Vehicles

An illustration of the transfer molding of two selected flip chip devices for our current study is shown in Fig. 6 with

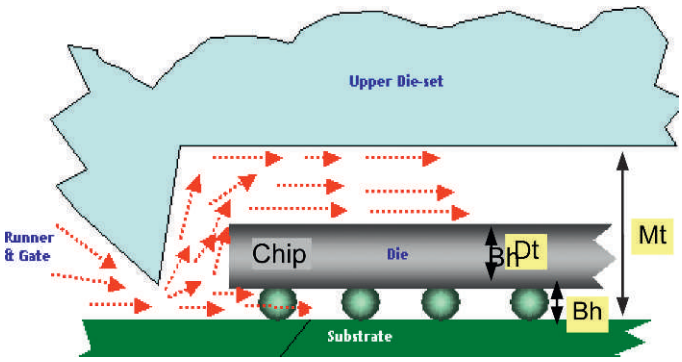


Fig. 6. Transfer molding of the selected flip chip devices.

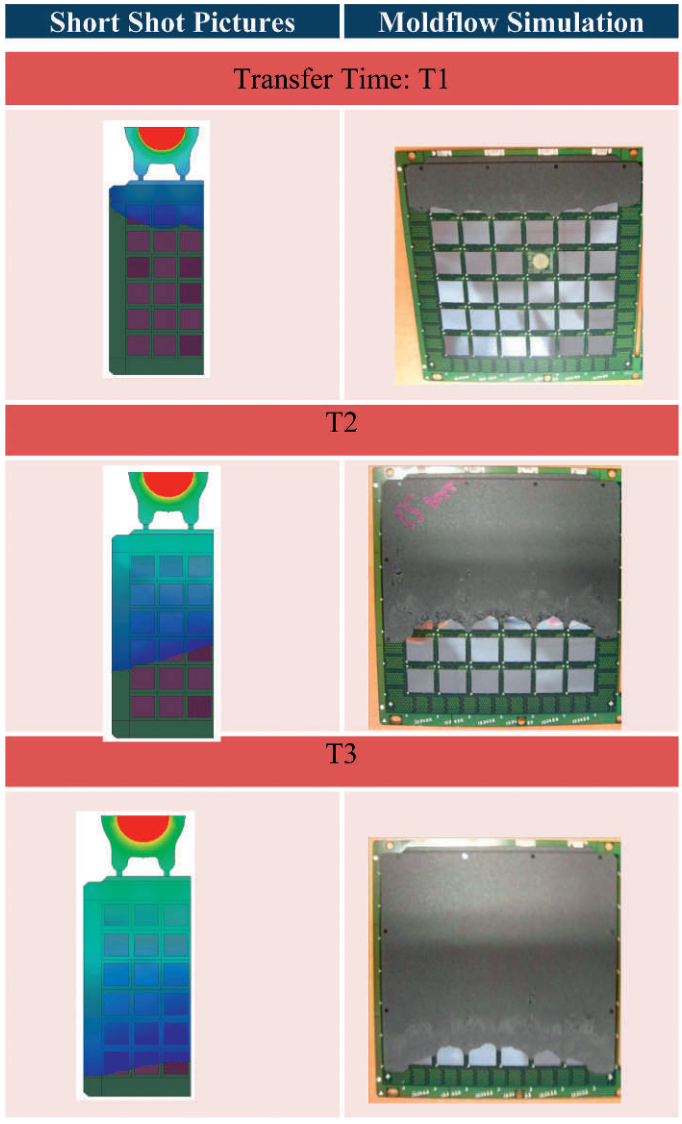


Fig. 7. Test vehicle 1, correlation between short shots and melt front simulations.

different package design and process conditions. For test vehicle 1, the die thickness (Dt) is 0.15 mm, the underfill gap between substrate and die (Bh) is 0.1 mm, and the total mold height (Mt) is 0.53 mm. For test vehicle 2, Dt = 0.15 mm, Bh = 0.09 mm, and Mt = 0.53 mm. There are at minimum three

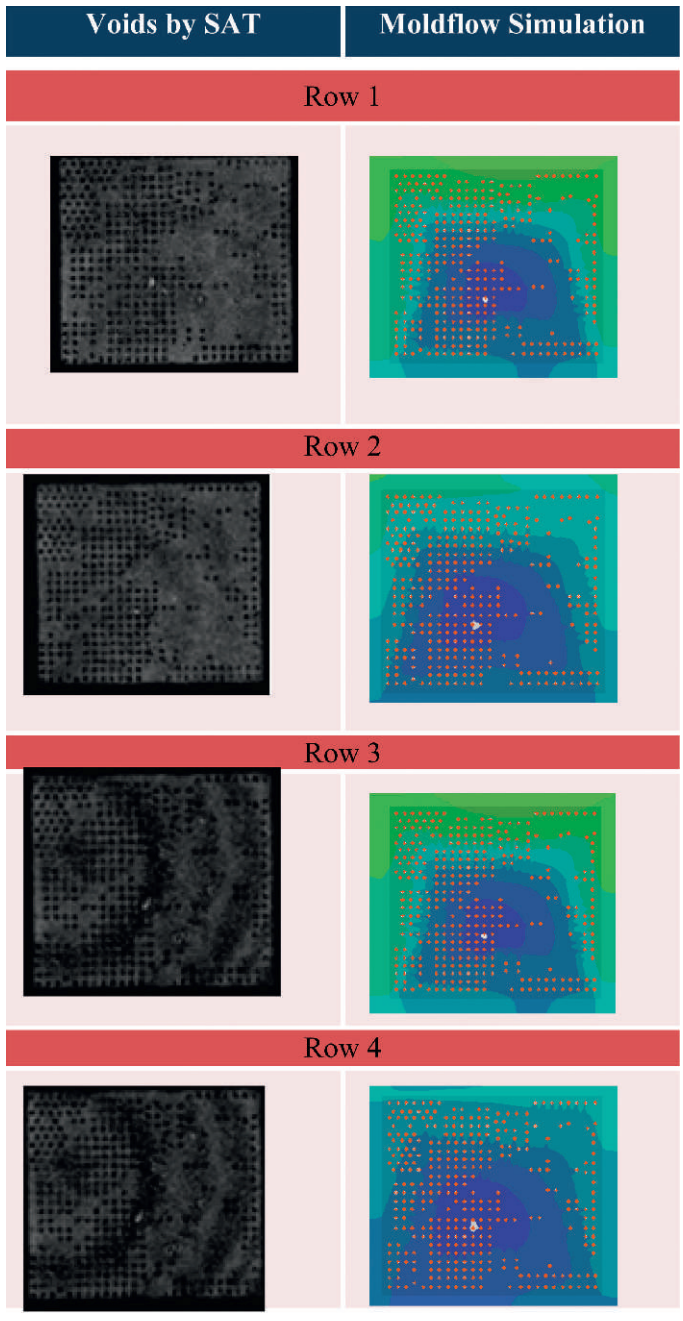


Fig. 8. Test vehicle 1, void correlations.

mesh elements between the smallest gaps in the model. The transfer time with optimum ram speed profile control was obtained from the mold process DOE. The transfer molding process simulation is conducted using the Moldex3D module for the IC molding process. Actual experimental data are used for both test vehicles in order to benchmark with our MUF flip chip transfer molding modeling.

For test vehicle 1, the experimental short shots and simulation results are compared to assess the melt front predictions. Fig. 7 shows the short shots of the mold process results captured during the mold process. The comparison shows good correlation of the melt fronts obtained by process short shots compared to the mold filling simulation, where the melt front

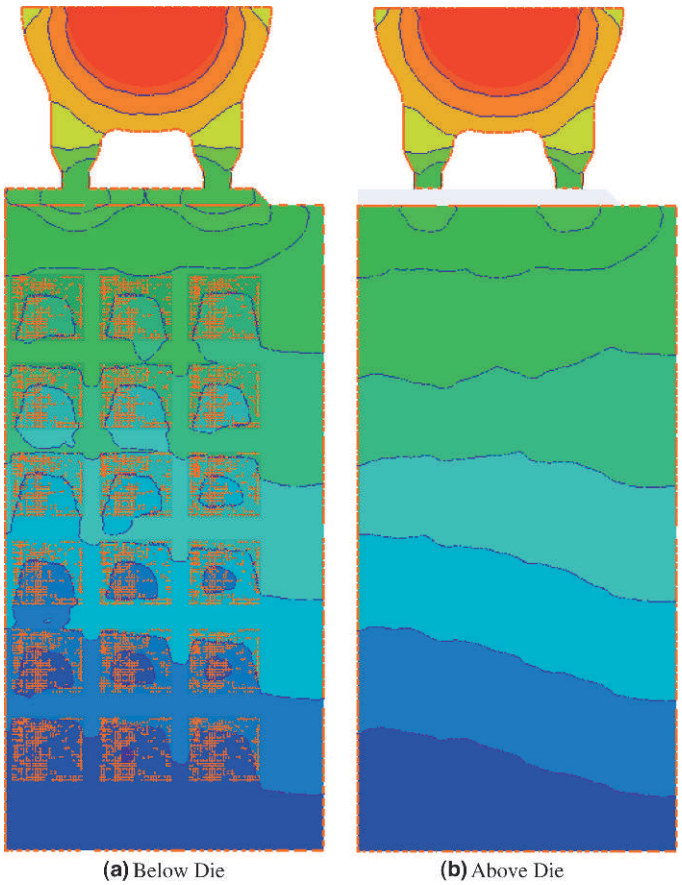


Fig. 9. Panel level melt front advancement contours.

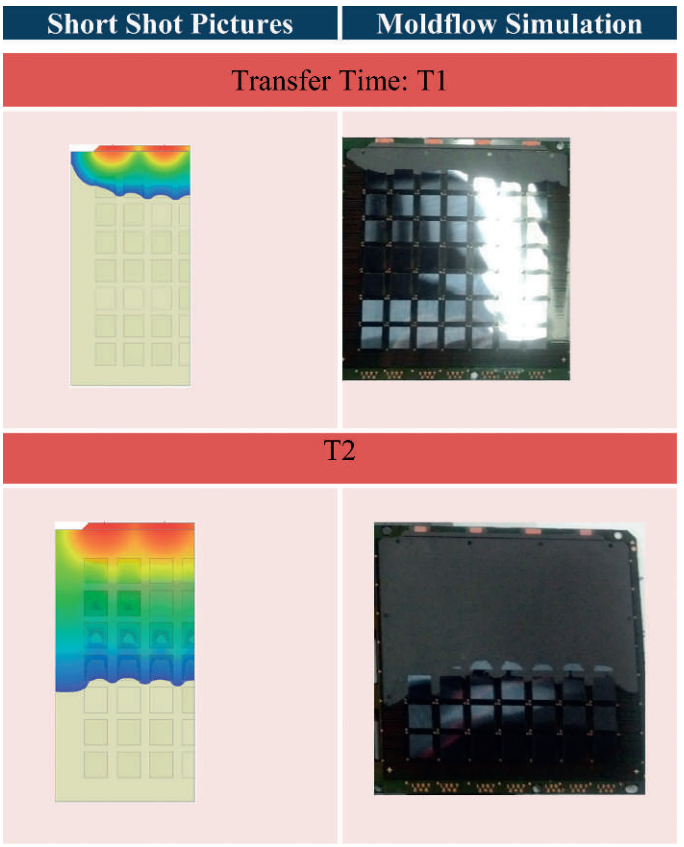


Fig. 10. Test vehicle 2, correlations between short shots and melt front simulations.

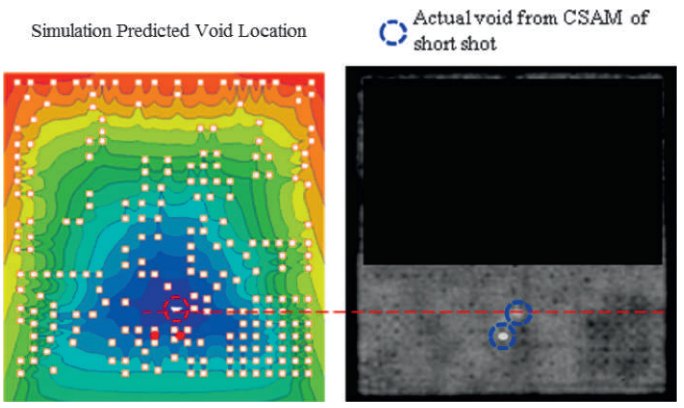


Fig. 11. Test vehicle 2, void correlation.

advancement patterns are similar to the simulated melt front contours. The melt front as observed from both short shots and simulations is generally balanced, except for a slight flow retardation observed on the area on top of the die due to flow resistance from the narrower flow channel.

The actual void location and size observed by experiment was captured by an SAT imaging machine. We can observe the entrapped voids in the underfill areas in selected packages on the different rows in the panel as shown in Fig. 8. The locations of the simulated and experimental void entrapments are nearly identical. Thus, the simulation showed good correlation with the actual void locations.

Fig. 9 shows the simulated melt front advancement contour results for both above and below the die with the flip chip bumps. Initially, the melt front of the mold top side and bottom side are similar, but due to the presence of bumps, the melt fronts above and below the die are separated. The melt front near the top side of the mold cavity is much faster than that of the bump area near the substrate side, where the 100 μm gap is much narrower than the usual 280 μm gap. For this test vehicle, it is observed that the void trapping phenomenon is more severe under the more densely bumped area, which is next to the much less densely bumped area. The flow imbalances due to the above factors are observed to be key factors of void entrapment where the two separated melt fronts merge.

For test vehicle 2, the experimental short shots and simulation results are also compared in Fig. 10 to assess the melt front predictions. The comparison showed generally good correlation of the melt fronts by process short shots with the mold simulation. The actual process short shots show a slightly faster melt front, which may be due to the higher vacuum applied on test vehicle 2 during the molding process. The results show that when vacuum levels are high, the effect of the vacuum on a simulated melt front has more impact.

Similarly, the actual void location and size from the experiment was captured by an SAT imaging machine. We can observe the entrapped voids in the underfill areas in selected packages on the different rows in the panel as shown in Fig. 11.

Consistent with prior study, the actual void location is within the ±5 bump pitch region from the predicted location. Closure and formation of actual voids in the experiment correlate well with the simulation.

Fig. 12 shows the simulated melt front advancement contour results for both above and below the die with the flip chip bumps. There is an imbalance melt front between the top and the bottom of the flip chip die.

Similarly, for this test vehicle, it is consistently observed that the void trapping phenomenon is more severe under a more densely bumped area below a less densely bumped area. The flow imbalances due to the above factors are observed to be key factors of void entrapment where the two separated melt fronts merge. This potentially results in air entrapment and potential formation of the void.

In addition to test vehicle 2, we observed different void shapes from the p-lap results as shown in Fig. 13. From the above analysis, we understand that voids are generally formed when the two separated melt fronts merge. Based on this key finding, we devised a systematic flow analysis matrix to identify the potential flow phenomena that may result in the different void shape formations. We analyzed various flow directions converging on four bumps, and we observed that due to mold flow hesitation around the bump area near the void location, different flow convergence configurations resulted in different void shapes, where the simulated void shapes and p-lap results are nearly identical. The results are summarized in Fig. 13, showing three different flow configurations and the resultant void shapes, and the p-lap results. The results show that the flow direction may be a potential cause of different void shapes, but the exact shape will be a result of several different factors.

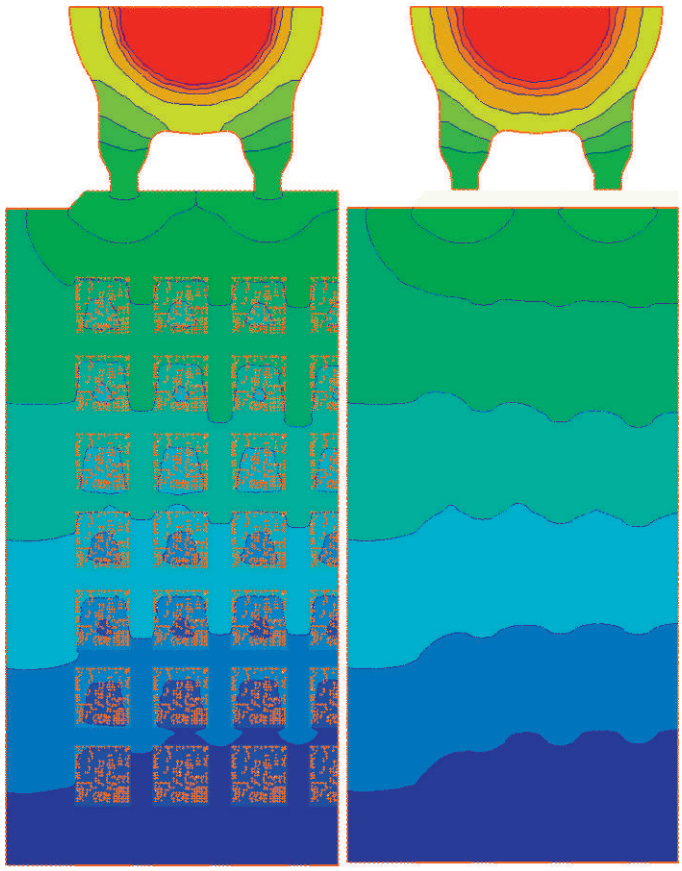


Fig. 12. Panel level melt front advancement contours.

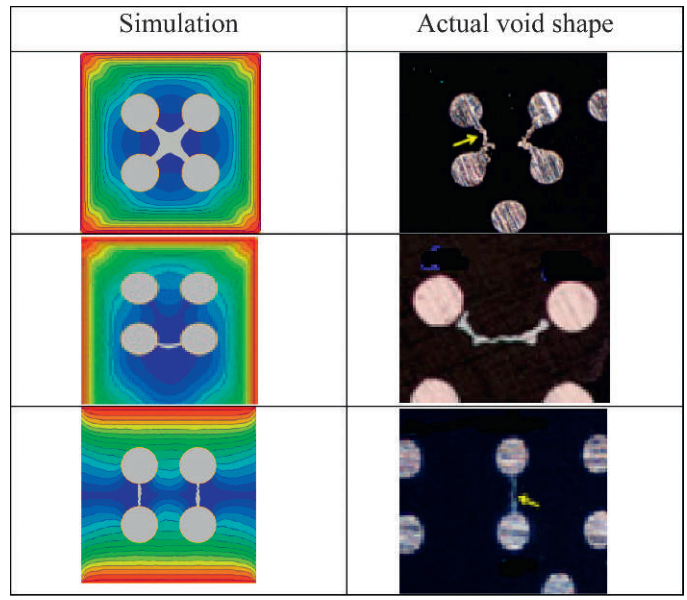


Fig. 13. Test vehicle 2, different flow configurations, resultant void shapes, and the p-lap results.

With the correlation of theoretical and actual phenomena, flow simulation enhances the understanding of the complex fluid dynamics during the molding process. With the successful validation of the simulations for both test vehicles, the simulation matrix as shown in Fig. 1 was then studied for a comprehensive assessment of the process, design, and material to enhance molding performance.

Systematic Evaluation of the Impact of Process and Design Parameters on Molding for a More Balanced Melt Front and to Minimize Void Issues

We developed a systematic approach to address the complex flow issues. As the full panel bumped array of flip chip devices would require high computational resources (~7 million meshes) compared to a chip level study (~500,000 meshes), an initial simplified chip level simulation is used to study the effect of

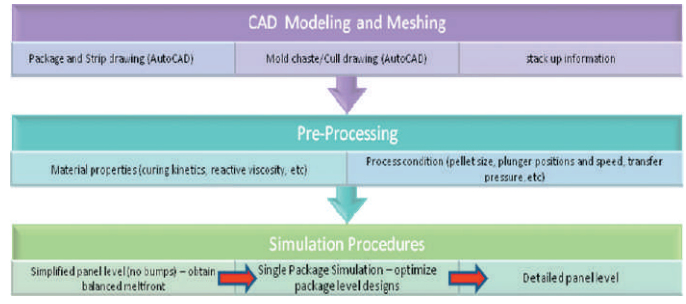


Fig. 14. Flowchart illustrating the systematic evaluation of the impact of process and design parameters on moldability using molding simulation tool Moldex3D.

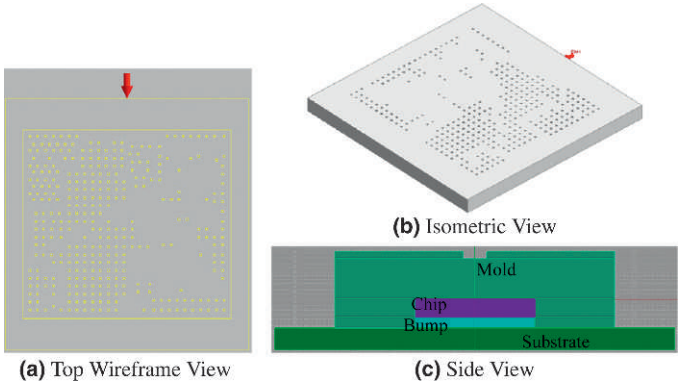


Fig. 15. Chip level simulation model.

various package-scale parameters. This analysis provides a prediction of the void location and an insight into key parameters to minimize the voiding problems, and overall to minimize the cycle time required to obtain the results. As the simulation for both test vehicles 1 and 2 are validated, we will use both test vehicles 1 and 2 to illustrate different aspects of systematic flow simulation methodology as shown in Fig. 14, to demonstrate different findings.

A. Chip Level Simulation

A simplified package 3D model with bumps is first created for an initial analysis as shown in Fig. 15, with the mold filling direction as indicated by the red arrow.

The process parameters such as filling time and mold cavity temperature are first varied to analyze the impact of process parameter change on molding performance using the molding simulation tool. The filling time was varied in the following two key ranges; 0.5 s, 1 s, 2 s (well below gel time) and 10 s, 20 s, 30 s (near gel time). The results, as shown in Fig. 16, show that when the filling time is varied in the range much lower than the MUF gel time, the change from 0.5 s to 2 s results in only minor impact on the void location. This may be due to the minimal variation in viscosity over this filling time range (Fig. 5) and hence only a minor impact on void locations is found. When the filling time is varied in the range near the MUF gel time, the void location varies, in this case shifting closer to the gate side. This could be due to the sharp change in viscosity near the gel time (Fig. 5) and with the rapid change in viscosity, a more significant impact on void location is observed. The results will vary based on the molding material used.

The mold temperature was varied in the following range: 130°C, 150°C, 170°C, 190°C, and 210°C. For this analysis, the filling time is 2 s. The results, as shown in Fig. 17, show that when the filling time is in a range much lower than the MUF gel time, the change from 130°C to 210°C results in only a minor impact on the void location. This may be due to the minimal change in viscosity over this the 2 s time period, even as the temperature changes from 130°C to 210°C. The results may vary with different materials and filling times used.

Next, the impact of different die thickness, keeping the bumps and total package height constant, was studied to determine the

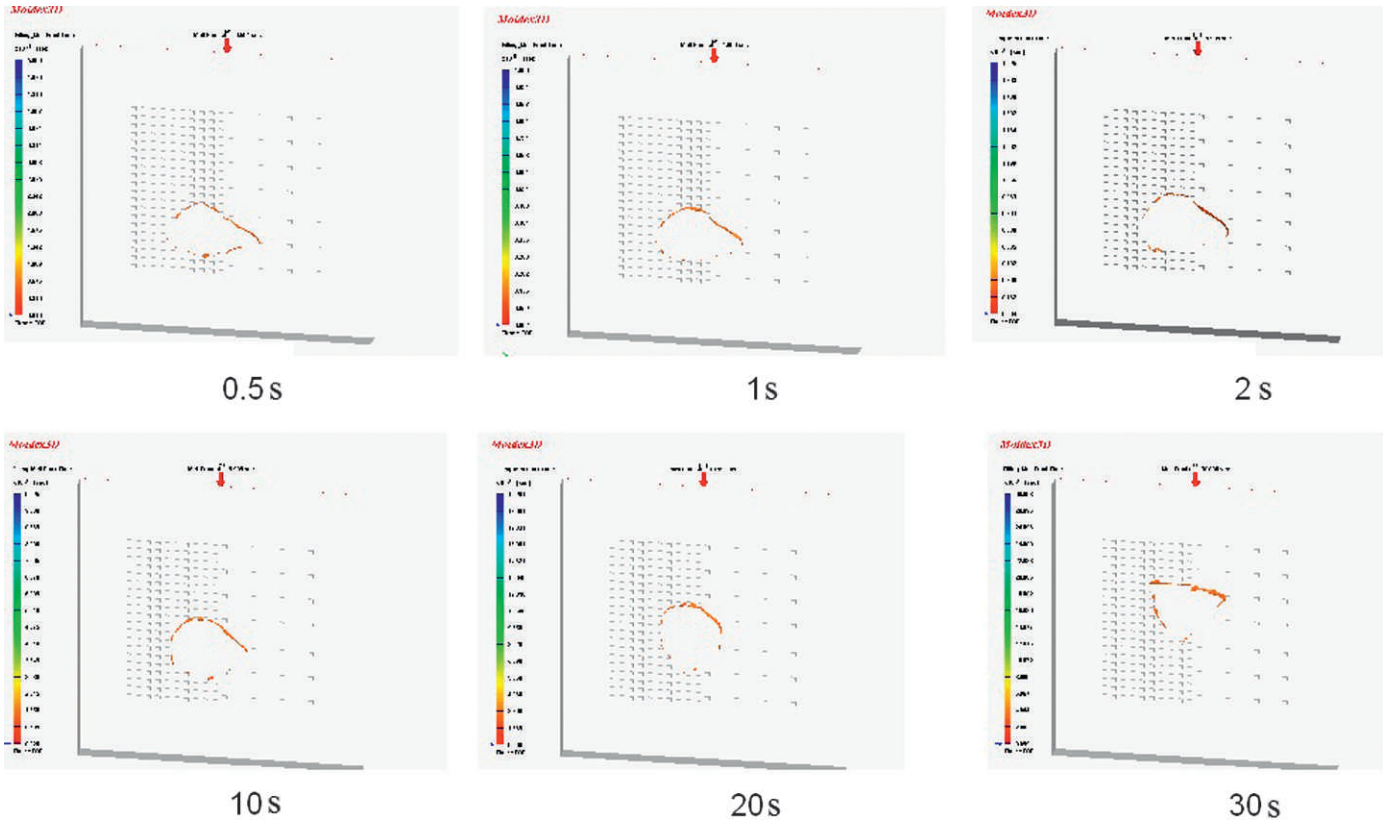


Fig. 16. Impact of filling time (s) on void location.

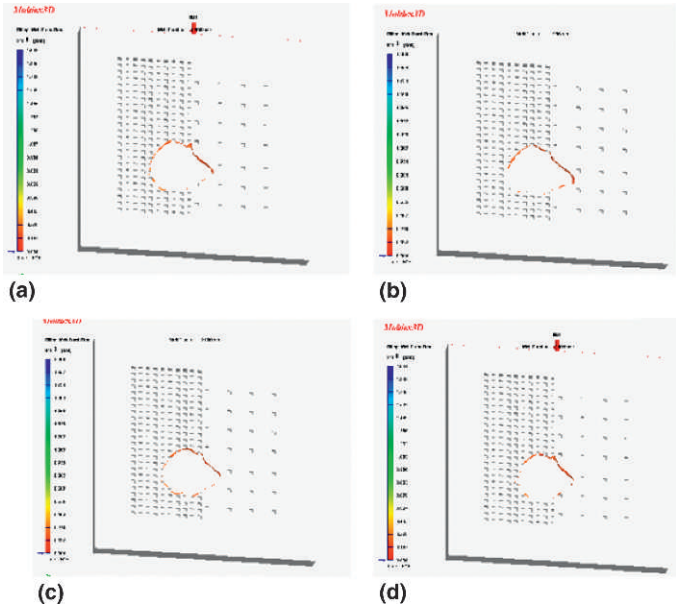


Fig. 17. Impact of mold temperature on void location, (a) 130°C, (b) 150°C, (c) 170°C, and (d) 190°C.

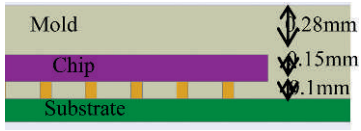


Fig. 18. Chip thickness of 0.15 mm.

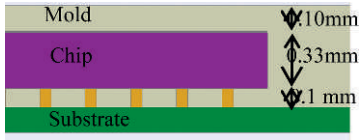


Fig. 19. Chip thickness of 0.33 mm.

impact of different gap sizes above and below the die on the melt front. As shown earlier in Fig. 9, initially, the melt front of the mold top side and bottom side are similar, but due to the presence of bumps, the layout, the difference in gap sizes between the die top and the mold cavity, and the bump height, the melt fronts above and below the die are separated. The melt front near the top side of the mold cavity moves much faster than that of the bump area near the substrate side. The preliminary results indicate that the flow imbalances are potential key factors of void entrapment at the location where the two separated melt fronts merge. Due to the clearance difference above and below the die, a greater flow lag is observed beneath the die. Our study investigates whether void issues can be ameliorated by reducing the flow imbalance. Hence, two different die thicknesses, as shown in Fig. 18 and Fig. 19, are studied to analyze the impact of different gap sizes above and below the die on the melt front.

The cross section planar cut is shown in Fig. 20 and the results of the cross sectional melt front advances for the thin and thick dies are shown in Fig. 21 and Fig. 22, respectively.

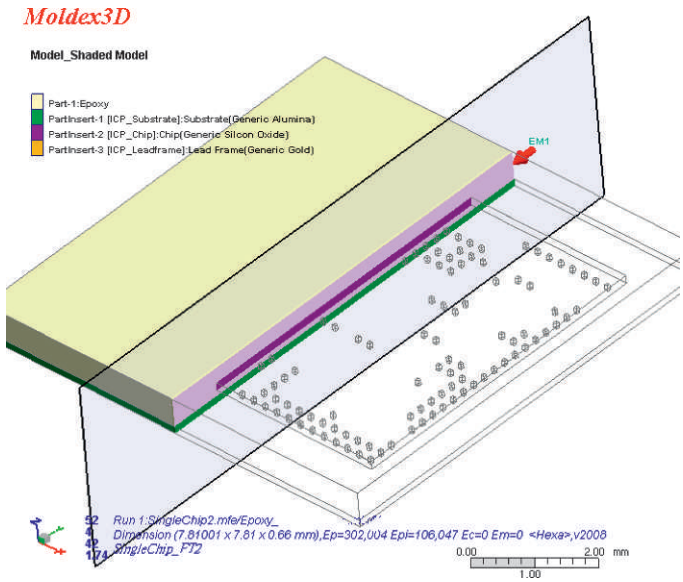


Fig. 20. Cross sectional planar cut for analysis.

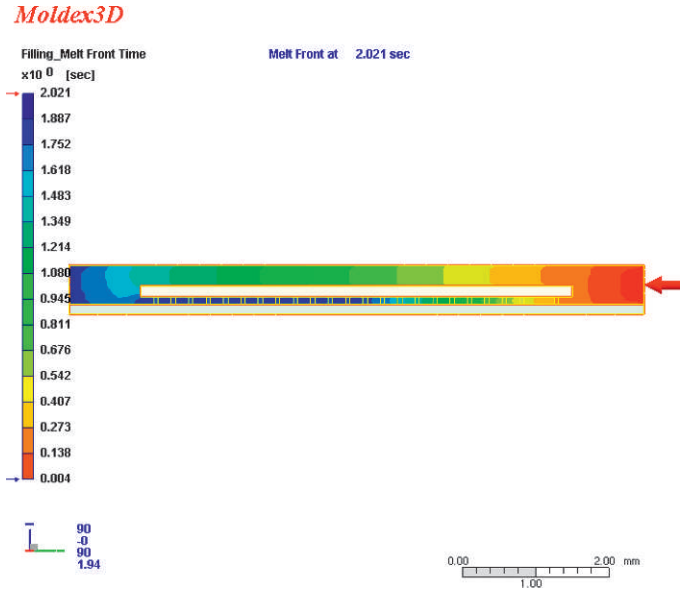


Fig. 21. Melt front profile for chip thickness of 0.15 mm.

The results show that balancing the flow resistance by decreasing the gap from the die top to the mold cavity resulted in a more balanced melt front above and below the dies, reducing the void issues caused where the two separated melt fronts merged.

We also varied the bump layout to analyze the impact of different bump pitch on the void locations, keeping the die thickness, bump height, and total package height constant. In Fig. 23, pitch array A has a denser bump area, with a pitch of approximately 0.1 mm and a less dense bump area with a pitch of approximately 0.6 m. The results, as shown in Fig. 24, indicate that the different bump layouts influence the location of void entrapment. With the denser bump area located next to the less dense bump area, the flow resistance caused by

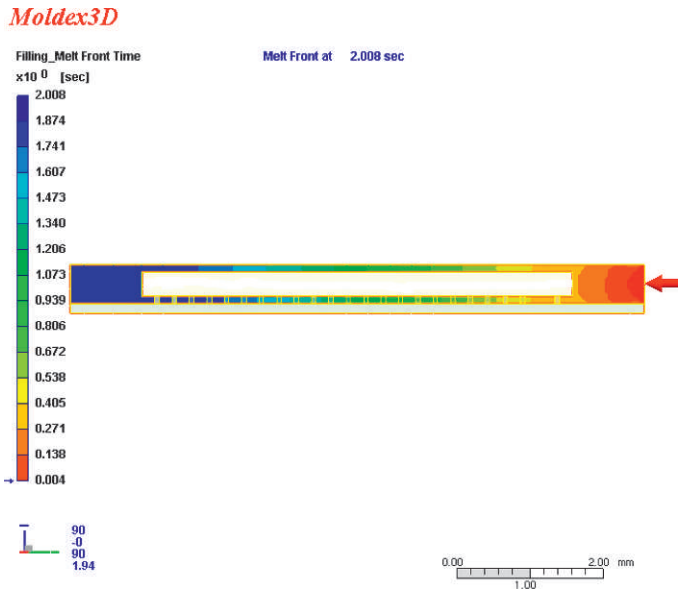
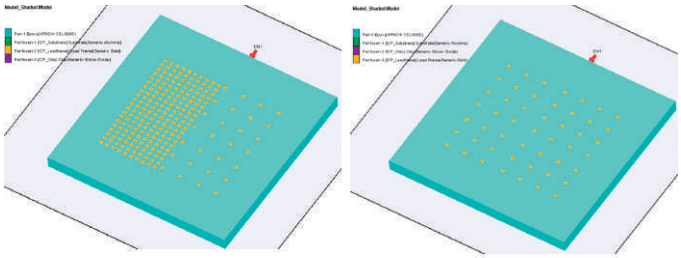
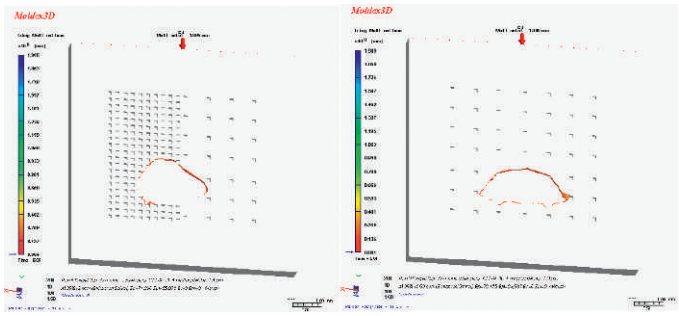


Fig. 22. Melt front profile for chip thickness of 0.33 mm.



(a) Pitch Array A **(b)** Pitch Array B

Fig. 23. Different bump layout simulation models.

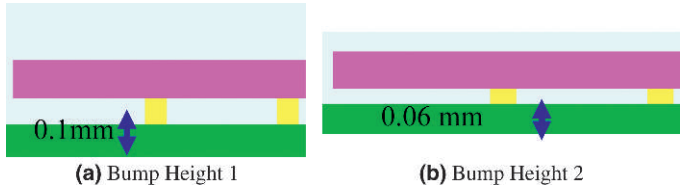


(a) Pitch Array A **(b)** Pitch Array B

Fig. 24. Void locations for different pitch arrays.

the denser bumps resulted in the shifting of void locations to the area with the denser bump layout. In comparison, when the bumps are evenly distributed, the void location is more centralized, though tending toward the vent side with higher viscosity values at the end of filling, which affects the void process.

The bump height is also varied to analyze the impact of different bump height on void location, keeping the die and mold thickness constant. As shown in Fig. 25, two different bump heights were evaluated; 0.1 mm and 0.06 mm. The bump layout used is pitch array A as shown in Fig 24a. The results, as



(a) Bump Height 1 **(b)** Bump Height 2

Fig. 25. Void locations for different bump weights.

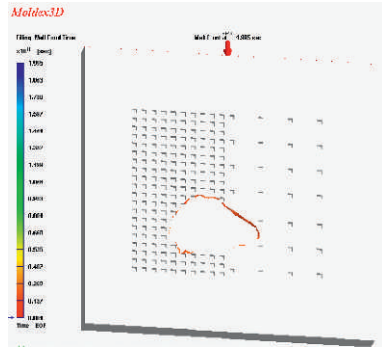


Fig. 26. Void location for bump height 1 (0.1 mm).

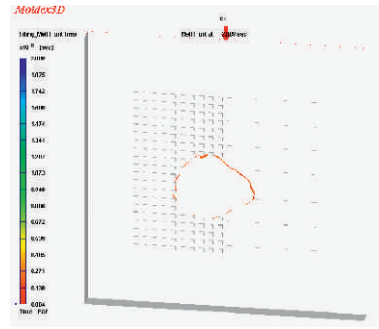


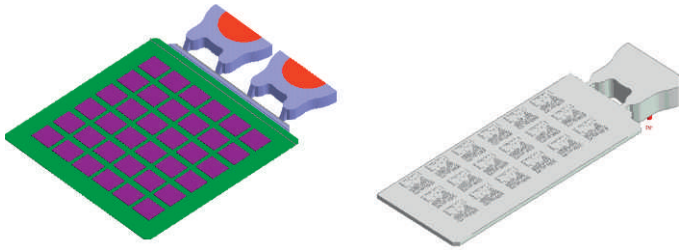
Fig. 27. Void location for bump height 2 (0.06 mm).

shown in Fig. 26 and Fig. 27, indicate that the bump height has an impact on the location of the entrapped voids. With the smaller bump height of 60 µm while keeping the other factors constant, the flow resistance of the bump area near the substrate side is increased compared to the larger smaller bump height of 100 µm. Hence, the melt front separation for the device with the smaller bump height of 60 µm above and beneath the die is more pronounced. The melt front near the top side of the mold cavity is much faster than that of the bump area near the substrate side when the bump height is smaller, resulting in voids trapped nearer to the gate side where the two separated melt fronts merge.

Using the insights provided by the preliminary study, the full panel level study is conducted next with the aim of obtaining a balanced melt front and minimizing voids in the most efficient way.

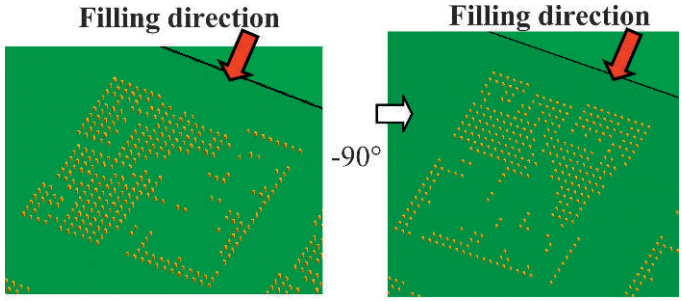
B. Panel Level Simulation

The panel level simulation model is shown in Fig. 28. The total number of finite element meshes used for the full panel 3D model for the current study is about 7 million, compared to



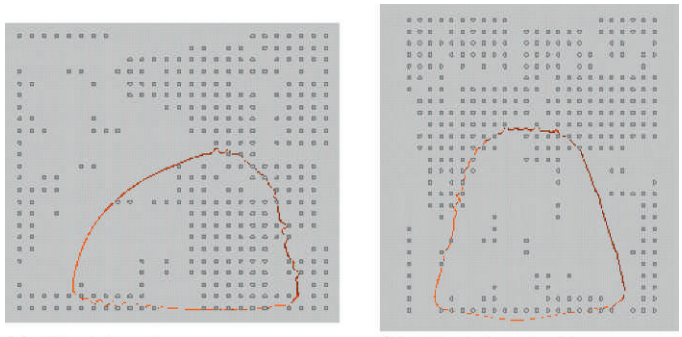
(a) Panel Solid Model **(b)** Panel Wire Frame Model

Fig. 28. Panel level simulation model, isometric view.



(a) Chip Orientation A **(b)** Chip Orientation A

Fig. 29. Panel level simulation model for different chip orientation.



(a) Chip Orientation A **(b)** Chip Orientation B

Fig. 30. Melt front on a package on the panel for different chip orientation.

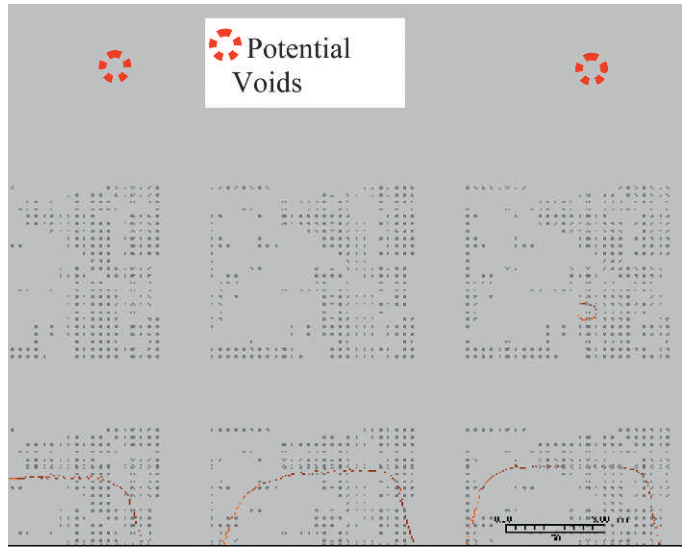


Fig. 31. Melt front on first two rows on the panel for chip orientation A.

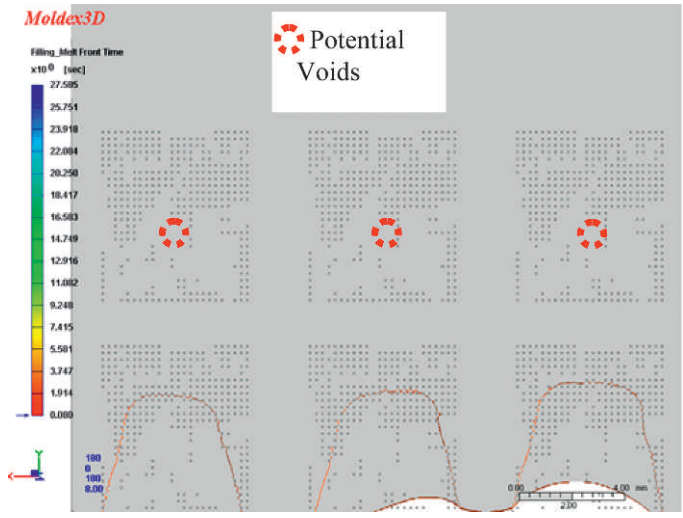


Fig. 32. Melt front on first two rows on the panel for chip orientation B.

500,000 meshes for the chip level study. An analysis was conducted to ensure that the trends for the single chip are representative of panel level studies for this selected test vehicle and conditions. From our findings, the identified trends of the single chip analysis are representative and insights useful for the subsequent full panel analysis for this test vehicle under the investigated conditions.

For the panel level analysis, we vary the chip orientation and study its impact on the void location for the test vehicle. Two different chip orientations were analyzed as shown in Fig. 29a and 29b.

The results of the two different chip orientations on the melt front advancements and potential void locations are shown in Fig. 30, Fig. 31, and Fig. 32. From the results, we observed that different chip orientation resulted in different mold filling trends. For chip orientation A, the denser bump area on the right resulted in higher flow resistance, where the melt fronts merged at the area of denser bumps, and the potential void location shifted toward the denser bump area. For chip orientation B, the denser bump area on top toward the gate side resulted in flow retardation at that area and melt fronts merged nearer to the center of the chip compared to chip orientation A where the voids are located nearer to the vent side. The results are also shown both for the panel view for both chip orientations as shown in Fig. 31 and Fig. 32.

C. Panel to Column Refined Mesh Simulation

To further enhance mold flow simulation capability, after identifying the potential main void areas, we further refine the mesh by zooming in from the panel level to single column level mold flow analysis as seen in Fig. 33. The key advantages of zooming in to single column are: (1) to reduce the computation requirement from a panel level mesh to a very fine column level; (2) to enhance the simulation to be able to predict the lower risk (secondary) voids (Fig. 34 shows a secondary void which is also seen in the actual experiment)

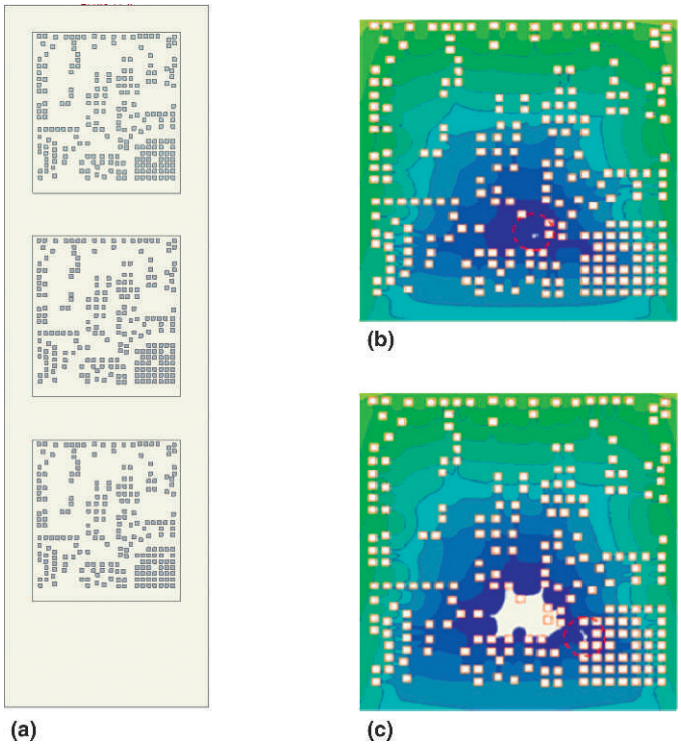


Fig. 33. (a) Column refined mesh model. (b) Primary potential void. (c) Secondary potential void.

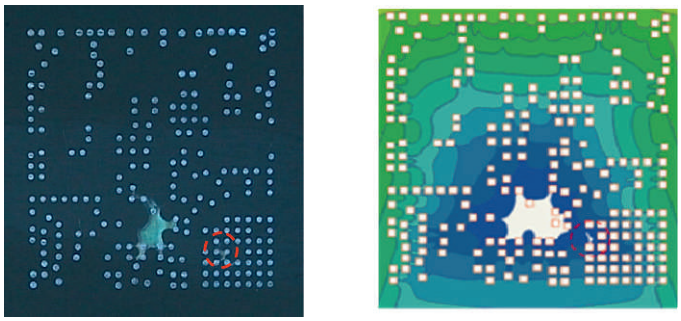


Fig. 34. Secondary potential void seen from experiment and simulation, highlighted in red.

because this methodology allows more accurate modeling of the actual package, such as the effect of bump diameter, among others; (3) to simplify the complexity, yet not overly simplified, as the column level model can include the effect of the entrance and the neighboring dies. This approach has enhanced the 3D mold flow simulation for better void location prediction capability. The panel level simulation can be used to study the main trend of the void location, while the single column model can be used to enhance the void prediction due to small geometry changes, such as bump size, among others.

Conclusions

This paper has demonstrated our 3D mold flow modeling capability of the transfer molding process for flip chip devices with MUF using Moldex3D V10. The full MUF rheokinetic behaviors and other material properties were characterized for the flow modeling. The full panel molding simulation was conducted and compared with actual void locations captured by an SAT machine and short shots. The mold filling simulation showed good correlation of the mold fronts obtained by process short shots and actual void locations. With the successful validation of the simulation capability, the tool is then applied to optimize design and process parameters to enhance flow balance, reduce voiding problems, and reduce device defects.

To address the complex flow issues with multiple interactive factors, we designed a systematic approach to tackle the problems. An initial simplified chip level simulation is used to provide insights on the key parameters to minimize the void problem. From the insights provided by the preliminary study, the full panel level study is conducted next to evaluate the impact of process and design parameters with the aim of obtaining a balanced melt front and minimizing voids. Such an approach will reduce the computational resources and total cycle time required to provide mold flow solutions.

From the rheokinetic flow modeling of the MUF process, we identified the key factors and secondary factors on void trapping simulation results from the extensive list of process and design parameters for this study; including filling time, mold temperature, different gap sizes above and below the die, bump pitch, bump layout, bump height, and chip orientation. These insights can be used as upfront guidelines to predict and reduce potential product defects and failures.

With consideration of process, materials, and design, we have demonstrated that mold flow simulation is an effective tool to reduce the design-to-implementation cycle time with identification of potential void and melt front imbalance issues. With our increasing range of flip chip products provided, we provide a comprehensive closed-loop solution including mold flow, materials, process, and thermal, mechanical, and electrical studies [3] to address the rising challenges faced with greater consumer demands for better performance and greater functionality.

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