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Die-Attach Technologies for Ultraviolet LED Multichip Module Based on Ceramic Substrate

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***Abstract*—A high power UV light emitting diode (LED) multichip module package based on aluminum nitride (AlN) and alumina (Al_2O_3) is presented. The AlN substrate with a high thermal conductivity of up to 180 W/(m·K) and LED chips based on a copper alloy provide superb thermal management and heat extraction. Efficient cooling is an important prerequisite for the increase of extractable optical power and for the reduction of thermally induced wavelength shift. A design of a stackable module featuring arrays of 7 × 2 indium-gallium-aluminum-nitride UV LED chips at 395 nm is developed. This configuration of submodules allows for the scalable assembly of line sources with different lengths. Applications using UV LEDs cover market segments such as curing of adhesives, inks, and coatings, sterilization of medical equipment, and treatment of potable water, as well as various uses in chemical detection, biochemical analytics, and spectroscopy.**

Thermal and thermomechanical modeling of the submount is conducted using finite element analysis. Die attach using eutectic gold-tin solder, lower melting tin-lead solder, and silver-filled adhesive are compared with respect to optical output power and wavelength drift. Mechanical strength and structure of the resulting joints are investigated using shear force measurements, cross-sectioning, and microtomography. An optical output power of 7.7 W is achieved using a cluster of 14 LED chips at 1050 mA, resulting in a peak irradiance of 33.9 W/cm^2 at the LED surface with respect to the footprint and pitch of the attached chips.

***Keywords*—Ceramic packaging, ceramics, solid state lighting, ultraviolet light emitting diode**

Introduction

UV sources are used in a wide variety of applications, such as the curing of adhesives, inks, coatings, and industrial paints, the sterilization of medical equipment, and the treatment of potable water. Furthermore, such light sources are needed for a variety of uses in chemical detection, biochemical analytics, and spectroscopy. Currently, high power mercury gas-discharge lamps are used to cover this wavelength range. Due to the high temperature of the discharge tubes and infrared (IR) radiation characteristics, such lamps find limited use in the processing of temperature-sensitive materials, for example, the curing of paints on plastics. Solid state light sources based on UV-LED offer a replacement for toxic mercury lamps, while providing additional benefits such as smaller form factor, increased lifetime and ruggedness, an application-tailored emission spectrum with reduced IR emissions, and added flexibility for UV applications [1, 2]. High power density UV-LED modules are currently under scientific investigation and commercial systems are entering the market. An Al_2O_3 based assembly using 98 densely packed LED chips is shown in [3]. Ceramic materials such as alumina, aluminum nitride, and even low temperature cofired ceramics (LTCC) can be used in high power packaging due to their high thermal conductivity [4]. These modules are particularly important for applications such as water and air disinfection, which need high power sources in the UVC range (100-280 nm) [5]. The focus of current research into solid state UV sources is on reducing the emission wavelength. The improvement of optical output power and external quantum efficiency are also of importance [6, 7]. Highly efficient light sources promise a significant contribution to global sustainable development due to energy savings, reduction in CO_2 emissions, and the elimination of pollutants such as mercury [8].

Efficient cooling is important for increasing extractable optical power and for minimizing thermally induced wavelength shift. Therefore, thin layer bonding techniques as well as reduced chip-die substrate thickness are ever more relevant to achieving these goals. [9]. Soldering processes can provide thin metallic bond layers with good thermal conductivity and high mechanical strength. Gold-tin solder alloys are used in opto-electronic packaging, die attach, and for the assembly of micro-optical systems [10, 11]. High temperature tin-based solder alloys with a high lead content and lead-free drop-in replacements such as BiAg are proposed for the assembly of power circuits [12]. Another die-attach technology is the use of microscale and nanoscale silver sinter materials to provide high-strength joints with outstanding electrical and thermal conductivity. Silver-sintering die-attach provides interconnects of semiconductor devices that are operable at high temperatures up to 350°C [13]. The reduction of bond pressure down to 2 MPa and temperatures down to 200°C, necessary for the processing of sensitive optoelectronic components, has been reported [14]. Thermo compression provides a simple yet high-temperature process for bonding of components. Thin and therefore highly thermally conductive bond layers are feasible [15].

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A new approach of die attach is reactive multilayer bonding using nanoscaled alternating layers of two materials. Foils or deposited films of nanoengineered materials can generate heat by a self-propagating exothermic reaction, allowing for a localized reflow of solder. Using this method, small and temperature-sensitive components can be joined without thermal or thermomechanical damage [16]. The high processing temperatures also allow for welding, and thus produce high shear strength joints [17]. Another state-of-the-art bonding technology for die attach is using silver-filled epoxy resins for which the filler particles provide thermal conductivity, while the epoxy generates adhesion bonding [18]. Current developments include nanoscaled filler materials to enhance the thermal conductivity of adhesives for packaging of high brightness LEDs [19]. Die-attach technologies for high temperature applications are an issue beyond solid state lighting. A review of materials for device interconnection technologies for high power electronics is given in [20].

The system presented utilizes a chip-on-board design to provide a multichip module package of high power UV-LED on ceramic substrates. LED chips in the UVA range (300-400 nm) are mounted on stackable aluminum nitride and alumina substrates. The goal of the project is an increase of optical output power by efficient cooling. Scalable design using submodules is advantageous for flexible and customer specific use. Die attach is conducted using eutectic gold-tin solder with flux-free processing, tin-lead solder, and two silver-loaded adhesives. The thermal behavior is determined by measurement of optical power and wavelength drift. Mechanical strength and microstructure are analyzed by shear force measurements, cross-sectioning, and microtomography.

Design

Based on the targeted areas of application, a design for a stackable multichip module is developed. This approach allows for the scalable assembly of line sources with different lengths as well as for the use of single modules for lighting systems. The suggested design offers flexible use in various applications. An array of 7 × 2 LED chips per submodule is designed to provide a line-shaped light source for homogenous illumination of a larger two-dimensional surface without complex beam shaping optics. Applications for this line-shaped source are the curing and polymerization of adhesives, inks, paints, and coatings in continuous processes. An alternate design of 3 × 2 LED chips per submodule is proposed for use as a UV light source for the homogeneous illumination of a digital mirror device (DMD). Such devices find application in the exposure of offset plates for offset printing. DMDs are capable of fast and cost-efficient manufacturing of offset plates in computer-to-plate (CTP) or computer-to-conventional-plate (CTCP) processes [21]. These techniques lead to reduced repress time and improved print quality.

A ceramic substrate (either alumina or aluminum nitride) is used as a mechanical system carrier, to provide electrical contact and to allow for proper thermal management and cooling of the LED chips. The substrate dimensions are 12 × 10 mm^2, with a thickness of 1 mm for aluminum nitride and 0.38 mm for alumina. The limits in substrate thickness were due to commercial availability, considerations of mechanical strength, and the surface quality necessary for thin film metallization and

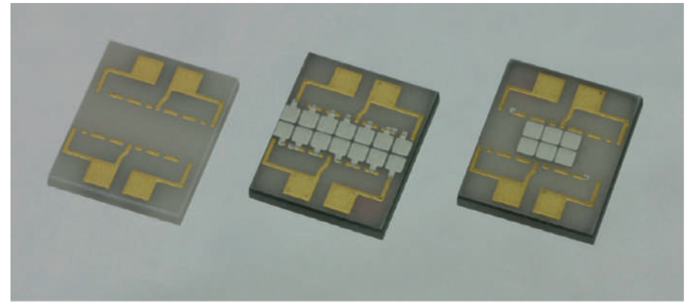

Fig. 1. Aluminum nitride substrates with electrical wiring and structured eutectic gold-tin solder layers in two design variants (7 × 2 LED chips and 3 × 2 LED chips).

thin film soldering. The electrical wiring and solder pads are manufactured directly onto the surface of the substrates. The wiring structures are manufactured thin film W/Ni/Pd/Au layers. Solder land pads with dimensions of 1100 × 1100 μm^2 with a spacing of 300 μm are shown on the substrate surfaces in Fig. 1. The pads are made of sputtered eutectic gold-tin (7 μm thickness) for soldering with gold-tin solder alloy [11]. Adhesive bonding and tin-lead soldering was conducted on a thin film layer stack of Ti (50 nm), FeNi (400 nm), and Au (600 nm).

UVA emitting indium-gallium-aluminum-nitride LED chips (SL-V-U40AC by Semiled Inc.) with a center wavelength of 395 nm, a chip size of 1070 × 1070 μm^2, and a rated typical optical output power of 210-250 mW are used. The initial design used for finite element (FE) analysis was based on NS375C-3SAA LED chips (Nitride Semiconductor Co., Ltd.) with a chip size of 600 × 600 μm^2, but was changed to the Semiled chip due to considerations of wavelength, optical output power, and availability. The Semiled chips are available with a back metal gold layer usable for soldering and adhesive bonding.

Electrical contacting of the front contact is conducted by ultrasonic assisted wedge-wedge wire bonding of Au and AlSi wires. Backside contacts are connected by the solder or the conductive adhesive to the wiring structures on the substrate. Submodules are mounted to a scalable and liquid-cooled heat sink by means of indium foil. The use of indium allows for a proper thermal contact and excellent cooling due to its high ductility and its high thermal conductivity of 82 W/(m·K).

Thermomechanical and Thermal Simulations

Based on the design data and the NS375C-3SAA LED chips, thermal and thermomechanical analyses are conducted by FE simulations. Thermomechanical analysis is used to evaluate the stresses due to different coefficients of thermal expansion of the substrate, LED chips, and joining material. Thermal analysis provides insight into the capability of the design and material selection on efficient heat removal from the chips. FE analysis is computed using ANSYS 11.0 SP1.

Targeted design goals were 80 mW and 100 mW optical output power. The LED chips achieve 80 mW optical at 200 mA, 4.5 V; and about 9.5% efficiency, resulting in a thermal load of 840 mW. An optical output of 100 mW was attained at 350 mA, at 5 V; with less than 6% efficiency, and a resulting thermal load of 1650 mW. A 1/4 model with symmetric boundary conditions was used for simulation. The base temperature of the substrate

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Table I
Material Properties for Simulation Model (Sources [22-24] and Respective Data Sheets)

Property Unit	λ W/K·m	TCE ppm/K	*E* GPa	ρ g/m^3
Al_2O_3	24	6.8	340	4.0
AlN	180	4.7	320	3.3
Sapphire	40	5.4[1]	430	4.0
Au80Sn20	58	16	59	14.7
Adhesive	17	30	1.21	3.2

[1] ⊥ C axis.

was set to 0°C and a natural convection with 10 W/(m^2·K) was applied to all outer surfaces. Table I shows relevant material properties used for the simulations. Additionally, the temperature dependency for Young's modulus, Poisson's ratio, and plasticity of the gold-tin solder were modeled.

Soldering was modeled using eutectic AuSn with a solder layer of 10 µm. Solidification of the solder alloy from solidus to room temperature leads to a shrinkage of about 5%. The resulting mechanical stresses within the solder layer are near the yield strength of the material, indicating plastic deformation of the solder. Maximum values of 320 MPa for AlN and 337 MPa for Al_2O_3 are calculated. Stresses within the base materials are computed to be 93 MPa for AlN and 95 MPa for Al_2O_3, which is significantly below the ultimate tensile stresses for these materials.

Thermal analysis modeling was conducted to provide the results of temperature distribution and heat flux within the subassemblies. For the design goal of 100 mW optical output power per chip and a thermal load of 1.65 W, chip temperatures were calculated to be 23 K above substrate temperature for AlN and 40 K above substrate temperature for Al_2O_3 using 10 µm AuSn solder layers (Fig. 2 and Fig. 3).

Calculations were repeated with respect to a conductive silver-loaded thermoplastic/thermoset adhesive with a thermal conductivity of 17 W/(m·K). The two assumed thicknesses of

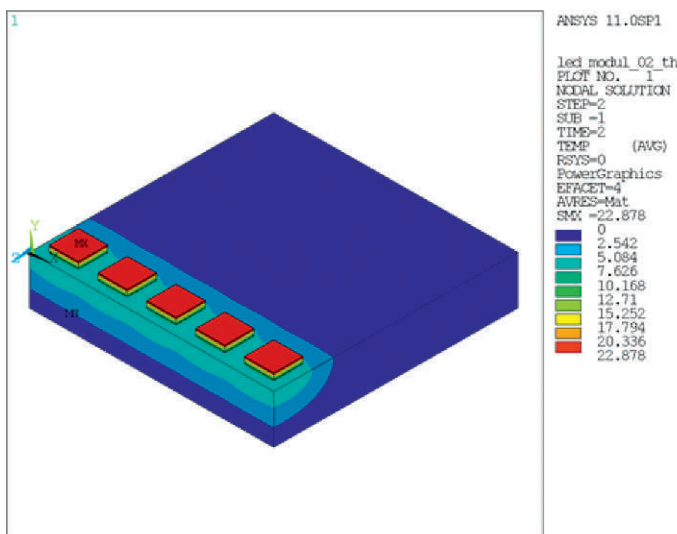

Fig. 2. Temperature distribution within LED chips and AlN substrate (thickness 1 mm) for eutectic AuSn solder (layer thickness 10 µm) and 1.65 W thermal load.

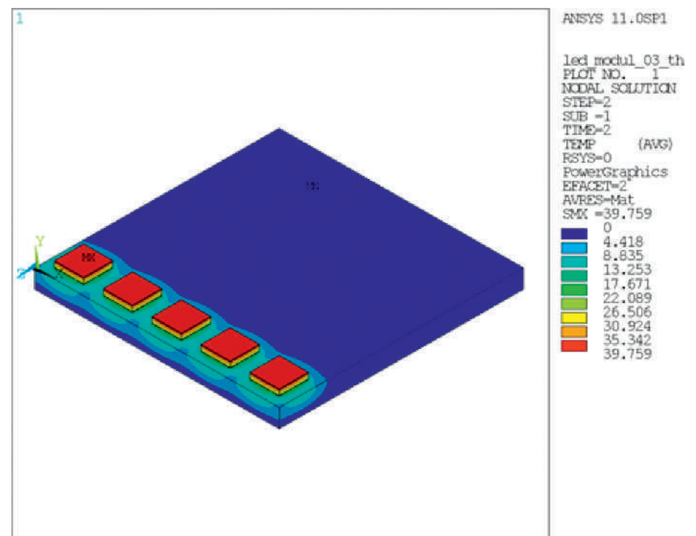

Fig. 3. Temperature distribution within LED chips and Al_2O_3 substrate (thickness 0.38 mm) for eutectic AuSn solder (layer thickness 10 µm) and 1.65 W thermal load.

the adhesive layers were 10 µm and 30 µm. The substrate material is Al_2O_3, with a thickness of 0.38 mm. Thermomechanical strain is mainly influenced by the base material and not the adhesive. Equivalent stresses were 43 MPa for both adhesive layer thicknesses. The stresses were significantly lower than for the solder attach, and thus below the ultimate tensile stresses of the substrate materials. Due to lower Young's modulus of the adhesive—1.2 GPa compared with 68 GPa for AuSn—the inherent stresses within the adhesive layers were significantly lower than within the solder. The results show equivalent stresses within the adhesive of 3.1 MPa for 10 µm layers and 2.6 MPa for 30 µm layers, respectively.

Thermal analysis for a thermal load of 1.65 W per chip results in chip temperatures of 42 K above substrate temperature for 10 µm layers and 47 K for 30 µm layers (see Fig. 4 and

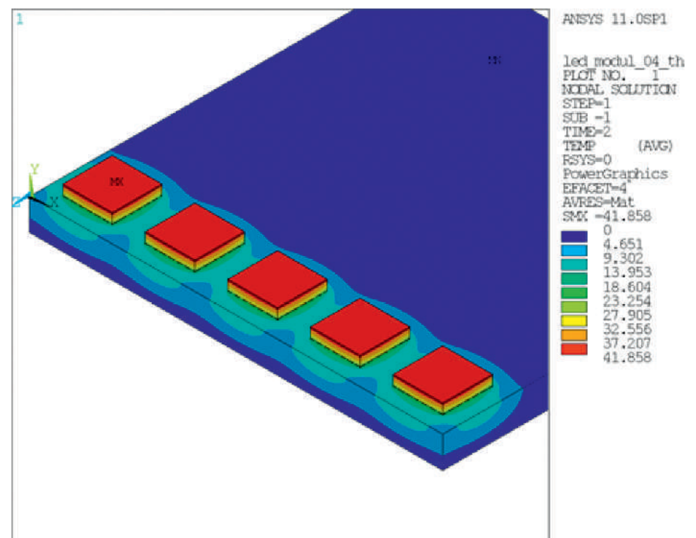

Fig. 4. Temperature distribution within LED chips and Al_2O_3 substrate (thickness 0.38 mm) for silver-filled adhesive (layer thickness 10 µm) and 1.65 W thermal load.

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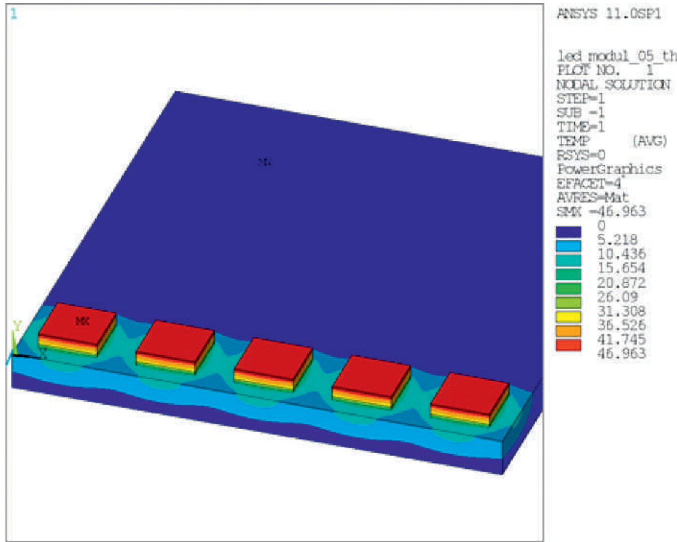

Fig. 5. Temperature distribution within LED chips and Al_2O_3 substrate (thickness 0.38 mm) for silver-filled adhesive (layer thickness 30 μm) and 1.65 W thermal load.

Fig. 5). These calculations indicate that a proper cooling of the chips may possibly be achieved using thermally conductive adhesives.

The comparison of chip temperatures (Table II) shows the significant influence of substrate material. Chip temperature is substantially lower using AlN substrates, even with a higher thickness. The results show that in the case of thin bonding layers (10 μm solder alloy or adhesive) thermal properties are mainly influenced by the chips and the substrate itself. There is only a modest increase in chip temperature of 5%, despite a 340% increase in thermal conductivity of the solder alloy compared with the adhesive.

The results of the FE calculations show acceptable thermomechanical stresses for both substrate materials and soldering with eutectic gold-tin. The thermal matching of sapphire based LED chips with AlN and Al_2O_3 keep the tensile stresses below the ultimate yield strength. The results allow the comparison of different die-attach technologies and can be transferred to other chip types.

Experimental Die Attach

Three different die-attach technologies were used: (1) eutectic gold-tin solder and flip-chip assembly, (2) standard vacuum reflow of a flux enhanced Sn63Pb37 solder (Fig. 6), and (3) two different silver-loaded adhesives. LED chips with a manufacturer-made gold metallization were used for SnPb soldering and adhesive attach.

Table II
Comparison of Chip Temperatures Depending on Substrate and Die Attach (AuSn Solder or Adhesive, Adh.)

Substrate	AlN 1 mm	Al_2O_3 380 μm	Al_2O_3 380 μm	Al_2O_3 380 μm
Die attach	AuSn 10 μm	AuSn 10 μm	Adh. 10 μm	Adh. 30 μm
ΔT	23 K	40 K	42 K	47 K

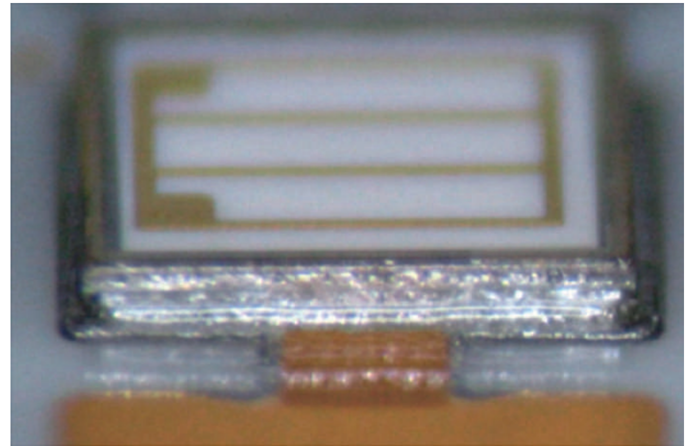

Fig. 6. LED chip soldered to an Al_2O_3 substrate.

Flip-chip assembly was conducted using a ficonTEC flip-chip bonder BL-2000 and a Finetech Fineplacer Lambda. Reflow during flip-chip placement is established by using a heated pick-up tool (PUT) and a hotplate with a substrate holder. The use of a substrate hotplate allows a stand-by temperature below solder alloy reflow and the subsequent placement and soldering of single chips by the PUT. Sputtered eutectic gold-tin is used for additional metallization of LED chips for flip-chip attach [11]. An optional increase of solder layer thickness was conducted by application of additional solder volume by means of solderjet bumping [25]. The process flow during flip-chip assembly follows these three steps: (1) application of solder layer (by physical layer deposition and solderjet bumping) to the LED chips and substrates, (2) pick and place of LED die with alignment of the chip with respect to the land pads on the substrate, and (3) reflow soldering by heating up the PUT and substrate hotplate under standard atmosphere.

The relevant process parameters were temperature profile and reflow regimen, as well as bonding force (applied pressure during placement and reflow). More than 30 assemblies using testing elements were manufactured for mechanical testing and process optimization. Soldering of chips using less than 10 μm sputtered AuSn layers (as-sputtered, without additional solder applied) did result in low shear forces, a large deviation in shear force between different lots, and irregular wetting. An additional 300 μm diameter solder sphere was applied to give an additional solder layer thickness of 12 μm. Fully operational 7 × 2 chip samples were made for optical testing (Fig. 7).

The process of vacuum reflow using SnPb solder follows the sequence: (1) dispensing of flux-containing solder paste at the land pads on the substrate, (2) placement of LED dice, and (3)

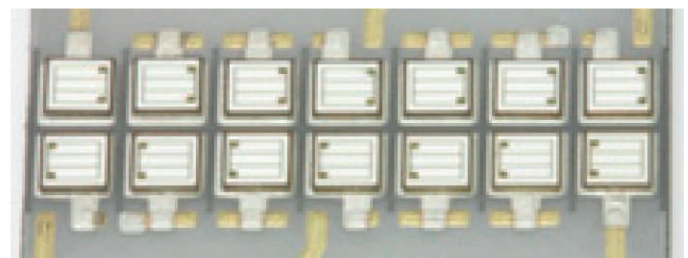

Fig. 7. Fully assembled 7 × 2 UV-LED module.

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vacuum assisted reflow soldering. The applied vacuum during reflow of below 50 mbar during liquidus of the solder is designed to assist the formation of void-free or void-less solder joints. Process parameterization was done with respect to the reflow profile, that is,temperature and ramp-up. The reflow was conducted at a peak temperature of 195°C, about 12 K beyond the liquidus of the solder (183°C).

The third die-attach technology used is adhesive bonding with silver-loaded and highly thermally conductive adhesives. The adhesive was provided by a direct dispense station. The process run is as follows: (1) picking of the LED die, (2) dipping the component into the adhesive reservoir of the direct dispense station, (3) placement of the LED onto the substrate, and (4) curing of the adhesive at 120°C for 15 min. The direct dispensing technique allows uniform layers of properly homogenized adhesive with a thickness adjusted by a height-adjustable stencil. Layer thickness is limited by particle agglutination of the filler material and the high viscosity during dispensing.

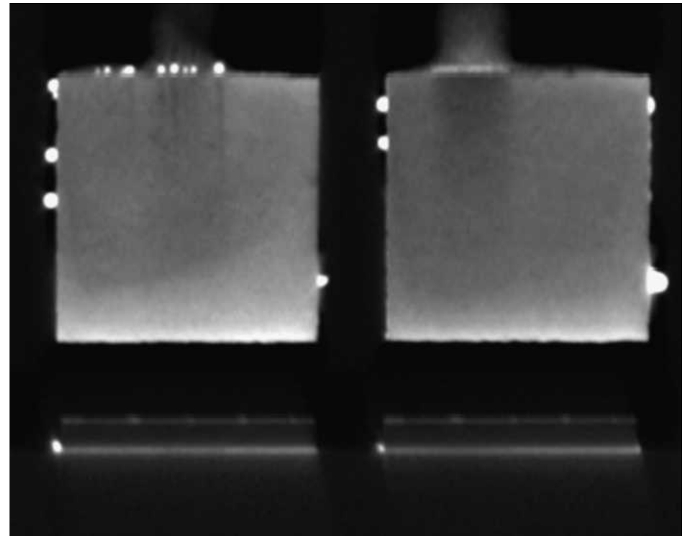

Fig. 9. MicroCT of AuSn soldered LED chips.

Experimental Analysis of Solder Joints

Mechanical testing of soldered components, both LED chips and equally sized testing vehicles (glass coupons) was conducted using shear force measurements. Using components with an additional solder volume, 6 N to 18 N of shear force with glass testing elements for variation of process parameters were achieved. LED chips show a shear force greater than 10 N with the main failure mode being the rupture of chips rather than failure of solder joints or layer interfaces.

Cross section views (Fig. 8) show a homogenous, near void-free filling and a solder layer thickness below 30 μm. Microcomputer tomography (MicroCT) analysis with a voxel size of 5 μm confirms a void-free and homogenous solder layer for AuSn soldering (Fig. 9). In comparison, the MicroCT shows significant voiding for the SnPb soldered LED chips despite the applied vacuum (Fig 10). The solder paste contains high amounts organic content—including binding agents, flux, thixotropic agents, and solvents. These organic compounds cannot be extracted from the joint completely, due to the disadvantageous aspect ratio of solder area ($1070 \times 1070\ \mu m^2$) versus layer thickness (30 μm). A higher fraction of voids reduces the equivalent area available to heat transfer by conduction. Using image processing of MicroCT pictures and analysis by histogram, a typical void fraction of 31% for the SnPb soldered samples is found. Flux-free processing of gold-tin solder further eliminates the need for additional cleaning after soldering.

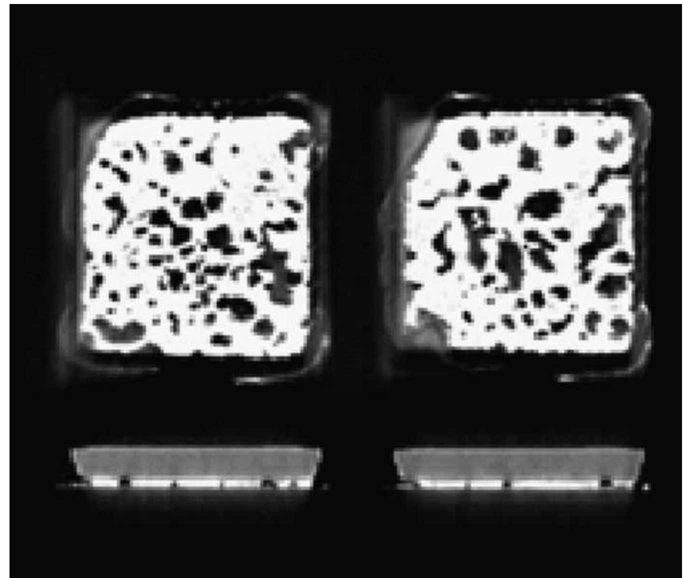

Fig. 10. MicroCT of SnPb soldered LED chips.

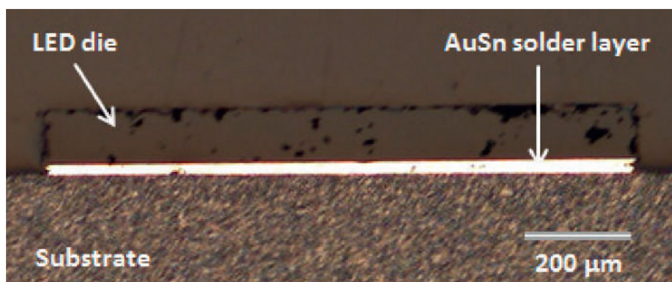

Fig. 8. Cross sectional view of a AuSn soldered LED chip.

Optical Measurements

Optical power measurements and wavelength shift were observed using an integrating sphere. A setup of an Ulbricht sphere that allows for the mounting of the proposed ceramic substrates attached to a heat sink was constructed. This structure permits the operation of the LED chips at high power ratings while diffusing the light for an integrating measurement of total power without concern for the directional characteristics of the LED assembly. The design of the heat sink and substrate clamping lead to approximately 30% NA loss during measurements. Calibration of the Ulbricht sphere was done

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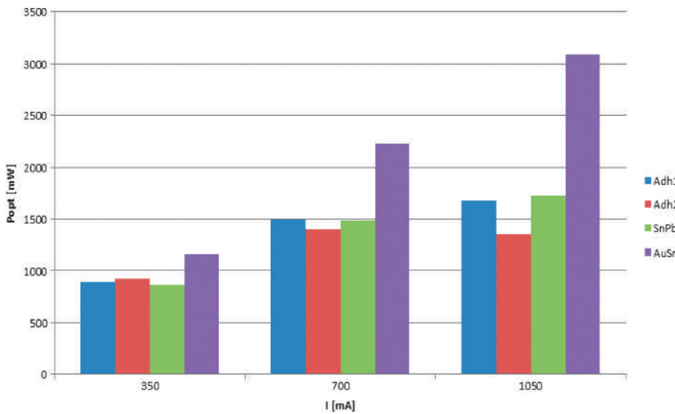

Fig. 11. Optical output power of one channel (1 × 7 chips) for four die-attach variants.

using a reference photo diode with known spectral sensitivity and a reference laser with known emission wavelength and optical output power to correct the results for the NA loss.

The results of optical output power of the four die-attach variants—adhesive 1 (four samples), adhesive 2 (four samples), SnPb solder (two samples), and AuSn solder (eight samples)—are shown in Fig. 11. Optical measurements were conducted on assemblies with SL-V-U40AC by Semiled Inc. using one channel of 1 × 7 chips per substrate and for operational currents of 350 mA, 700 mA, and 1050 mA. A significant improvement of output power was observed for AuSn die-attach. Adhesive 2 shows a decrease of output power with increased current.

Using both channels of 2 × 7 chips, an optical output power of 7.7 W was achieved at 1050 mA for AuSn soldered assemblies. The resulting peak irradiance was 33.9 W/cm^2 at the LED surface with respect to the footprint and pitch of the attached chips. The necessary spacing between the chips leads to a resulting fill factor of 70.5% that was taken into account for calculation of irradiance. The optimized cooling of AuSn-soldered LED chips was demonstrated by the significantly increased optical output power compared with adhesively joined LEDs (Fig. 12).

Additionally, the thermally induced shift of emission wavelength can be used to compare different die-attach technologies with respect to thermal transfer capabilities. Better cooling corresponds to a lower chip temperature and thus to a lower

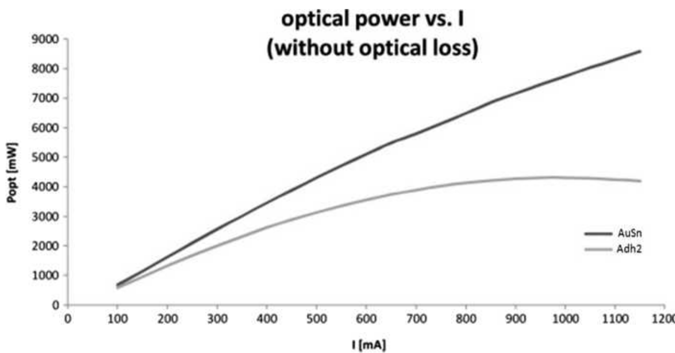

Fig. 12. Optical output power of both channels (2 × 7 chips) for the gold-tin solder (AuSn) and adhesive (Adh2) die attach.

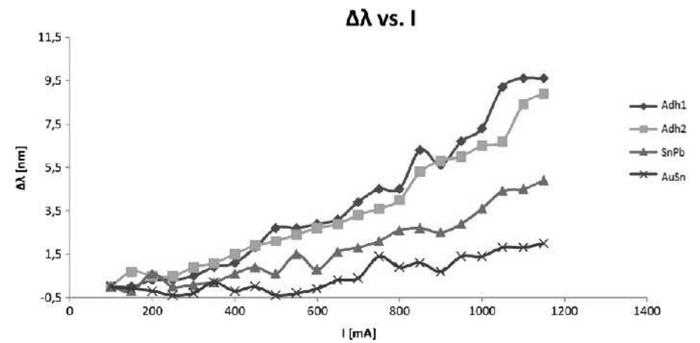

Fig. 13. Wavelength shift over current for four die-attach variants.

wavelength shift. Both soldering techniques show improved behavior compared with the adhesives (Fig. 13). Gold-tin solder layers show a lower drift than the SnPb solder. This effect could be attributed to the significantly higher void ratio.

Summary and Outlook

The assembly of a UV-LED multichip module using different die-attach technologies has been demonstrated. FE analysis determined acceptable thermomechanical stresses and the realization of highly thermally conductive joints using solder alloys and new highly conductive silver-loaded adhesives. Measurements of the thermal resistance and inclusion of such values in FE analysis could further improve the predictions made by thermal simulations.

The design of a multichip submodule is flexible and versatile to use. Line-shaped light sources are achievable by stackable modules. A six-module assembly is demonstrated. Easy scaling of optical output power as well as a simplified servicing by changing single modules are benefits to the consumer. Measurement of optical output power and low thermally induced wavelength drift as well as analysis of solder layer structure show the superior performance of thin gold-tin solder layers. A 14 chip module attains 7.7 W optical output power and a respective peak irradiance of 33.9 W/cm^2. The module-based approach offers a higher fill factor and a better thermal coupling than the placement of individually housed light sources on a PCB. Long-term behavior and the investigation of reliability over the full lifetime are the next steps to confirm the usability of the proposed module design and die-attach technologies.

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References

[1] M.S. Shur and R. Gaska, “Deep-ultraviolet light-emitting diodes,” *IEEE Transactions on Electron Devices*, Vol. 57, No. 1, pp. 12-25, 2009.

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[2] S.L. McDermott, J.E. Walsh, and R.G. Howard, “A comparison of the emission characteristics of UV-LEDs and fluorescent lamps for polymerisation applications,” *Optics and Laser Technology*, Vol. 40, No. 3, pp. 487-493, 2008.

[3] M. Schneider, C. Herbold, K. Messerschmidt, K. Trampert, and J.J. Brandner, “High power UV-LED-clusters on ceramic substrates,” Proceedings of the 60th Electronic Components and Technology Conference (ECTC), pp. 679-685, 2010.

[4] J.K. Park, H.D. Shin, Y.S. Park, S.Y. Park, K.P. Hong, and B.M. Kim, “A suggestion for high power LED package based on LTCC,” Proceedings of the 56th Electronic Components and Technology Conference (ECTC), 2006.

[5] M.A. Würtele, T. Kolbe, M. Lipsz, A. Külberg, M. Weyers, M. Kneisel, and M. Jekel, “Application of GaN-based ultraviolet-C light emitting diodes, UV LEDS, for water disinfection,” *Water Research*, Vol. 45, No. 3, pp. 1481-1489, 2011.

[6] Y. Liao, C.Thomidis, C. Kao, and T.D. Moustakas, “AlGaN based deep ultraviolet light emitting diodes with high internal quantum efficiency grown by molecular beam epitaxy,” *Applied Physics Letters*, Vol. 98, No. 081110, 2011.

[7] M. Kneisel, T. Kolbe, C. Chua, V. Kueller, N. Lobo, J. Stellmach, A. Knauer, H. Rodriguez, S. Einfeldt, Z. Yang, N.M. Johnson, and M. Weyers, “Advances in group III-nitride-based deep UV light-emitting diode technology,” *Semiconductor Science and Technology*, Vol. 26, p. 014036, 2011.

[8] J.K. Kim and E.F. Schubert, “Transcending the replacement paradigm of solid-state lighting,” *Optics Express*, Vol. 16, No. 26, pp. 21835-21842, 2008.

[9] K.T. Lam, S.C. Hung, C.F. Shen, C.H. Liu, Y.X. Sun, and S.J. Chang, “Effects of the sapphire substrate thickness on the performances of GaN-based LEDs,” *Semiconductor Science and Technology*, Vol. 24, No. 6, p. 065002, 2009.

[10] R.W. Chuang, D. Kim, J. Park, and C.C. Lee, “A fluxless process of producing tin-rich gold-tin joints in air,” *IEEE Transactions on Components and Packaging Technologies*, Vol. 27, No. 1, pp. 177-181, 2004.

[11] H. Banse, R. Eberhardt, E. Beckert, and W. Stöckl, “Laser beam soldering—A new assembly technology for microoptical systems,” *Microsystem Technologies*, Vol. 11, No. 2/3, pp. 186-193, 2005.

[12] M. Rettenmayr, P. Lambracht, B. Kempf, and M. Graff, “High melting Pb-free solder alloys for die-attach applications,” *Advanced Engineering Materials*, Vol. 7, No. 10, pp. 965-969, 2005.

[13] L. Guo-Quan, J.N. Calata, Z. Zhiye, and J.G. Bai, “A lead-free, low-temperature sintering die-attach technique for high-performance and high-temperature packaging,” Proceedings of the 6th IEEE CPMT Conference on High Density Microsystems Design and Packaging and Component Failure Analysis, pp. 42-46, 2004.

[14] W. Schmitt, “New silver contact pastes from high pressure sintering to low pressure sintering,” Proceedings of the Electronic System-Integration Technology Conference (ESTC), pp. 1-6, 2010.

[15] T. Aalto, M. Harjanne, M. Kapulainen, S. Ylinen, J. Ollila, V. Vilokkinen, L. Mörl, M. Möhrle, and R. Hamelin, “Integration of InP-based optoelectronics with silicon waveguides,” *Proceedings of the SPIE*, Vol. 7218, No. 72180O, pp. 1-14, 2009.

[16] G. Caswell, “NanoBond® assembly—A rapid, room temperature soldering process,” Proceedings of the European Microelectronics and Packaging Conference, EMPC, 2009.

[17] A.J. Swiston, Jr., T.C. Hufnagel, and T.P. Weihs, “Joining bulk metallic glass using reactive multilayer foils,” *Scripta Materialia*, Vol. 48, No. 12, pp. 1575-1580, 2003.

[18] S.K. Kang, R.S. Rai, and S. Purushothaman, “Development of high conductivity lead (Pb)-free conducting adhesives,” *IEEE Transactions on Components, Packaging, and Manufacturing Technology A*, Vol. 21, No. 1, pp. 18-22, 1998.

[19] D. Lu, C. Liu, X. Lang, B. Wang, Z. Li, W.M.P. Lee, and S.W.R. Lee, “Enhancement of thermal conductivity of die attach adhesives (DAAs) using nanomaterials for high brightness light-emitting diode (HBLED),” Proceedings of the 61st Electronic Components and Technology Conference (ECTC), 2011.

[20] V.R. Manikam and K.Y. Cheong, “Die attach materials for high temperature applications: A review,” *IEEE Transactions on Components Packaging and Manufacturing Technology*, Vol. 1, No. 4, pp. 457-478, 2011.

[21] T. Richter, “Als Werkzeug voll etabliert—Laser in der Druckvorstufe,” *Laser Technik Journal*, Vol. 8, No. 4, pp. 19-21, 2011.

[22] CeramTec Product Data Sheet, “CeramCool® The Ceramic Heat-Sink for Efficient Thermal Management,” May 2009.

[23] GWI Product Data Sheet, “Eigenschaften von Monokristall-Saphir.”

[24] Indium Corporation Product Data Sheet, “Eutectic Gold/Tin Solder.”

[25] E. Beckert, T. Oppert, G. Azdasht, E. Zakel, T. Burkhardt, M. Hornaff, A. Kamm, I. Scheidig, R. Eberhardt, A. Tünnermann, and F. Buchmann, “Solder jetting—A versatile packaging and assembly technology for hybrid photonics and optoelectronical systems,” Proceedings of the IMAPS 42nd International Symposium on Microelectronics, p. 406, 2009.

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