

Advanced SiP Packaging Technologies of IPD for Mobile Applications

Meenakshi Prashant,^{1,*} Seung Wook Yoon,¹ GeunSik Kim,² Kai Liu,² and Flynn Carson³

Abstract—Integrated passive device (IPD) technology was originally developed as a way to replace bulky discrete passive components, but it is now gaining popularity in ESD/EMI protection applications, as well as in RF, high-brightness LED silicon submounts, and digital and mixed-signal devices. IPD is a device realized by resistors, inductors, capacitors, filters, and so on, for electrical functions such as matching and transforming, among others. Passive devices essentially optimize overall device performance. The key benefits offered by IPDs, as compared with LTCC and laminate-embedded passive devices, are primarily a smaller form factor and higher performance. IPDs are finding applications wherever it is desirable to reduce space on the application board or to reduce cost at the system level.

Keywords—Packaging, SiP, mobile, inductors, embedded, interposer

INTRODUCTION

New applications for many electronic products are driving the trend for innovating advanced packaging solutions with small form factor using reliable interconnection technologies at low cost. In particular, wireless communication's demand for high integration of RF devices is a challenge for the development of integrated package solutions. RF integrated circuits have emerged as candidates to satisfy the strong demands and to work with silicon technologies in the rapidly growing markets for wireless communication products.

In many RF applications like GSM/DCS, CDMA cellular phones, WLAN, and WiMAX systems, primarily the RF power amplifier and front-end modules make up for the critical parts of the radio systems. In these modules, the passive networks are predominantly used in system circuits where 60-70% of the footprint area is consumed by discrete passives [1] (Fig. 1). These applications typically use ceramic technology because of its good electrical and thermal characteristics. However, integrated passive devices (IPDs) based on the thin film deposition wafer processes at the silicon wafer level offer more advantages for a simplified and compact passive module with excellent parameter control to form large value resistors, high Q inductors, and capacitors. They also provide higher performance than the standard devices. These IPDs can be integrated

with other functionalities, enabling complete module solutions and offering overall better system performance.

Currently, the IPD market is also being driven by RF applications such as WLAN, GPS, GSM, WiMAX, and WiBro. In particular, there is high demand for mobile applications and products in the emerging RF CMOS market that require low cost, smaller size, and high performance.

In order to get the right products having reduced size, lower cost, and good performance, packaging design and technology should be considered in device integration and implemented together in IPD designs. In addition, a comprehensive understanding of electrical design, packaging, and mechanical properties in component and system level design is important.

In this paper, we discuss some IPDs integration schemes such as system in package (SiP), chip scale module package (CSMP), embedded wafer level ball grid array (eWLB), and IPD as a through silicon via (TSV) interposer, that enable device miniaturization and provide better performance.

INTEGRATED PASSIVE DEVICE TECHNOLOGY DESCRIPTION

IPD technology is based on thin film processes on a silicon substrate on which the metal layers and dielectric layers are grown to form thin film passive structures. As shown in Fig. 2, MCAP, M1, and M2 are the metal layers, and silicon nitride, polyimide-1, and polyimide-2 are the dielectric layers. The MCAP and M1 metal layers with silicon nitride as the dielectric are used to form MIM (metal-insulator-metal) capacitors with 1 μm and 2 μm metal thickness, respectively. A thick Cu metal layer of 8 μm is implemented as the M2 metal layer, forming an inductor. A TaSi layer is used to obtain sheet resistance of a resistor. IPD can be either wire bondable or a flip-chip type that enables further integration with other functionalities into module [1].

IPD INTEGRATED SOLUTIONS

A. SiP Packaging Solution with IPD

SiP integrates different dies on one package substrate. It also allows the system to be partitioned into separate RF/analog/digital blocks. Thermal issues are also easy to mitigate. However, this requires advanced design and packaging capabilities. For example, digital blocks can be implemented in advanced CMOS and high performance analog blocks in RF CMOS or SiGe or BiCMOS. Analog integration provides better performance and lower power dissipation, and can also enable

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¹STATS ChipPAC Ltd., Singapore 768442

²STATS ChipPAC Inc., Tempe, Arizona 85284 USA

³STATS ChipPAC Inc., Fremont, California 94538 USA

*Corresponding author; email: Meenakshi.PADMANATHAN@Statschipac.com

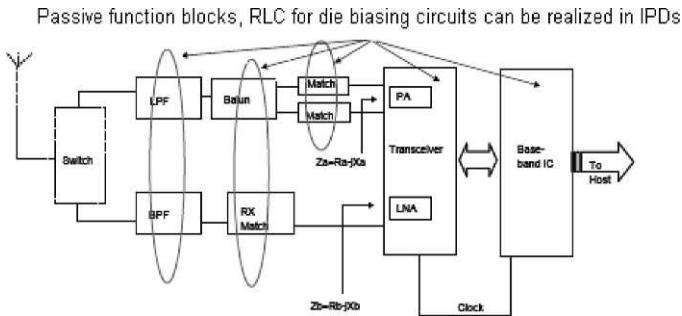


Fig. 1. Wireless system block diagram.

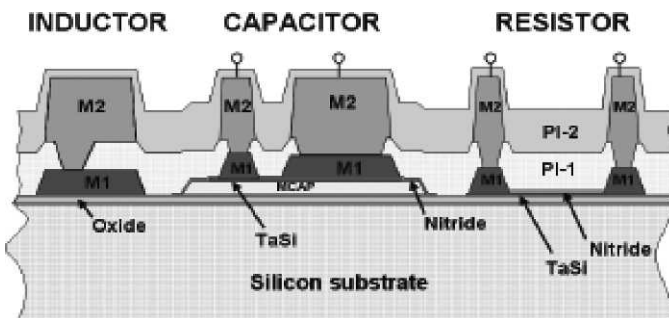


Fig. 2. Schematics of thin film integrated passive device structure.

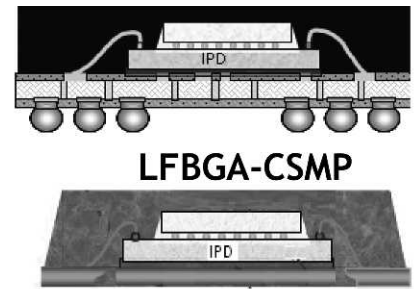
passives integration on a chip in the form of IPDs. SiP technology helps to integrate these and enables faster time to market with shorter cycle time in design and manufacture. Fig. 3 shows some examples of the SiP solutions with IPD.

CSMP is an advanced SiP solution that features a modular architecture that integrates mixed IC technologies and a wide variety of passive devices (IPDs), such as resistors, capacitors, inductors, filters, baluns and interconnects directly onto a silicon substrate. The result is a high performance system level solution that provides a significant reduction in package size, number of interconnections, and system board space requirements, and can be used for many applications.

Fig. 3 shows CSMP integration with different interconnection schemes such as wire bonding or flip chip with organic or leaded packaging format. IPD in the WLCSMP is used as an interposer module that integrates flip chip devices such as an RF transceivers, baseband chips, memory modules, and some discrete components as shown in Fig. 4. In LFBGA-CSMP and QFPp CSMP, IPD is wire-bonded to the laminate substrate/lead frame and a flip chip die is mounted on it. In another example, a flip chip IPD consisting of baluns is integrated in a fcVFBGA-SD2 + 1 package that includes an RF transceiver die wire-bonded to a two layer laminate substrate. In these cases, IPDs enable increasingly complicated microelectronics systems with the integration of diverse electronic functions such as RF transceivers, power amplifiers, power management units, and digital processors.

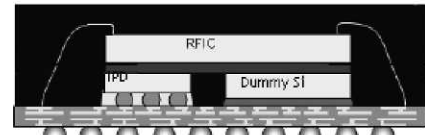
B. IPD, High Q Inductor Solution with eWLB Technology

RF applications implement functional blocks such as the low noise amplifier (LNA), transceiver, power amplifier



LFBGA-CSMP

QLPp-CSMP



fcVFBGA-SD2+1 CSMP

Fig. 3. Examples of various SiP solution with IPD.

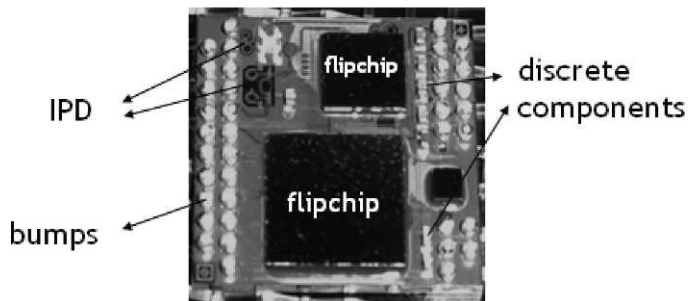
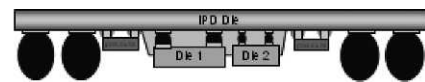


Fig. 4. WLCSMP (wafer level chip scale module packaging).

(PA), baluns, filters, and so on, in which the inductors play a key role in the performance of the circuits. The quality factor of an inductor is the figure of merit for inductor performance. Even though PAs made from GaAs are widely used due to their good electrical and thermal properties, their costs still needed to be reduced. CMOS based technology is used in order to substantially reduce the costs of RF modules. In an RF circuit, for example, a power amplifier has an impedance matching circuit consisting of capacitors and inductors that consume a significant portion of the die size that can potentially be replaced by an IPD. Although CMOS technology also has the drawback of degraded inductor Q due to silicon substrate losses, there are other solutions developed to form inductors for RF integrated circuits with improved performance.

The typical approach is to make inductors from laminate substrates [2, 3]. Alternatively, inductors made from a wafer level package RDL approach have been introduced and successfully used for RF modules/SiP in PA matching and

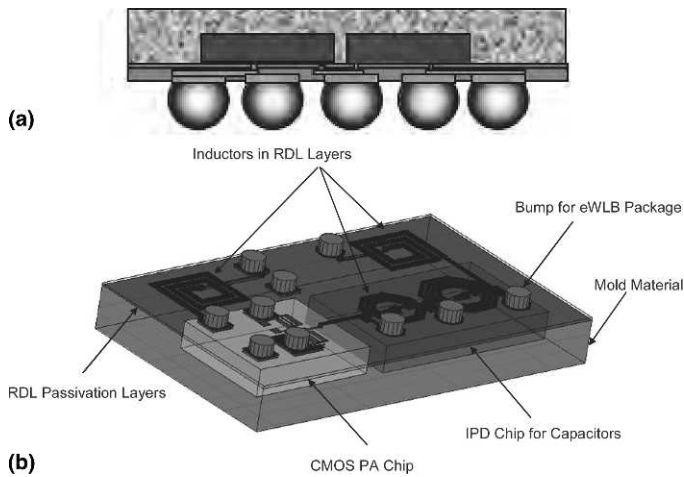


Fig. 5. (a) Schematics of multichip eWLB and (b) illustration of a CMOS PA die and silicon IPD die embedded in mold substrate (eWLB).

coupling circuits. In this process, the inductors are not in the area directly above an active IC, but above the mold compound material of the eWLB through RDL layers. These mold materials mainly serve two purposes. Primarily, they are package substrates, providing mechanical strength for their respective packages. Secondly, they have low loss tangent, which is essentially a good property for making RF components, such as inductors. Since the inductors are not on top of active ICs, their interference with active ICs is minimized and the signal integrity of ICs can be maintained [4].

Fig. 5 illustrates an eWLB package that includes an RF CMOS PA chip, an IPD chip, and RDL inductors above the IPD chip (but not made from the IPD process) [4]. The IPD die mainly serves as an impedance matching network for the PA. In an eWLB package, the connection from the RDL inductors to the RF chip is made through vias connecting the RDL layer and the top metal layer in the RF chip. The connection between the RDL and the IPD chip is made through vias connecting the RDL layer and the top thick metal layer in the IPD. There are three different substrates: CMOS substrate, IPD substrate, and mold compound substrate, as shown in Fig. 5, and the passivation layers are made through the wafer fabrication process.

Fig. 6 shows the measured response of a 1.4 nH inductor made from the wafer-level package process. The measurement was conducted through the G-S-G pads implemented with the inductor. The plotted response includes the contribution from the G-S-G probing pads (not de-embedded).

Fig. 7 depicts Q performance comparison of a 3.6 nH inductor made from different processes/options. As shown, if an inductor is made directly above an active IC through this process, its Q peak is around 26. However, if it is made in an eWLB mold area, its peak Q can be 35. Even compared with the same inductor made from a standard IPD process [4], the Q value from the inductor made in the mold material is still the best.

The high-Q inductors made in the mold material as eWLB packaging are therefore good candidates for RF passive functional blocks. In addition, the plating Cu RDL process on a molded substrate may make it unnecessary to use specially-

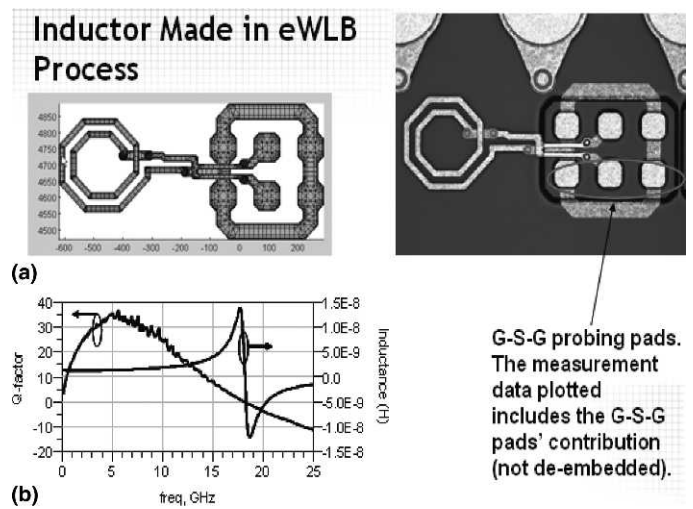


Fig. 6. (a) Inductor layout with G-S-G pads for characterization. (b) Electrical response of a 1.4 nH inductor made from wafer-level package process.

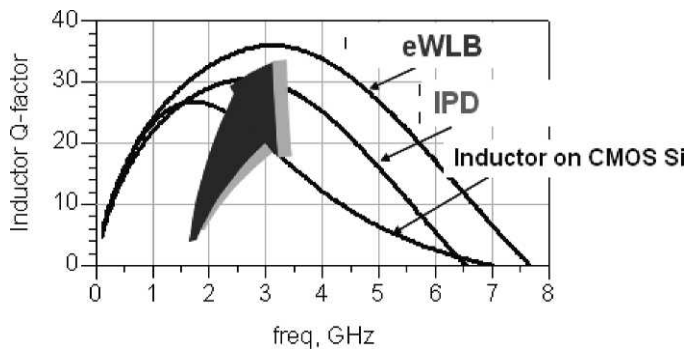


Fig. 7. Q-factor comparison of inductors made from different options/processes.

treated IPD substrates for low cost. If capacitors are needed in the circuits, we may still use an IPD chip to build them, but the IPD substrate can be a regular p-type substrates too for low cost.

Thus, RF CMOS technology has a bright potential for PAs to be made in CMOS instead of GaAs for further cost reductions. Apart from the new technology, the key requirement is to overcome the high RF loss from the CMOS Si substrates, so it is preferable to keep passives in PAs such as inductors for circuit matching away from the CMOS chips. In contrast to traditional GaAs PA processes, CMOS processes do not have back side metallization. For an RF power amplifier, the key aspect is the heat dissipation that can affect the performance, for which a bumped PA instead of a wire bondable PA die is preferred, thus providing shorter interconnection to its periphery. In addition, this is required for electrical performance in terms of degeneration inductance or ground inductance [4].

C. Embedded Substrate Packaging with IPD

Drivers for 3D packaging solutions are manifold and each requirement calls for different answers and technologies. Mainly miniaturization, but also density, performance,

simplification of design and assembly, flexibility, functionality, and finally, cost and time to market have been found as the core drivers for going 3D. Even beyond die and package stacking and folded packages, embedding dies is a key technology for heterogeneous system integration [5].

There are two main approaches for embedded die technologies: wafer level integration, in which chips are embedded into polymer encapsulants and 3D vertical integration, in which dies are embedded in substrate. For wafer level integration, a lot of activities are running worldwide and one good example is an eWLB package. Another concept for high 3D integration of active components is chip in substrate (CiS), or embedded die substrate (EDS) technology. It is based on embedding of device (die or IPD or discrete components) into built-up layers of printed circuit boards (PCBs). The dies are bonded onto a core substrate using an adhesive; a resin coated copper (RCC) layer with thin Cu is used for the subsequent lamination. Interconnects are established by laser drilled microvias followed by a PCB-compatible Cu plating [6]. The combination of both concepts (embedding into polymer by molding and redistribution by PCB technologies) has the potential for highly integrated and low cost packages [7].

The EDS package technology is an extension of the standard multilayer organic flip-chip-ball-grid-array (fcBGA) substrate used for microprocessor packaging. The schematic of the fcBGA package is illustrated in Fig. 8, wherein IPDs are embedded in the organic substrate. The package stack-up consists of the core and multiple metal layers, and microvias are used to provide electrical connectivity between the embedded component and the rest of the package, just as in the case for the conventional organic substrate.

As shown in Fig. 9, as a performance baseline, an embedded 2.4 GHz bandpass filter (BPF) is compared against the flip-chip version of the same component. Both embedded and flip-chip IPDs exhibit the same electrical performance up to 5 GHz. As a result of the package parasitic inductance, both flip-chip and embedded die filters exhibit a transmission zero at high frequencies. The difference in the location is due to the package vias used to connect the embedded IPD to the surface of the package. In comparison, the flip-chip device has only small solder bumps, which reduces the inductance and moves the resonance slightly. With being said above, Silicon-based radio frequency integrated passive devices (IPDs) have been successfully embedded in the core of a multilayer organic package substrate. The combination of the silicon-based precision technology for the RF passives and the multilayer organic package substrate provides a good alternative to traditional substrate-embedded RF passives, where at least one low-loss thin film is directly embedded in the package substrate stack-up.

D. IPD as TSV Interposer

IPD serves analog filtering, power conversion, and digital applications where a high density capacitor is the main component. The use of a digital interposer requires a combination of isolated metal-filled through silicon vias with high density capacitors. The drive to explore digital interposers comes from the need to reduce technology geometries, improve power dissipation, and increase yield. Digital interposers reduce parasitic inductance loop from the circuit power pins and the

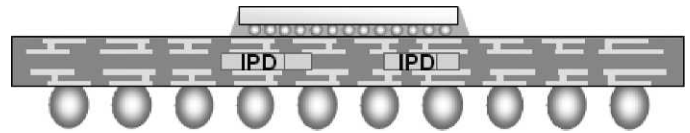


Fig. 8. Schematics IPD embedded substrate for fcBGA packaging.

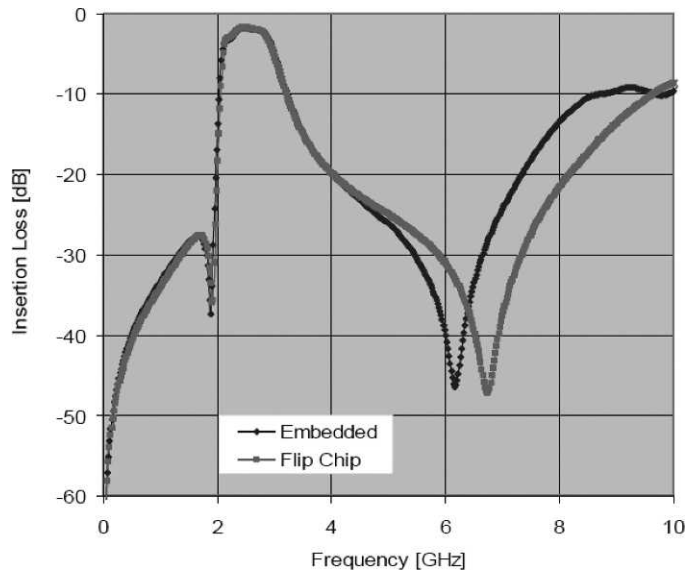


Fig. 9. Comparison between embedded and flip-chipped 2.4 GHz bandpass filter [5].

nearest decoupling capacitors that can be integrated in the IPD interposer [8].

IPD TSV offers alternative packaging solutions rather than limiting to passive replacement alone. TSVs provide support for the integration of passive elements directly onto the silicon substrate for much higher densities like embedded decoupling capacitors which are mainly used in a wide range of digital applications. The advantage of IPD over non-IPD technologies is further vertical interconnection, thus enabling high density capacitor embedding. As TSV interposers provide the shortest electrical path between devices and power supply decoupling capacitors, TSVs with their very low inductance interconnects will thus enable very high electrical performance when integrated with embedded capacitors.

Fig. 10 shows an IPD interposer. In this approach, first the passives are formed on a silicon wafer as an IPD. Secondly, the deep vias are etched and filled with metal, followed by a thin film process of dielectric deposition and metal layer RDL patterning on the front side of the wafer first and then the back side of the wafer. Finally, bump interconnections are made. Adding TSV to the IPD process does add to the process complexity and cost, but in the end, it results in footprint reduction to offset the higher cost. IPDs can be extended to the digital market as well due to their capability to integrate different passive functions as like filters, with TSV technology implementation for smaller form-factor, higher electrical performance as well as 3D stacking/integration. TSV interposers become increasingly significant to 2.5D or 3D SiP solution for highly integration purpose as shown in Fig. 11.

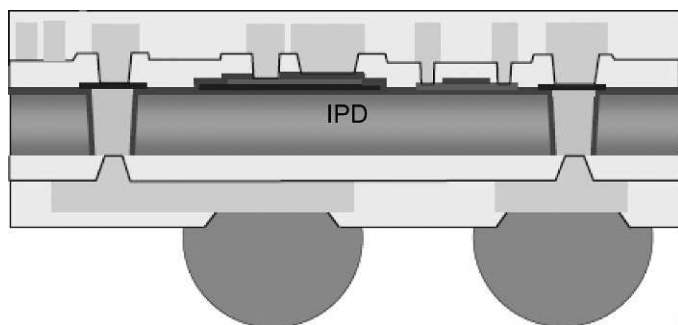


Fig. 10. TSV integration in IPD interposer.

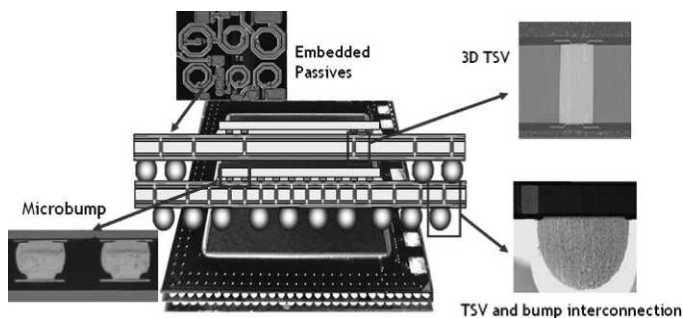


Fig. 11. 3D SiP module concept integrating TSV in IPD interposer.

Moving forward, the application areas for IPD will continue to evolve, especially as new packaging technology, such as 3D stacking, wafer level packaging, TSV become available to provide vertical interconnections within the IPD.

SUMMARY AND CONCLUSIONS

The wireless communication sector is driving radical changes in the electronics industry, stimulating a number of new packaging solutions. Size, performance, reliability, and cost are the major drivers to function-oriented packaging. In the quest for achieving smaller form factors, system in package

(SiP) has gained particular attention as the approach can deliver the desired form factor with good performance, reasonable cost, and fast time to market.

Direct die-on-die stacking, embedded die in wafer level package, and vertical integration of IPD in SiP have been widely promoted as the means to reduce the footprint while enabling 3D integration in SiP. eWLB and 3D TSV integration enable solutions expanding into various application ranges for a true 3D SiP system. These new packaging platforms with IPD may provide more value-added performance in a mobile/portable microelectronics system with reduced cost.

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