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Overview of Fatigue Failure of Pb-Free Solder Joints in CSP/BGA/Flip-Chip Applications

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Abstract—**The purpose of this paper is to provide an overview of SnAgCu solder joint fatigue in BGA/CSP/flip-chip applications and the concern of long-term reliability. The most common mode of failure is ductile fracture due to creep strain. Several methods of predicting the overall life of the solder joint are the Coffin-Manson approach, a constitutive fatigue law, and a damage based model using FEM (finite element methods). The effects of underfill and its processes as well as design considerations that will increase reliability will also be discussed.**

Keywords—**BGA, CSP, Coffin-Manson, Damage, Fatigue, flip-chip, Pb-free, Solder, Underfill, SnAgCu**

Introduction

Many electronic packages today use BGA (ball grid array), CSP (chip scale packaging), and flip-chips. These packages offer many advantages including increased I/O count and functionality in a reduced size; an increase in thermal efficiency which results in improved heat dissipation, robustness in the manufacturing process (chip attach); and the design further allows for self centering if misaligned during the solder reflow process. The concern, however, is solder joint fatigue and the overall solder reliability. This is due to the CTE (coefficient of thermal expansion) mismatch between the BGA/CSP/flip chip, the solder joint (primarily SnPb and SnAgCu), and the PWB (printed wiring board), resulting in increased thermal stresses, ultimately resulting in low cycle fatigue failure. See Fig. 1 for an example of a solder joint fracture [11].

Due to the recent environmental and legislative concerns of the use of Pb (lead), there is a sense of urgency for replacing SnPb eutectic solder with a Pb-free variant, such as SnAgCu, within the electronics industry. Many studies have been done on the reliability of SnPb solder joints in CSP/BGA/flip chip packages [1]. SnAgCu solder has been endorsed by the National Electric Manufacturing Initiative (NEMI) due to its similarity in both cost and performance to SnPb solder. However, limited characterization has been done to date on long term reliability.

To evaluate thermal fatigue in solder joints in CSP/BGA/flip chip packages, many experiments have been done using FR4 (substrate material) as it is one of the most commonly used materials, mainly for its performance, ease of manufacturing, and low cost. To accelerate failure, the most common test is thermal cycling, usually over a temperature range of –55 °C to +125 °C. Data-logging, measuring the thru-resistance of the chip, is monitored throughout the test to measure continuity. If the resistance is too high, then the solder joint of the test sample has a formation of a crack or a complete fracture which will lead to failure.

To evaluate the creep strain of the solder joint, several different types of methodologies will be discussed. They are the modified Coffin-Manson approach, the finite element method (FEM), the constitutive fatigue model, and the damage model. Also discussed are the potential design improvements to improve the overall fatigue life of the solder joint, such as the use of underfill and geometry design considerations.

Failure Modes

The primary mode of failure is creep-induced ductile fatigue fracture, which occurs at the interface of the solder joint and the chip package. The outermost solder joint within the package experiences the most thermal stress due to the CTE mismatch. The chip package (e.g., silicon) and substrate (e.g., FR4) are assumed to be elastic, while the SnAgCu solder joint exhibits inelastic properties. Because of temperature cycling, the thermal stress induced initiates the creep in the solder joint which ultimately leads to crack propagation and then failure. See Fig. 1 for SEM (scanning electron microscopy) of a typical fractured solder joint [11].

Vandevelde et al. [14] indicated that Pb-free solder (i.e., SnAgCu) is more creep resistant (i.e., lower creep strain rate) than conventional eutectic SnPb solder at higher temperatures, which results in a longer fatigue life, assuming equal stress states. In comparing the elastic modulus of SnAgCu solder to that of SnPb solder, it was found that the inelastic strains were better than the SnPb. However, when comparing the inelastic strain energy density, the SnPb performed better [14]. They concluded that the slower creep strain rate coupled with the higher stress states of the SnAgCu resulted in higher hysteresis loops with more energy dissipated per cycle [14].

Drop impact and vibration effects also have an impact on solder fatigue reliability [14]. The failure is brittle fracture at the solder joint to substrate interface. These modes of failure will not be discussed in the survey.

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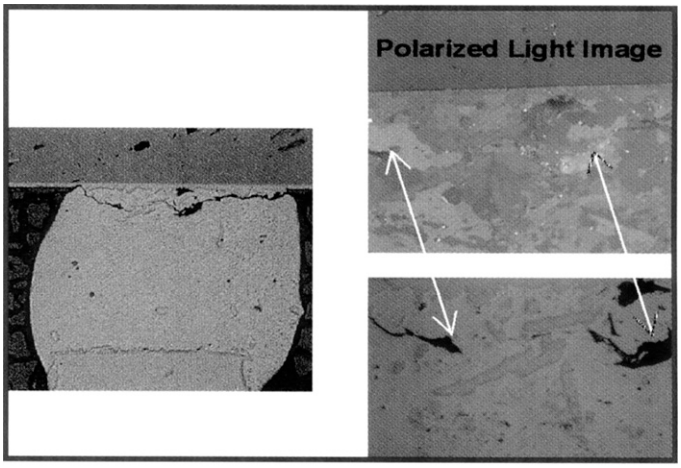

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Fig. 1. Example a partially failed SnAgCu solder joint [11].

Modeling

A. Modified Coffin Manson Approach

The modified Coffin-Manson approach developed by Engelmaier [16] is often used to predict the fatigue life of the solder joint bump early in the design process [1]. The predicted model for cycles to failure, N_f, however, is often conservative. The relationship can be given by the following equations for SnAgCu [1]:

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f}\right)^{1/c} \quad (1)$$

$$c = -0.347 - 1.74\times10^{-3}T_{sj} + 7.83\times10^{-3}\ln\left(1+\frac{360}{t_{dwell}}\right) \quad (2)$$

$$\Delta\gamma = F\left[\frac{L_d(\alpha_c - \alpha_s)\Delta T}{h}\right] \quad (3)$$

where N_f is the number of cycles to 50% failure; $\Delta\gamma$ is the shear strain range; ε_f is the fatigue ductility coefficient for the material; and c is the fatigue ductility exponent which is dependent on the solder material. T_{sj} is the average cyclic joint temperature; and T_{dwell} is the dwell time at the maximum temperature (during thermal cycling). F is a model calibration coefficient; L_d is the distance to the neutral point from which the thermal expansion occurs; α_c and α_s are the CTE (coefficient of thermal expansion) of the component and the substrate, respectively; ΔT is the maximum temperature range, and h is the effective height of the solder joint. See Fig. 2 for an example of a plastic strain range versus fatigue life curve.

The use of Engelmaier's modified Coffin-Manson approach is limited and must meet the prerequisites per IPC-D-279 [2]. These are: (1) the solder joint quality, (2) large temperature excursions, (3) high frequency/low temperature, (4) local expansion mismatch, and (5) very stiff leads/very large expansion mismatches. Ridout et al. [2] provides further explanation.

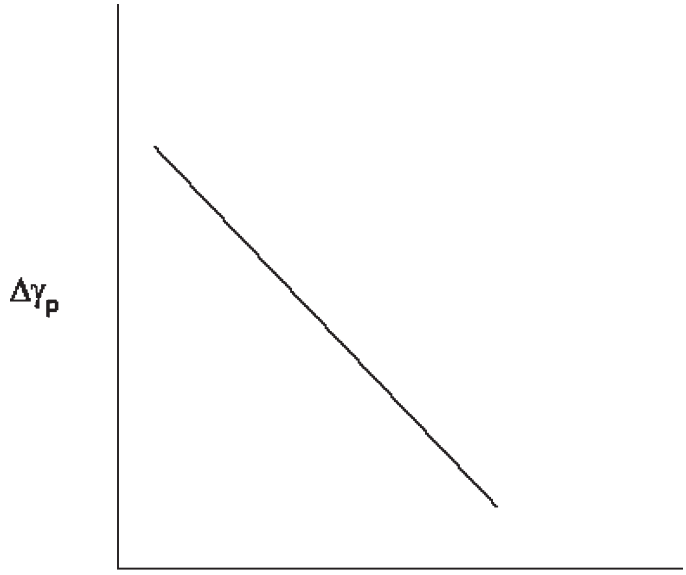

Fig. 2. Example of a Coffin-Manson's plot relating the fatigue life with the plastic strain range.

Finite Element Method

FEA (finite element analysis) is used to analyze the inelastic strain range and strain energy density of the solder joint due to thermal cycling. This is later used to predict the fatigue life cycles to failure for the solder joint. Both 2D and 3D FEAs are used, the latter requiring more computational time due to the increased mesh size. Examples of a 3D FEA are shown in Figs. 3 and 4 [10].

Ridout et al. [2] summarized the required steps which are: (1) Geometry creation—typically from 3D CAD software. Because of the symmetry involved in the chip package, a typical analysis usually requires one-eighth the size. (2) Mesh size—Depending on the accuracy required, the mesh may need to undergo an iterative process to converge on a result that has little variation. (3) Material properties. (4) Boundary conditions (i.e., constraints). (5) Application of the fatigue law—As previously discussed, the inelastic strain range and strain energy density need to be extracted as well as the plastic and creep strain. Pang et al. [3] indicated that the inelastic strain range directly relates the normal and shear strain components induced in one thermal cycle to the fatigue life of the solder joint. The deformation due to the thermal cycling alters the displacements in both the in-plane as well as the out-of-plane from the center of the chip package. This then introduces the normal and shear strains in the solder joints. Pang et al. [3] noted that the accumulated strain ranges per cycle weakens the solder joints, which leads to failure.

Constitutive Fatigue Model

This method employs the use of the initial results obtained from FEA to determine the constitutive response of creep in SnAgCu solder. Numerous studies have accepted both the

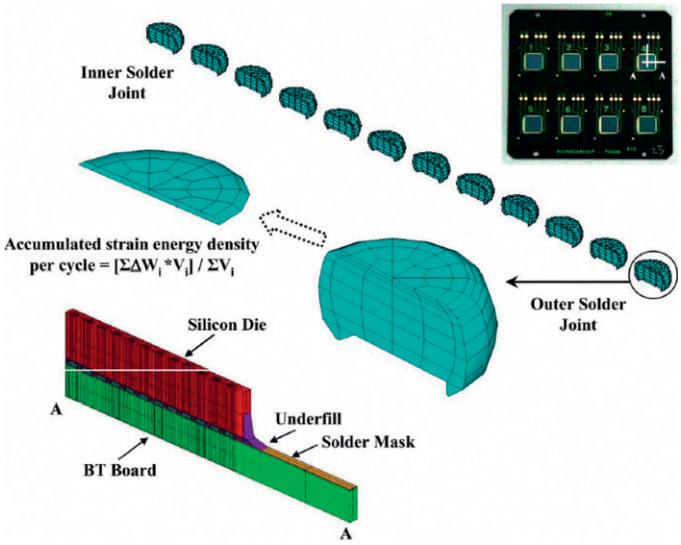

Fig. 3. Example of a fatigue failure parameter extraction by elemental volume averaging method [10].

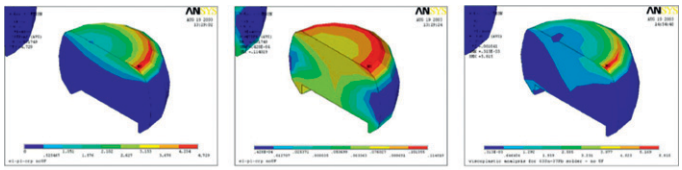

Fig. 4. Example of a non-underfill flip chip on board (FCOB) solder joint. (a) Plastic strain energy density from elastic-plastic-creep analysis. (b) Creep strain energy density from elastic-plastic-creep analysis. (c) Viscoplastic strain energy density from viscoplastic analysis [10].

double power law formulated by Wiese et al. [17] and the hyperbolic sine law by Schubert et al. [18] to approximate steady state creep [4]. Of note, both of the constitutive fatigue laws are based on empirical data for that particular experiment. Caution must be exercised since the amount of experimental data with regard to SnAgCu solder is limited and further investigation is required.

The double power law is used to describe the state behavior (or the secondary creep) of the solder, first at a low stress state (climb controlled creep) and at a high stress state (glide/climb controlled creep). For SnAgCu solder, the relation is given by [4]:

$$\dot{\varepsilon}_{cr} = A_1 \exp\left(\frac{-Q_1}{RT}\right)\left(\frac{\sigma}{\sigma_n}\right)^{n_1} + A_2 \exp\left(\frac{-Q_2}{RT}\right)\left(\frac{\sigma}{\sigma_n}\right)^{n_2} \quad (4)$$

where $\dot{\varepsilon}_{cr}$is the steady state creep rate; according to Wiese et al. [17] $A_1 = 4 \times 10^{-7}$ s^{-1}; $Q_1/R = 3223$; $n_1 = 3.0$; $A_2 = 1 \times 10^{-12}$ s^{-1}; $Q_2/R = 7348$; $n_2 = 12$ when $\sigma_n = 1$ MPa [4].

The hyperbolic sine law of Schubert et al. [18] is also used to approximate steady state creep at intermediate and high stresses [4]. Of note, the creep data varies based on the test sample geometry size and the methodology in which the sample was taken [2]. The relation is given by the following equation:

$$\dot{\varepsilon}_{cr} = A_1[\sinh(\alpha\sigma)]^n \exp\left(\frac{-Q_a}{RT}\right) \quad (5)$$

where according to Schubert et al. [18], $\dot{\varepsilon}_{cr}$ is the steady state creep rate; $A_1 = 277984$ s^{-1}; $\alpha = 0.02447$ MPa; $N = 6.41$; $Q_a/R = 6500$; and the Poisson's ratio = 0.36 [4].

Eqs. (4) and (5) are used to create a hysteresis curve. Primary creep can also be used to provide better predictions in SnAgCu solder joints. Utilizing kinematic hardening, isotropic hardening (Anand model), as well as the use of a time variable, the work by Darveaux et al. [15] can be used for predicting primary creep. Ridout et al. [2] provides equations for the aforementioned methods. At this time, there is limited information on the hysteresis curve for SnAgCu solder. Also, limited studies have been performed with regard to kinematic hardening, isotropic hardening, and a time- use variable; further investigations are needed.

For all of the methods described above, it is important to note that the studies were performed using specific chip, chip technology, and solder bump geometries, as well as specific temperature profiles. Deviations will often result in inaccurate fatigue life.

Damage Model

The main advantage of the damage mechanics method is that unlike the previous prediction methods, there is no reliance on chip geometry. It mainly focuses on crack propagation of the solder joint.

Tang and Basaran [5] used this technique on the eutectic SnPb solder with promising results. Instead of using the accumulated shear strain per cycle which is typically used in damage mechanics, they based their technique on the second law of thermodynamics and used entropy as a damage metric. Basaran and Yan [19] have shown that entropy (the amount of disorder in the system) can be used as a damage metric in solid mechanics [5]. Extensive modeling has been done by Tang and Basaran [5] using the ABACUS FEA software package to characterize the unified viscoplastic model for cyclic fatigue behavior under thermal cycling. This simulation was then compared to laboratory work performed by Adams [20], Skipor et al. [21], McDowell et al. [22] and the FEAs show very close correlation to each other [5].

A recent study was performed by Wei et al. [6] with regard to the use of damage mechanics for SnAgCu solder. Using the shear strain per cycle, they formulated several damage-based and constitutive equations for evaluation and compared that to experimental data [6]. Validation tests were done at room temperature to determine the effect of the strain rate with respect to the hysteresis loop and show close correlation to each other. Wei et al. [6] indicated that although the study shows significant promise in damage based mechanics, further evaluation is needed.

Design Improvements

A. Effects of Underfill

Concerns within the microelectronics industry about thermal fatigue damage have led to the implementation of underfill, which minimizes the effects of the CTE mismatch of the solder joint and the chip. One of the main features is that it alters the stress-strain relationship of the package as well as providing stress relief to the solder joint [7]. It also provides

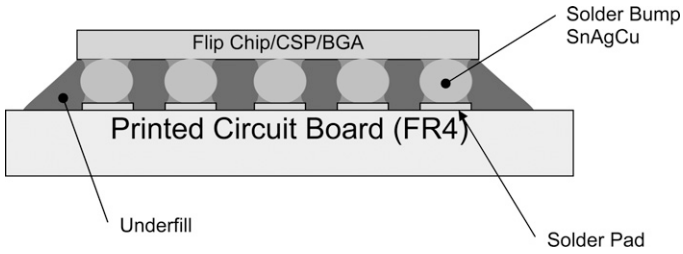

Fig. 5. Example of flip chip/CSP/BGA.

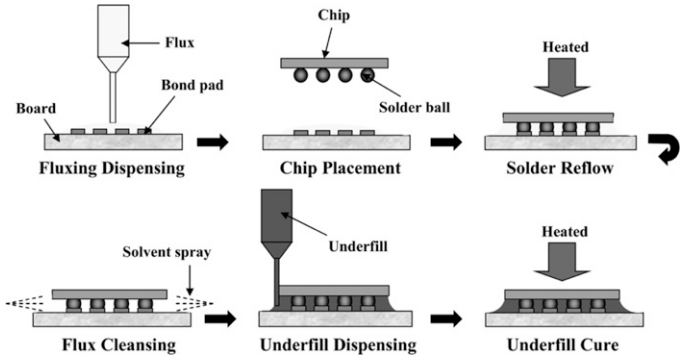

Fig. 6. Conventional underfill process for flip chip [9].

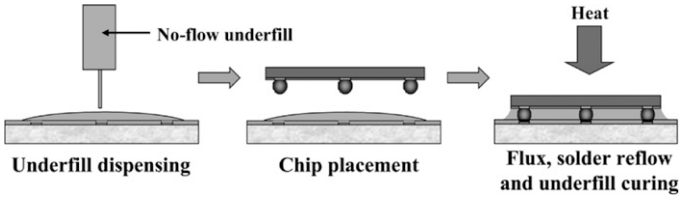

Fig. 7. No-flow underfill process for flip chip [9].

environmental protection and minimizes the possibility of corrosion or electromigration [8].

Underfill material contains approximately 60% epoxy/40% silica (but can change depending on the application). As shown in Fig. 5, the underfill fills the gaps between the underside of the chip and the substrate after assembly. Once cured, the underfill provides a high elastic modulus and a low CTE to closely match that of the solder joint. The stresses from CTE mismatches are then evenly distributed throughout the entire chip assembly. Studies have shown that the fatigue lifetime of the solder joint increases by approximately 10–100× [9]. The equivalent total strain is reduced through the use of underfill [13].

The addition of the underfill has also caused the industry to determine the most cost-effective way to integrate this added process. There are several methods of installing underfill. They are: (1) The conventional method—a post chip assembly process, by which, through capillary action, the underfill is dispensed. (2) No-flow underfill—a prechip assembly process which eliminates the flux cleaning steps, avoids the capillary flow of underfill, and combines the reflow and curing (of the underfill) in one step [9]. (3) Molded underfill—applied using a transfer molding process, by which the underfill encapsulates the entire chip package [9]. (4) Wafer level underfill—installed at the chip level, where the underfill is B-staged

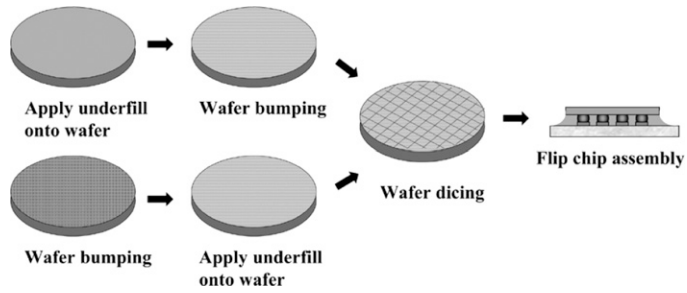

Fig. 8. Wafer-level underfill process for flip chip [9].

and applied either on the bumped wafer or a wafer without solder bumps [9]. See Figs. 6, 7, and 8 for the process steps of the conventional, no-flow, and wafer level underfill, respectively [9]. Out of the four processes, the no-flow and conventional underfill are the most common. The wafer level underfill is promising as it could reduce operational cost and improve manufacturing robustness.

B. Chip Geometry/Design

Darveaux et al. [15] indicated that die size, solder ball count, mold compound filler content (package), test board thickness, test board pad design, temperature cycle, and other conditions affects solder joint reliability. Although the evaluations were based on BGA packages, the results could also apply to flip-chip and CSP packages.

In the Darveaux et al. study, they indicated that the fatigue life can increase up to 6× if the die size is reduced. This was due in large part to the CTE of silicon being low, but having a high elastic modulus. This resulted in higher stresses and strains as the chip size increased. For solder ball count, there was about a 1.8× increase in fatigue life when a large package contained more solder balls, because as more balls were added, the overall stiffness of the matrix increased relative to the assembly, or else the solder balls reinforced each other [15]. For mold compound filler content, the fatigue life is reduced by half as the filler content increases [15]. Darveaux et al. [15] noted that a reduction in test board thickness may increase fatigue life. A reduction in pad size on the substrate increases the fatigue life. This is because the increase in joint height uniformly distributes the stress at the solder joint/pad interface [15]. Conditions such as routing density, manufacturing yields, and performance under bending load need to be taken into account [15]. Quicker ramp rates often result in higher stresses and more matrix creep in the solder joint [15].

CONCLUSIONS

Concern about solder joint fatigue in BGA/CSP/flip-chip packages has led to extensive stress analysis to predict the overall life of the SnAgCu solder joint as a replacement of the conventional eutectic SnPb solder due to political and environmental concerns. The primary failure mode is ductile fatigue fracture at the chip/solder joint interface due to creep strain. Due to the CTE mismatch between the solder joint chip package and substrate, the highest amount of thermal stress occurs at the outermost solder joint. SnAgCu solder was also found to be more creep resistant than SnPb solders, and its

overall performance varies at different temperatures/stresses. Other modes of failure include vibration effects as well as drop test effects, which cause brittle fracture at the solder joint/substrate interface. Various methods of analysis are used to predict the overall lifetime of the solder joint. These are: the use of a modified Coffin-Manson approach, implementation of FEA (finite element analysis), the constitutive fatigue law, and damage mechanics. The implementation of the underfill has a positive effect on increasing the fatigue life of the solder joint by as much as 10–100×. Various processes are used to apply the underfill; the most common within the industry is conventional underfill, which utilizes post processing, and no-flow underfill, which is a prechip assembly process. The use of molded underfill along with wafer level underfill has shown some promise as it may reduce operating costs and improve reliability. It was found that a reduction in chip size, an increase in solder ball count, a decrease in filler content of the chip package, a reduction in substrate thickness, smaller solder pads, and slower ramp rates help improve fatigue life.

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