A Systematic Approach to Thinning Silicon Wafers to the sub-40µm Thickness Range

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Abstract

The present trend in electronics packaging is the stacking of die at the wafer or chip level. However to ensure stacked chip packages maintain overall low height and weight package profile, silicon wafers have to undergo extensive wafer thinning processes. In this work, a systematic approach to thinning silicon wafers down to sub-40µm in thickness is presented. This paper will cover a detailed three stage wafer thinning method, which includes the mechanical back-lapping method for the bulk removal process and a combination of mechanical polishing and spin-spray wet chemical etch method for the fine removal wafer thinning process. The results will show that by just utilizing the mechanical back-lapping and mechanical polishing process the wafers can be easily thinned from 380µm to less than 50µm with ±2.5µm Total Thickness Variation (TTV). These back-lapped wafers are then further thinned by the spin-spray etching method to achieve final wafer thickness of less than 40µm. The paper will also show that by utilizing a modified carrier wafer, the handling of these sub-40µm ultra-thin wafers do not require custom made tools and can be easily integrated into existing wafer handling tools.

Key words

Wafer thinning, wafer back-lapping, mechanical polishing, spin-spray etching, wafer handling, stacked chipIntroduction

1. INTRODUCTION

The present call for increased device functionality and the shrinking of device geometry has clearly propelled the thinning of silicon wafers in the semiconductor industry. For example the Intel® Ultra Thin - Stacked Chip Scale Packages (SCSP) is a 5-stack wire-bonded package utilizing 75µm dies [1]. Prior to die stacking the wafer undergoes extensive thinning, typically from 380µm to sub-100µm. The wafer thinning process can be divided into two sub-processes, which are the bulk removal process and the fine removal process. The primary goal of the bulk removal process is to remove the majority of the wafer total thickness. The fine removal process serves several purposes, which are to remove damage caused by the bulk removal process, to relieve wafer stress, to planarize wafer and to reach the desired final thickness of the wafer.

There are several methods for silicon (Si) wafer thinning, namely mechanical backgrinding, chemical mechanical polishing (CMP), spin-spray wet chemical etching and plasma etching. Of the four wafer thinning methods, mechanical backgrinding is the most cost effective and common method for reducing Si wafer thickness by significant amounts while maintaining good total thickness variation (TTV).

The backgrinding process involves the use of a grinding wheel that rotates while in contact with the backside of the wafer. Most wafer backgrinding processes are conducted in several stages, beginning with coarse grinding and gradually finishing with fine grinding. Another variation on the backgrinding process is the back-lapping process. Pinel et al. [2] successfully used the lapping process to thin a 600µm Si substrate (10mm x 10mm) that was partially embedded in a carrier substrate to 10µm by using the method described.

Wafer thinning, by just utilizing mechanical backgrinding to attain wafer thickness of less than 50µm is not easily achievable. This is due to excessive stresses induced by the vigorous grinding process onto the wafer [3,4]. Alternative methods to thin wafers after backgrinding are by CMP, spin-spray wet chemical etching or dry etching. All three methods also have the capability to stress relief the Si wafer.

The CMP process involves polishing or thinning by affixing the Si wafer onto a carrier or backing wafer, which is then placed on a chuck (via vacuum). The chuck is then pressed faced-down on a polishing pad attached to a rotating plate. Typically a slurry containing silica particles with sizes between 10nm~200nm is dripped onto the rotating polishing pad. With the improvements in key monitoring techniques [5] and understanding the mechanical interaction between the wafer and the CMP system [6], the present day CMP results can give extremely good surface finishes with excellent TTV.

Wet chemical etching involves spraying an etching agent onto the surface of a rotating wafer periodically. Different chemical compositions of etching agents can give a wide variety of surface finishes [7], from a mirror-like surface finish to a very rough surface finish. The most common isotropic etching agent used for thinning Si wafers is a mixture of hydrofluoric acid (HF) and nitric acid (HNO_3).

Atmospheric downstream process (ADP) introduced by Tru-Si [14], is an all-dry etch process that removes material isotropically from the Si wafer surface [8]. The process uses a combination of argon (Ar) and carbon tetrafluoride (CF4) plasmas. The thinning mechanism occurs when radicals of the reactive gas, produced in the plasma, causes chemical reactions on the Si wafer surface. This process can selectively remove silicon from the wafer backside [9].

Table 1 shows a brief summary of the advantages and disadvantages of the various Si wafer thinning methods. It is clear from the discussion above that there are numerous ways to thin wafers. The choice of a specific thinning technique will depend on several key parameters, which are, the desired final thickness, TTV, and the surface finish of the wafer. In addition to this, cost, time to produce and handling of the thinned wafers will also play a key role for high volume production.

Table 1. The Advantages and Disadvantages of Various Wafer Thinning methods

Thinning Method	Type	Advantages	Disadvantages
Mechanical Backgrinding	Bulk	Cheap, fast process, good total thickness variation (TTV)	Prone to wafer cracking at thicknesses < 120µm, poor surface finish
Mechanical Polish	Fine	Cheap, fast process, good TTV, good surface finish	Prone to wafer edge cracking < 100µm
CMP	Fine	Excellent for wafer planarization, excellent surface finish	Expensive, slow process
Spin-Spray Chemical Etch	Bulk/Fine	Cheaper than plasma etching, fast process, good surface finish	Hazardous etchant, difficult to control the wafer TTV
Plasma Etching	Bulk/Fine	Fast process, can selectively etch Si without a mask	Very expensive process, dull surface finish

This paper will describe the thinning methodology employed to achieve sub-40µm ultra-thin Si wafers utilizing a modified carrier wafer. The thinning technique used in this study is the mechanical back-lapping method for the bulk removal process, mechanical polishing and spin-spray wet etching method for the fine removal process.

2. ANALYSIS

The wafers used for the thinning process in this study are 5" <100> phosphorous-doped 380µm thick prime silicon wafers. The silicon wafers had one polished side that was considered to be the front-side of the wafer. The front-side of the wafer is protected by an adhesive tape and attached to a handling wafer. The mechanical back-lapping method is considered for the bulk removal process instead of the conventional back-grinding process due to its capability of removing material with less subsurface damage (SSD). Close to 300µm of the wafer thickness will be removed by

this method. The wafer is then subjected to mechanical polishing to further reduce the thickness by 30µm. The polishing method has the capability to thin wafers with very little TTV and to remove partial SSD caused by the lapping process.

The subsurface damage (SSD) layers of mechanically thinned silicon wafers are divided into several layers as shown in Fig. 1. The first two layers, which are strongly damaged, are the polycrystalline and the mosaic layer. This is followed by the brittle crack layer which can extend as deep as 20µm into the wafers surface. The mechanically induced dislocations expand into the wafer until a third elastically strained layer is reached. Beyond this third layer the mono-crystalline silicon can be found [10-12].

The final spin-spray etch process utilized in this paper will have two vital roles in the wafer thinning process, the first to remove all SSD induced by the mechanical thinning, and the second to achieve the desired final thickness of the wafer. This final step also stress relieves the Si wafer from stresses induced by the mechanical thinning processes.

2.1 Wafer Front-Side Protection and Handling

The wafer front side is protected by thermal release adhesive tape manufactured by Nitto-Denko. This tape was

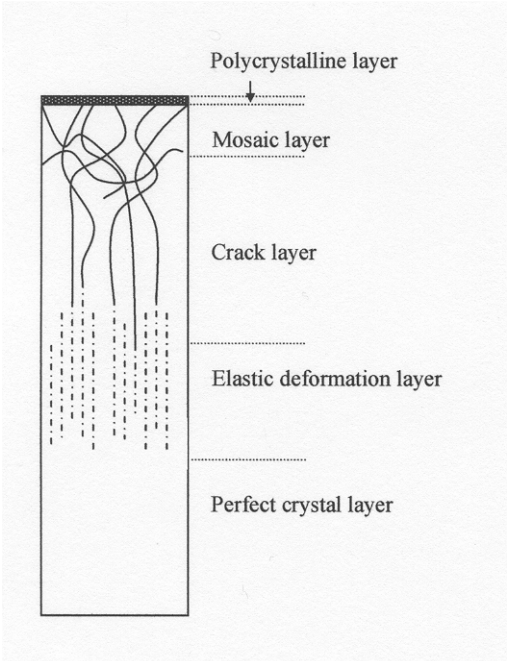

Fig. 1. SSD Layers of Mechanically Thinned Silicon

chosen because of its ease of use and uniform bonding layer thickness. The tape consists of three distinct layers, which are the thermal-release adhesive layer, the interface layer and the regular adhesive layer. Fig. 2 shows the complete assembly of the Si wafer, tape and carrier wafer prior to thinning. Only the thermal release adhesion layer is temperature dependant. The adhesion strength of this layer is completely lost when the thermal activation temperature is reached, while the other layer continues to retain its adhesion strength. This feature is extremely attractive as the wafer can be easily removed from the tape damage free at the end of the wafer back-lapping process. The tape also offers minimal out-gassing properties, making it very suitable for further wafer backside processing.

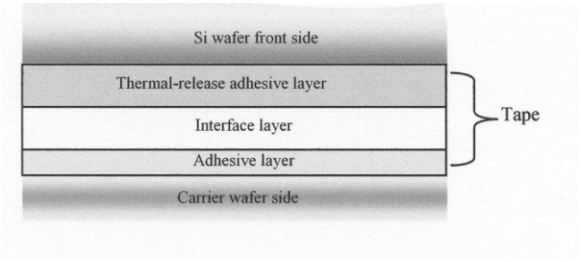

Fig. 2. Si Wafer and Carrier Wafer Assembly

The carrier wafers used in this study were single-sided polished 5" Si wafers. 75µm deep channels at 1cm spacing were created on the polished side of the carrier wafer with a dicing machine. These channels were created to eliminate air to be trapped during the taping procedure. A carrier wafer without channels was used as a control for comparison purpose.

The wafer TTV has to be determined before and after the taping procedure. This is to see the quality of work performed during the taping procedure and to be able to monitor the overall wafer TTV throughout the thinning process. The thicknesses at 14 different points on the wafer's surface are measured and recorded. Fig. 3 shows the location of these 14 points on the wafer.

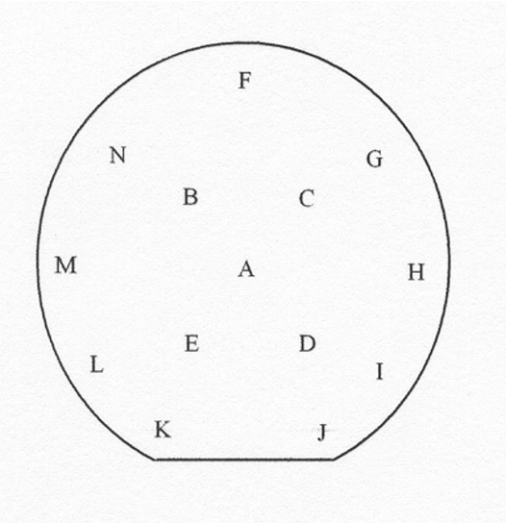

Fig. 3. Wafer Thickness Measurement Locations

2.2 Mechanical Back-Lapping

The Logitech PM5 lapping machine was utilized for the wafer back-lapping process. The lapping process is conducted by constantly wetting the lapping plate with a slurry containing abrasives. Logitech 15µm and 9µm alumina abrasives were used in this study. The 15µm abrasive falls in the large-medium range abrasive whereas the 9µm abrasive falls in the medium-small range abrasives. By using these two abrasives, the effects of abrasive size on the back-lapped wafer can be determined. The slurry composition is 200ml of abrasives mixed with 2-liters of water. This composition is based on the manufacturer's specifications.

2.3 Mechanical Polishing

For the polishing process the Logitech 5µm and 0.3µm alumina abrasives were used. The polishing slurry is prepared in the same manner as described in the back-lapping process. The mechanical polishing process is exactly the same as the wafer back-lapping process except for the type of plate used in the PM5 machine. For the polishing process the lapping plate is replaced with the polishing plate. The polishing plate is made out of aluminum with a stainless steel top. The top of the plate is covered with a consumable polishing pad made out of soft cloth (Buehler Ultra-Pad™, Ultra-Pol™ or Nylon).

2.4 Spin-Spray Wet Chemical Etching

The WS-400 spin processor built by Laurell Technologies Corporation is utilized for the spin-spray wet chemical etching process. The spin processor is made out of solid polypropylene material which is very resistant to the chemicals that are contained in the etching agent. The etching agent composition used in this research is HNO_3, phosphoric acid (HP_3O_4) and HF. The role of HP_3O_4 is to moderate the etching process. The acids are mixed to make up 2-liters of etching agent at a time. The etching agent is then poured into a Teflon coated pressure vessel and pressurized.

3. Results and Discussions

Wafers were first back-lapped utilizing 15µm and 9µm abrasives at 70rpm until slight edge cracks were visible. The lapping profile for both abrasives is shown in Fig. 4. For the 15µm abrasive, edge cracks were apparent at wafer thickness of 170µm and the wafers were completely damaged at 130µm. For the 9µm abrasive, edge-cracks were apparent at wafer thickness of 105µm, and the wafer was completely damaged at 80µm. The data indicates that the larger sized abrasive causes more wear to the wafer surface hence causing more damage to the wafer.

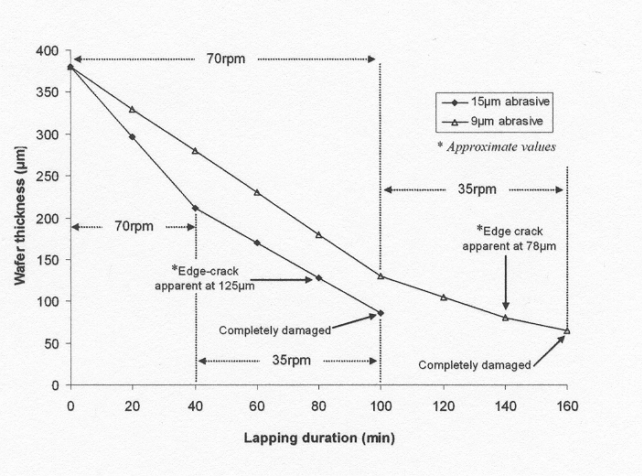

Fig. 4. Wafer Back-Lapping at 70rpm and 35rpm Plate Rotation Speed

Reducing the plate rotation speed was also conducted to see if reduction in plate rotation speed prior to the appearance of edge cracks would allow us to further back-lap the wafer without damaging it. For this study the wafers were initially back-lapped at 70rpm close to the thicknesses where edge cracks first appeared. Upon reaching that limit the lapping plate speed was gradually reduced to 35rpm.

The data in Fig. 4 indicates that by reducing plate rotation speed, the wafers can be easily back-lapped to 130µm with the 15µm abrasive and to 80µm with the 9µm abrasive. This is due to lower stress induced by the chuck on to the wafer at lower rotational speeds. Further reduction in plate speed did not enhance the lapping capability because the thinned wafer was too weak to bear the stress induced by the lapping plate and the weight of the jig. The study also shows that with the 9µm abrasive it is possible to thin wafers to less than 100µm by adjusting the lapping plate rotation speed. This is especially attractive because utilizing the 15µm abrasive would have required a switch to finer sized abrasive when wafer thickness dips below 130µm. The 9µm abrasive was chosen to be the ideal candidate for the wafer back-lapping process.

Fig. 5 shows the TTV of Si wafer that was back-lapped with the 9µm abrasive for 140min utilizing a channel free carrier wafer. From the figure we can see that after 20min of the thinning process the wafer TTV was within ±1µm. The TTV of the wafer only increased an additional ±0.5µm after undergoing 100min of the back-lapping process. However it was found that once wafer thickness reached below 100µm the overall wafer TTV suffered tremendously (±20µm). Similar results were observed for several wafers.

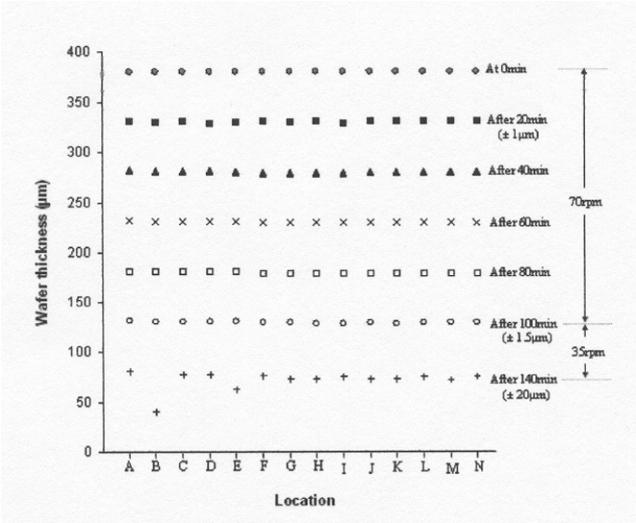

Fig. 5. TTV Results of Back-Lapped Si wafer Utilizing Channel Free Carrier Wafer

Upon closer inspection of the thinned wafer, blister like formations were found to be on the wafer surface, indicating air trapped below the wafer's surface. It is relatively easy to place the thermal release tape on the wafer (to be thinned) without trapping air, but bonding the carrier wafer on the taped wafer without trapping air was virtually impossible. Trapped air between the thermal release tape and the carrier wafer was deforming the wafer once its thickness reached below 100µm. This compromised the planarity of the wafer due to higher thinning rates at locations with large quantities of trapped air.

One solution to this problem is to conduct the whole taping assembly in a vacuum chamber. This solution was not explored because it would require additional investments to purchase a vacuum chamber and taping fixtures, and furthermore, it is deemed to be a cumbersome process. Alternatively 75µm deep channels at 1cm spacing were created on the carrier wafer with a dicing machine. These channels were created as an escape route for the trapped air while the wafer undergoes the lapping process. Fig. 6 shows scanning acoustic microscope (SAM) image comparison between two back-lapped Si wafers, whereby one was lapped with a channel free carrier wafer and the other with channels. Both wafers were back-lapped to 80µm in thickness. The images were captured through a SAM using a 75MHz transducer. From the images, we can clearly see that the channels provide an excellent escape routes for air trapped during the taping process. Hence, promising better overall wafer planarity at thicknesses below 100µm.

With the creation of these channels on the carrier wafer, the lapping process was conducted again with the 9µm

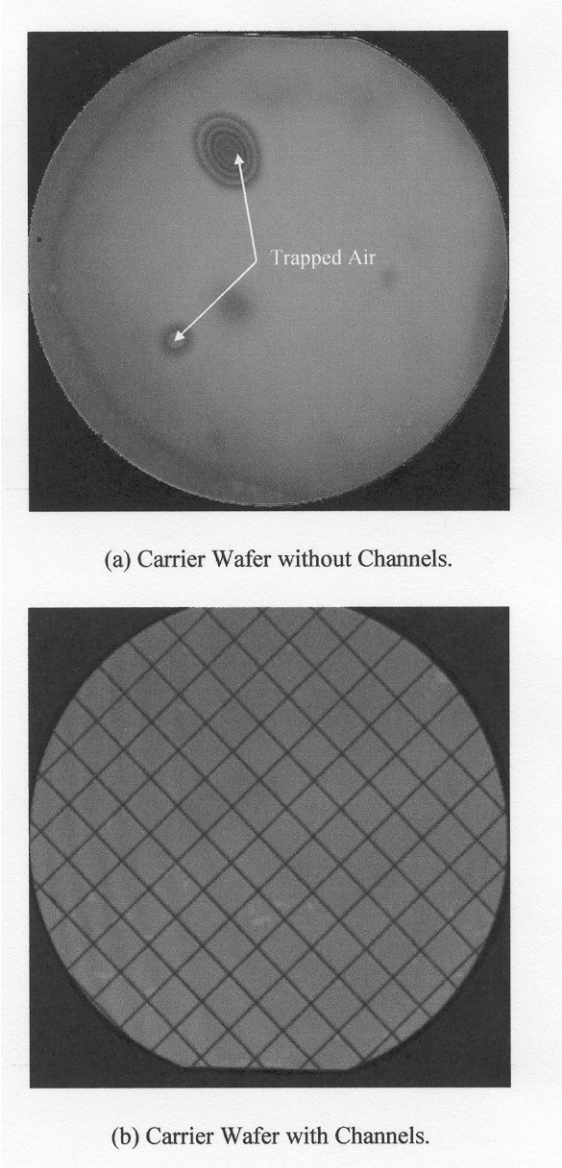

Fig. 6. SAM Image Comparison Between Two Carrier Wafers

abrasive. Fig. 7 shows the TTV results of a wafer that was back-lapped for 140min. There was a ±0.5µm increase in the overall wafer TTV when back-lapped from 100min to 140min compared to the ±20µm TTV increase obtained from the previous results. Clearly the channels have aided in removing the trapped air and improving the wafer TTV. The final wafer TTV was ±2µm.

The polishing process was conducted with 5µm and 0.3µm abrasives suspended in water. Wafers that were back-lapped to 80µm with the 9µm abrasive were polished with each of

the abrasives at 35rpm for 80min. From the study, both abrasives were found to be capable of polishing the wafer down to 50µm in thickness easily. Other than the damage

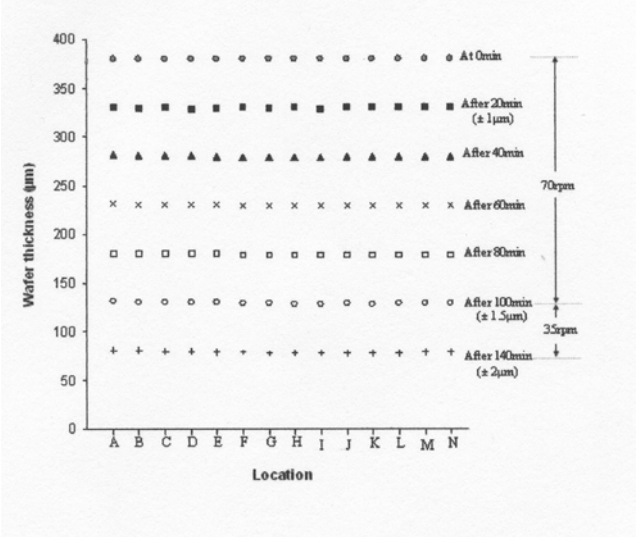

Fig. 7. TTV Results of Back-lapped Si wafer Utilizing Carrier Wafer with Channels

caused from the lapping process, the polishing process does not cause much or any additional damage to the wafer when the wafer thickness is or greater than 50µm. However, severe wafer edge damage was observed when wafer thickness reached approximately 40µm for both polishing abrasives. Since damage was observed at about the same thickness for both abrasives, it was concluded that failure was mainly due to the stress induced by the weight of the jig that holds the wafer in place via vacuum.

Figs. 8 and 9 show the thickness variation of wafers that were polished at 35rpm with 5µm and 0.3µm abrasives. The initial thicknesses of all wafers used in this study were 80µm with a TTV of ±2µm. The average thickness of the wafer polished with the 5µm abrasive for duration of 40min was approximately 51µm and the thickness of the wafer polished with the 0.3µm abrasive after 80min was approximately 50µm. The final TTV produced for the wafers polished by the 5µm abrasive were between ±4µm to ±7µm whereas for the wafers polished by the 0.3µm abrasive were less than ±2.5µm. Clearly the choice of abrasive for the mechanical polishing process is the 0.3µm abrasive.

The surface of the 50µm thick wafer produced by the 0.3µm abrasive has a close to mirror-like finish with minimal wafer edge damage. An AFM scan of the wafer surface revealed a surface roughness of 2.2nm (rms). The surface roughness on the front-side of the wafer (polished by the wafer manufacturer) is about 2nm (rms). Clearly the backside surface finish produced by the suggested polishing process is comparable to the wafer's front-side surface finish.

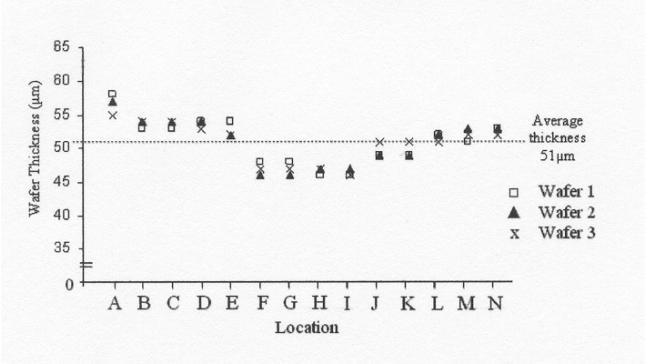

Fig. 8. TTV of Wafers Polished with 5µm abrasive at 35rpm for 40 min

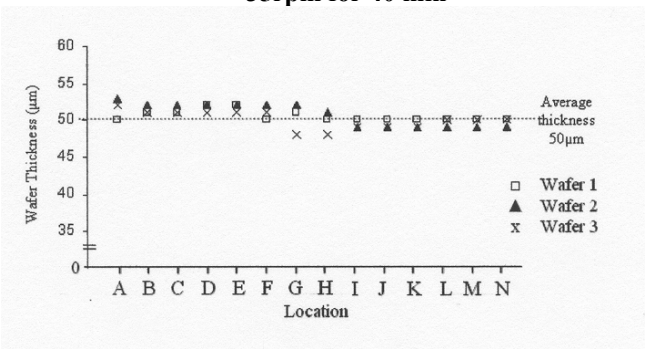

Fig. 9. TTV of Wafers Polished with 0.3µm Abrasive at 35rpm for 80min

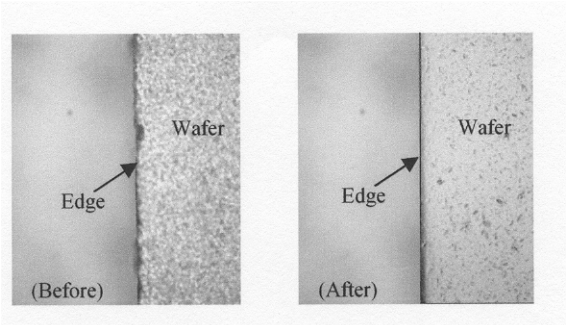

Fig. 10. Comparison of Wafer Edge Damage Before and After the Polishing Process

Fig. 10 shows two images of the same wafer edge that was taken before and after the polishing process through an optical microscope. The images reveal that the polishing process not only thins but also smoothes and removes the wafer edge damage created by the lapping process. Fig. 11 shows a portion of a 60µm thick silicon wafer (2.5" by 1") that was released from the thermal tape. The bending of the wafer indicates that most of the SSD has been removed by the polishing process. The polishing process was not

utilized to thin wafers beyond 50µm due to the extremely fragile nature of the wafer at this thickness.

The spin-spray wet chemical etch process is utilized to further thin the wafers down to less than 30µm with zero

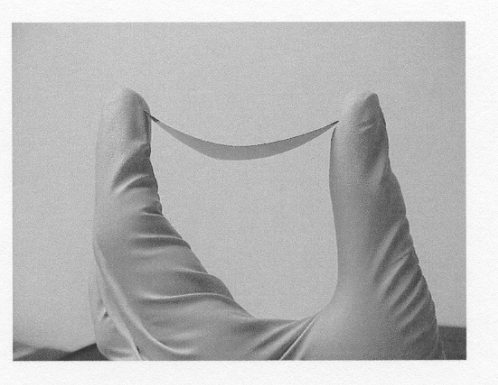

Fig. 11. 60µm Thick Polished Wafer

SSD. The material removal rate and wafer TTV is affected by several variables in the spin-spray system. These variables are the wafer rotation speed, etching agent composition and spray fan size. Hence to very quickly establish the relationship of these variables towards the etch rate and wafer TTV, a simple design of experiment (DOE) was conducted. The initial conditions are set to 100rpm for wafer rotation, 21° spray fan size created by 10psi of vessel pressure, and 70% HNO_3, 15% HP_3O_4 and 15% HF as the etching agent composition [13]. The result of the experiment is shown in Table 2.

Table 2. Design of Experiments Results for Wafer Thinning by Spin-Spray Etching Process

Variables					Effects on	
Wafer rotation speed	Spray angle	Etching agent composition			Etch rate	TTV
		HF	HNO_3	HP_3O_4		
▲	●	●	●	●	▼	▼
▼	●	●	●	●	▲	▲
●	▲	●	●	●	—	▼
●	▼	●	●	●	—	▲
●	●	▲	●	●	▲	▲
●	●	▼	●	●	▼	▼
●	●	●	▲	●	—	—
●	●	●	▼	●	▲	▲
●	●	●	●	▲	▼	▼
●	●	●	●	▼	▲	▲

Note: ● Initial Condition
▲ Increase
▼ Decrease
— Constant

3.1 Several important relationships can be established from the experiment. They are as follows:

(a) The etch rate of the Si wafer is only dependent upon two variables which are the wafer rotation speed and the etching agent composition.

(b) The TTV of the wafer, however, is dependent upon all three variables.

(c) When etch rate is increased, the wafer TTV also increases, and when it is reduced the wafer TTV is also reduced.

(d) When spray angle is increased and all other variables are maintained, the etching rate remains constant, but the wafer TTV decreases. The TTV is reduced because greater spray angles give better surface coverage of the etching agent on the wafer.

(e) When HF composition is increased, the wafer etch rate and TTV are also increased.

(f) When HNO_3 composition is increased the etch rate remains constant. This is due to the dependence of the etching rate on the rate of removal of the oxide layer. This is controlled by the HF concentration.

(g) HP_3O_4, which is a moderator for HF, decreases the etch rate when its concentration is increased, and when its concentration is increased the etch rate is reduced.

3.2 Based on the DOE results the following conditions are recommended for the variables in the spin-spray etch process:

(a) The etching agent composition should consist of ratios with high composition of HNO_3 (≥70%), moderate composition of HP_3O_4 (20%-25%) and low composition of HF (5%-10%).

(b) High wafer rotation speed (100rpm-500rpm) and maximum etching agent spray angle, which can be controlled by manipulating the etching agent storage vessel pressure (>25psi).

Based on the recommendations made, an etching agent composition of 7-parts HNO_3, 2-parts HP_3O_4 and 1-part HF was prepared to thin wafers with initial thickness of 50µm and TTV of ±2.5µm.

Fig. 12 shows the results of wafers TTV that were thinned at maximum spray angle (55° at 45psi) for various rotating

speeds. The data in Fig. 12 shows that the TTV suffers tremendously during the spin-spray process. Higher rotation speeds do improve the overall wafer planarity. This is mainly due to faster dispersion of etchant on the wafers surface. But this came with a price: extremely slow etch rates and wastage of etching agent. The approximate volume of etching agent used per wafer is 1-liter at 100rpm and at higher rotation speeds the process can easily consume 2-liters of etching agent.

The maximum spray angle produced by the nozzle in the spin-spray system is 55º. This spray angle is not enough to cover the whole wafer surface. Hence increasing the wafer rotation speed enhances the etchant coverage over the wafer surface. To further enhance the etchant coverage over the wafer, the nozzle was manually manipulated in an oscillating fashion. Fig. 13 compares the wafer TTV results produced by an oscillating nozzle and a static nozzle at a wafer rotation speed of 100rpm. Clearly by manipulating the nozzle, the wafer TTV was reduced significantly. The maximum and minimum thickness of the wafer thinned by the oscillating nozzle is 30µm and 15µm respectively. The average thickness of the wafer is 26µm and the final wafer TTV is ±7.5µm.

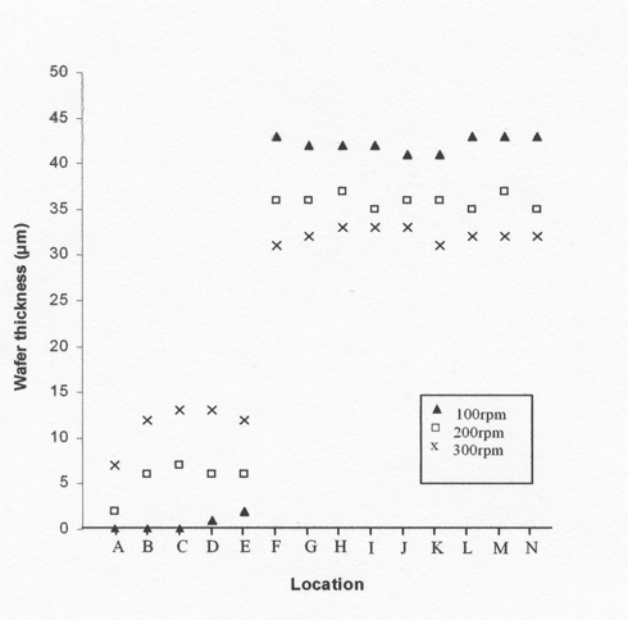

Fig. 12. Spin-Spray Etched Si Wafer TTV Analysis for Various Rotation Speeds

The surface finish of the 26µm thick (average thickness) wafer produced by the spin-spray process has a close to mirror-like finish. The surface roughness can be manipulated by reducing or increasing the HF content. Higher HF concentrations will yield higher surface roughness value and vice-versa. Fig. 14 shows the surface finishes of all three thinning processes captured through a microscope. Clearly the figure shows that surface damage (grainy spots) caused by the back-lapping and polishing process have been completely removed.

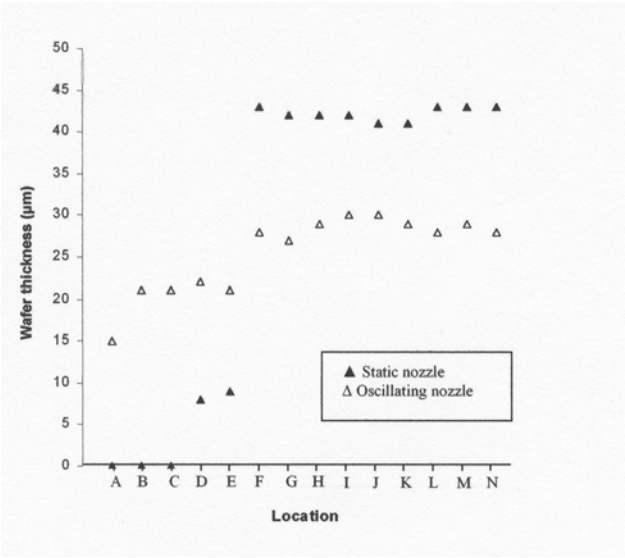

Fig. 13. Si Wafer TTV Results for Spin-Spray Etching Utilizing Static and Oscillating Spray Nozzles

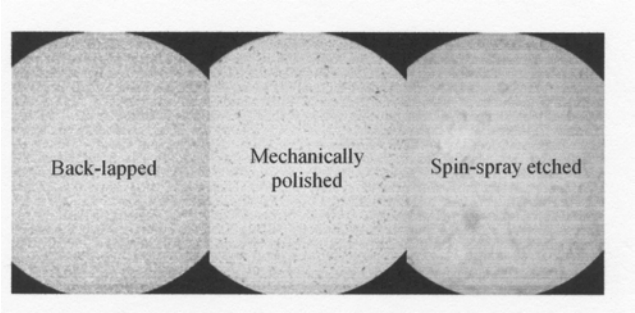

Fig. 14. Optical Micrograph of Si Wafer Surface Finishes After Various Thinning Processes

The wafers were then singulated (1cm^2 die) with a dicing saw. The diced ultra thin wafer was then placed on a hot plate kept at 90ºC. In less than two minutes the adhesion on the thermal release tape was lost. The dies were removed and die TTV were measured. Although the original thinned wafer had a TTV of about ±7.5µm, the singulated die obtained from the same wafer recorded a maximum TTV of ±0.2µm with most dies recording less than ±0.05µm TTV. Finally the thermal tape was peeled away from the carrier wafer. The carrier wafer was cleaned and dried and was ready to be used to thin a new Si wafer.

4. CONCLUSION

Three Si wafer thinning methods were used to thin wafers from 380µm to 30µm in thickness. The mechanical wafer

back-lapping method was chosen for the bulk removal process for the thinning procedure. This is followed by a combination of mechanical polishing and spin-spray wet chemical etch for the fine removal process. Two types of abrasives were considered for the lapping (15µm and 9µm) and the polishing (5µm and 0.3µm) procedures. The 9µm abrasive and 0.3µm were found to be most suitable for the thinning process. By combining these two methods, wafers were thinned down to 50µm with TTVs of ±2.5µm. The spin-spray wet etch method was utilized to thin wafers from 50µm to less than 30µm in thickness. Based DOE results, wafers were successfully thinned down from 50µm to less than 30µm with a final TTV of ±7.5µm. In conclusion a valid wafer thinning method has been demonstrated to thin 5" silicon wafers to the ultra-thin scale.

Acknowledgment

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