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Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration

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Abstract—**The design, materials, process, and fabrication of a heterogeneous integration of four chips by a fan-out panel-level packaging (FOPLP) method are investigated in this study. Emphasis is placed on (1) the application of a dry-film epoxy molding compound for molding the chips and (2) the application of a special assembly process called uni-substrate-integrated package for fabricating the redistribution layers (RDLs) of the FOPLP. The Ajinomoto build-up film is used as the dielectric of the RDLs and is built up by the semiadditive process. Electroless Cu is used to make the seed layer, laser direct imaging is used for opening the photoresist, and printed circuit board (PCB) Cu plating is used for making the conductor wiring of the RDLs. The panel dimensions are 508 × 508 mm. The package dimensions of the FOPLP are 10 × 10 mm. The large chip size and the small chip sizes are, respectively, 5 × 5 mm and 3 × 3 mm. The uniqueness of this study is that all the processes are carried out by using the PCB equipment.**

Keywords—**FOPLP, heterogeneous integration, reconstituted panel, redistribution layers**

Introduction

Moore's law [1] has been driving the system-on-chip (SoC) platform. Especially in the past 10+ y, SoCs have been very popular for smartphones, tablets, and the like. SoCs integrate different-function interated circuit (ICs) into a single chip for a system or subsystem. Two typical SoC examples are shown in Fig. 1 (sources from Chipworks and SystemPlus Consulting). The application processor (AP) A10 is designed by Apple and manufactured by Taiwan Semiconductor Manufacturing Company (TSMC) using its 16 nm process technology. It consists of a six-core graphics processor unit (GPU), two dual-core central processing unit, two blocks of static random access memories, etc. The chip area is 125 mm^2 and has 3.3 billion transistors. The AP A11 is also designed by Apple and manufactured using TSMC's 10 nm process technology. The A11 consists of more functions, including a tricore Apple-designed GPU, a neural engine for face ID (identity), etc. However, because of the Moore's law, i.e., the feature size is from 16 nm down to 10 nm, the chip area is about 30% smaller than that of the A10 and there are 4.3 billion transistors.

Why is heterogeneous integration of such great interest [2-14]? One of the key reasons is because the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make SoCs. Some of the early researches in heterogeneous integration have been provided by Georgia Institute of Technology [2-4], where they reported a differential Si complementary metal-oxide semiconductor (CMOS) receiver IC (operating at one Gbps) integrated with a large-area thin-film InGaAs/InP I-metal-semiconductor-metal (MSM) photodetector (Fig. 2).

Heterogeneous integration contrasts with SoCs in the following manner. Heterogeneous integration uses packaging technology to integrate dissimilar chips with different functions from different foundries, wafer sizes, and feature sizes (as schematically shown in Fig. 3) into a system or subsystem, rather than integrating most of the functions at the chip level, using finer feature sizes. For the next few years, we will see higher levels of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, or cost. Heterogeneous integration is going to take some of the market share away from SoCs for high-end applications such as high-end smartphones, tablets, wearables, networkings, telecommunications, and computing devices. System-in-package (SiP) [15-25] is similar to heterogeneous integration except less dense, larger pitch, and simpler. How should these dissimilar chips talk to each other? The answer is: redistribution layers (RDLs) [26, 27]. How should those RDLs be made? They can be made by fan-out wafer (FOW)/panel-level packaging (PLP) methods [28-33]. In this study, we use fan-out panel-level packaging (FOPLP) technology because it is a higher throughput process and has a potentially lower cost than fan-out wafer-level packaging (FOWLP).

In this article, the feasibility of a chip-first and die facedown FOPLP of a heterogeneous integration of four chips is demonstrated. To have a very high-throughput and low-profile package and save the epoxy molding compound (EMC), a

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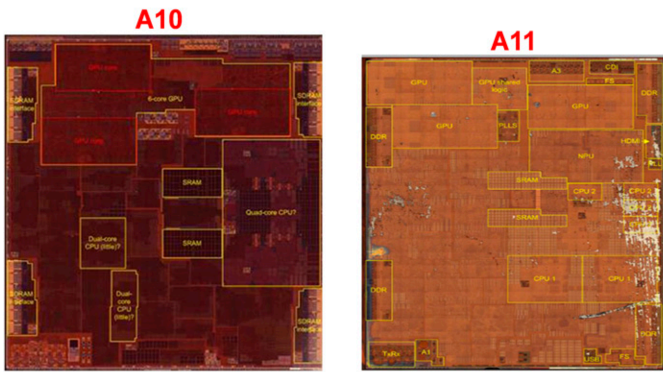

Fig. 1. SoC platforms for the A10 and A11 APs.

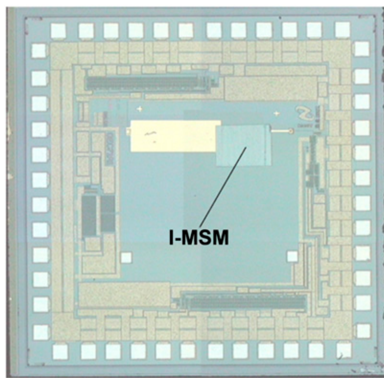

Fig. 2. InGaAs/InP I-MSM integrated onto differential Si CMOS receiver IC.

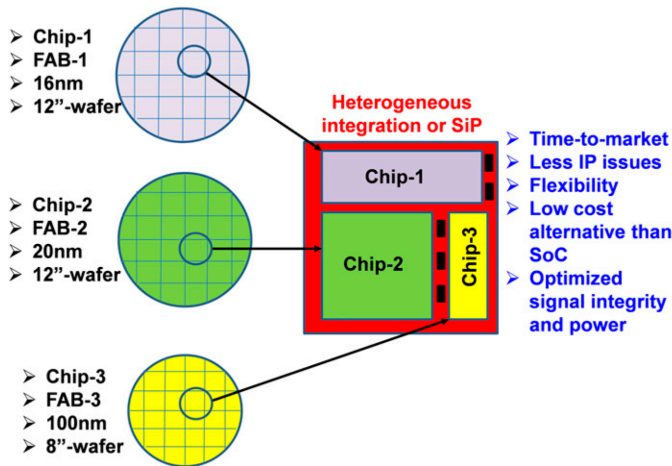

Fig. 3. Heterogeneous integration or SiP.

process called uni-substrate-integrated package (Uni-SIP) [11] is used to fabricate the RDLs. Unlike in [11], the panel dimensions in this study are 508 × 508 mm and a dry-film EMC is laminated on the reconstituted panel (instead of the liquid EMC with compression molding as in [11]).

The Uni-SIP process starts off by attaching the backside of the ECM panel on both sides of a coreless panel substrate with an epoxy resin. (In this study, chips embedded in the dry-film EMC is called the ECM panel.) The RDLs are formed on both surfaces

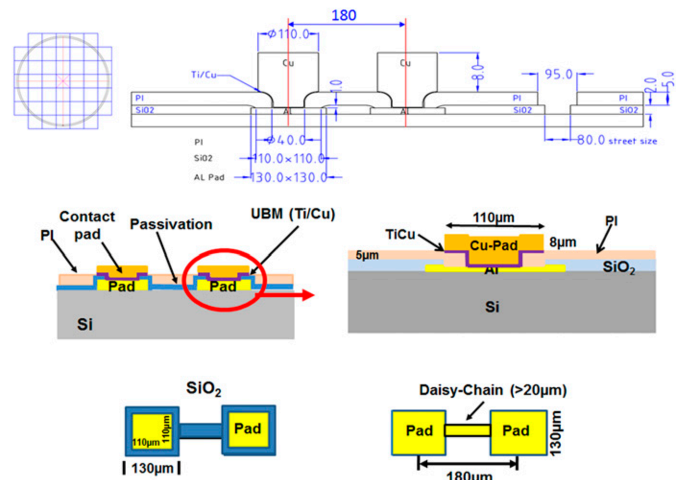

Fig. 4. Cross section of the test chips.

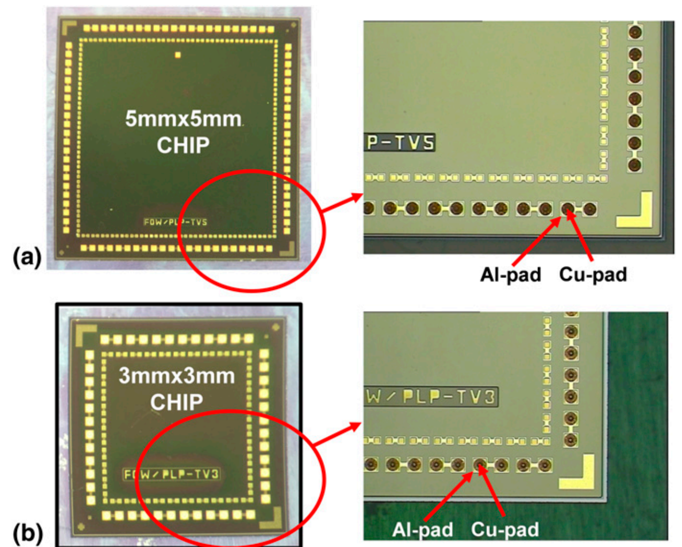

Fig. 5. Test chips. (a) 5 × 5 mm. (b) 3 × 3 mm.

of the ECM panels. The Ajinomoto build-up film (ABF) is used as the dielectric of the RDLs and is built up by semiadditive process. Electroless Cu is used to make the seed layer, laser direct imaging (LDI) is used for opening the photoresist, and printed circuit board (PCB) Cu plating is used for making the conductor wiring of the RDLs. The solder mask is then applied on both sides of the ECM panel leaving pad openings for surface finishing. The ECM panels with build-up RDLs are finally separated from the coreless panel substrate mechanically. It is followed by solder-ball mounting and dicing. This process adds a new dimension in high-throughput and thin fan-out packaging without using semiconductor equipment.

Test Chips

Figs. 4 and 5 show the test chips (5 × 5 mm and 3 × 3 mm) under consideration. The layout of the test chip is shown in Fig. 4, and the fabricated chips are shown in Fig. 5. It can be seen

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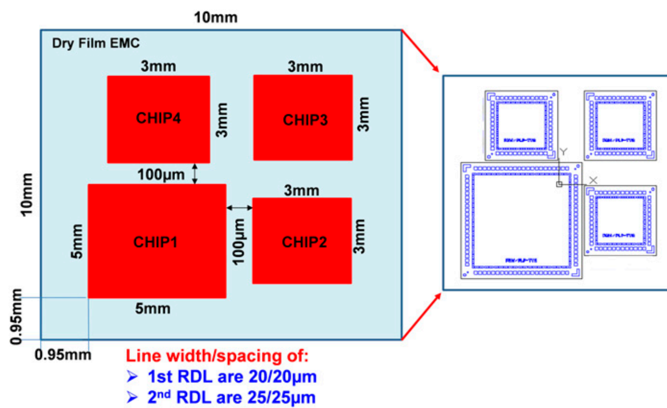

Fig. 6. Test package. One 5 × 5-mm chip and three 3 × 3-mm chips. Package dimensions = 10 × 10 mm.

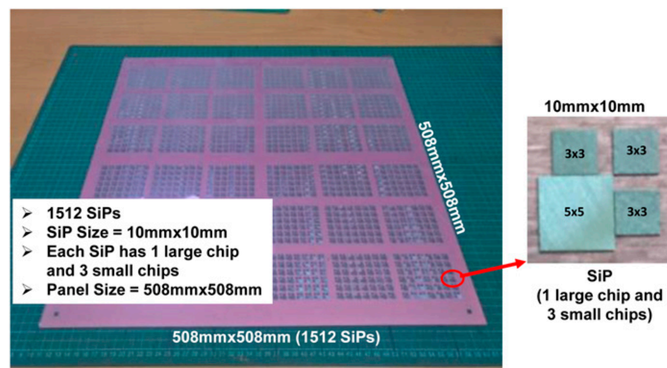

Fig. 7. Reconstituted panel (508 × 508 mm) with 1512 SiPs, and each SiP with four chips.

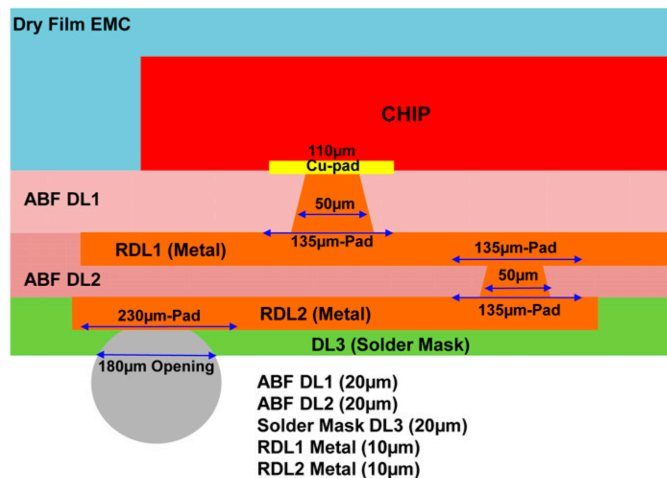

Fig. 8. Cross section of the test package.

that, for the 5 mm × 5 mm × 150 µm chip, there are 88 pads with a pitch = 180 µm (the outer rows). The polyimide opening of the Al pad is 40 µm in diameter and is 5 µm thick. The SiO_2 passivation opening of the Al pad is 110 × 110 µm, and the size of the Al pad is 130 × 130 µm. The Cu contact pad is 110 µm in diameter and is 8 µm tall from the Al pad.

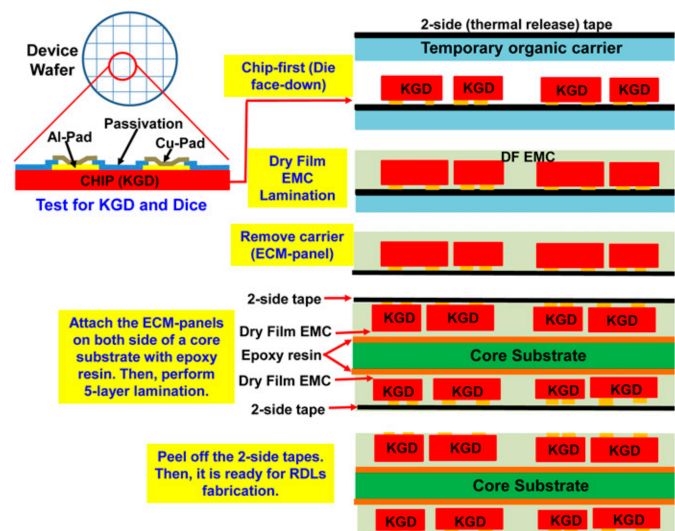

Fig. 9. Uni-SIP key process steps.

The dimensions of the small chip are 3 mm × 3 mm × 150 µm as shown in Fig. 5. It can be seen that there are 48 pads on a 180-µm pitch (outer rows). The cross section and dimensions of the pads of the small chip are the same as those of the large chip.

Test Fan-Out Package

Fig. 6 schematically shows the test package under consideration. The dimensions of the test package are 10 × 10 mm, and it consists of one large chip (5 × 5 mm) and three small chips (3 × 3 mm). In real applications, the large chip could be an AP and the small chips could be memory. The spacing (gap) between the large chip and the small chip is 100 µm. These packages are to be made from a 508 × 508 mm reconstituted panel as shown in Fig. 7.

Fig. 8 schematically shows the cross-sectional view of the test package. It can be seen that there are two RDLs, and the thickness of the metal of RDL1 and RDL2 is 10 µm. The line width and spacing of the metal of RDL1 are 20 µm, and those of RDL2 are 25 µm. The dielectric layer thickness of DL1, DL2, and DL3 is 20 µm. The via through the first dielectric layer (DL1), connecting the Cu contact pad of the test chip to the first RDL (RDL1) is 50 µm in diameter. The pad diameter on the RDL1 is 135 µm, which is connected to RDL2 through the via with a diameter of 50 µm. Similarly, the pad diameter on the RDL2 is 135 µm. Finally, 230-µm solder-ball Cu pads are formed on RDL2. The opening of the solder mask (DL3) is 180 µm. The solder ball size is 200 µm, and the ball pitch is .4 mm.

Dry-Film Lamination and Uni-Substrate-Integrated Package Process

Fig. 9 shows schematically the FOPLP with chip-first and die face-down assembly process. Basically, work must be carried out on the device (test chip) wafer (Fig. 9 [left]) and the reconstituted panel (Figs. 9a-f).

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Table I
Material Properties of the Dry-Film EMC

T_g (°C) (dynamic mechanical analysis (DMA))	167
T_g (°C) (thermomechanical analysis (TMA))	157
CTE (30-150°C) (ppm/K) (TMA)	7
CTE (50-150°C) (ppm/K) (TMA)	7
CTE (150-240°C) (ppm/K) (TMA)	21
Young's modulus (MPa)	7,000
Elongation (%)	1
Poisson's ratio	.25

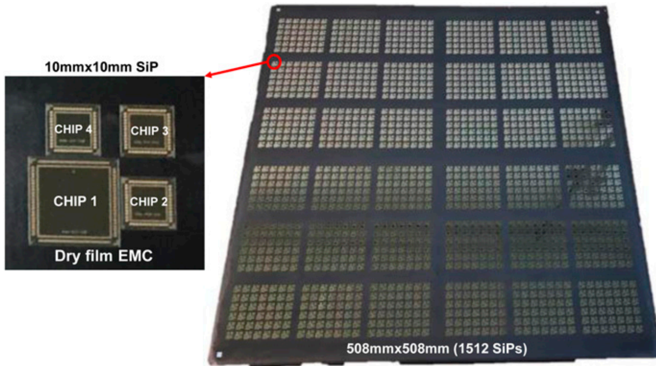
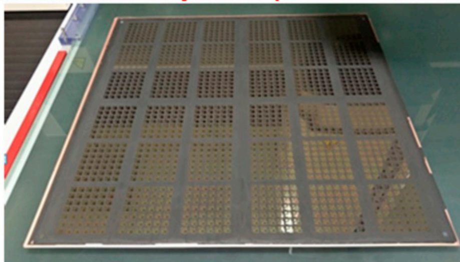


Fig. 10. Uni-SIP (view from the front side).



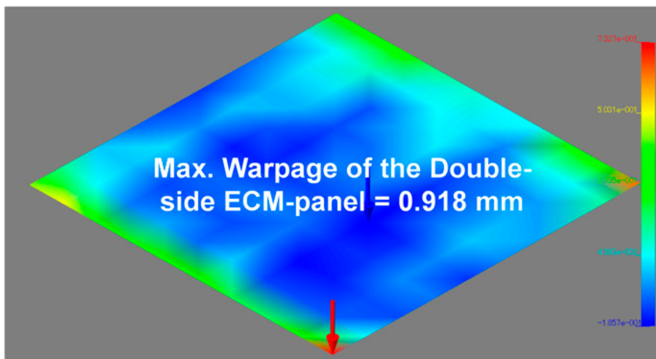


Fig. 11. Warpage of the double-sided ECM panel.

As shown in Fig. 4 and the left-hand side of Fig. 9, the original device (test) wafer must be modified with a Cu pad on top of the Al pad. Then, dice the wafer into individual known-good dice or test chips.

On the 508 × 508-mm reconstituted panel (in this case, it is a piece of organic carrier), first attach a two-side thermal release

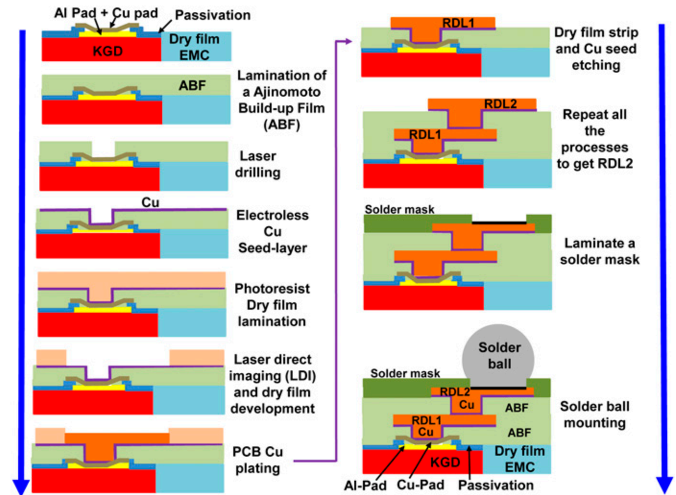


Fig. 12. Uni-SIP process steps in making the RDLs.

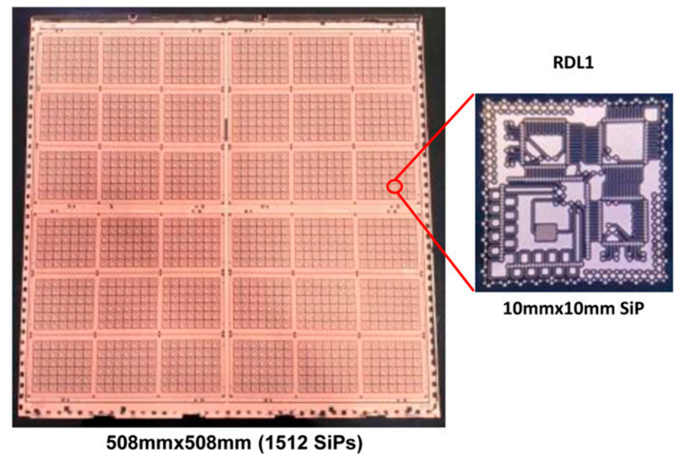


Fig. 13. RDL1 (line width and spacing = 20 μm).

tape, Fig. 9a. Then, pick and place the test chips (face-down) on the tape, Fig. 9b. It is followed by laminating (pressure = .8 MP, temperature = 110°C, and annealing at 180°C for 60 min) a dry-film EMC on top of the reconstituted panel as shown in Fig. 9c. The material properties of the dry-film EMC are shown in Table I and the EMC is placed about 140 μm above the backside of the chips. Then, removing (debond) the carrier, we have the ECM panel as shown in Fig. 9d. It is followed by stacking the backside of two ECM panels on a core substrate with an epoxy resin on both sides, and by the standard PCB lamination process (.68 MPa and 180°C for 30 min), the Uni-SIP structure (Fig. 9e) is obtained. It is followed by peeling off the tape (Fig. 9f). The Uni-SIP as shown in Fig. 10 is ready for fabricating the RDLs from the Cu pads on both sides.

The de-taping was very successful and there was no evidence of EMC cracking. The warpage of the de-taped double-sideed ECM panel (Uni-SIP) was .918 mm as shown in Fig. 11.

Fig. 12 shows the process steps in fabricating the RDLs for the Uni-SIP structure from the Cu pads on both sides of the structure. First, laminate an ABF on both sides of the structure. Then, laser drill the ABF and stop at the Cu pad (this is the

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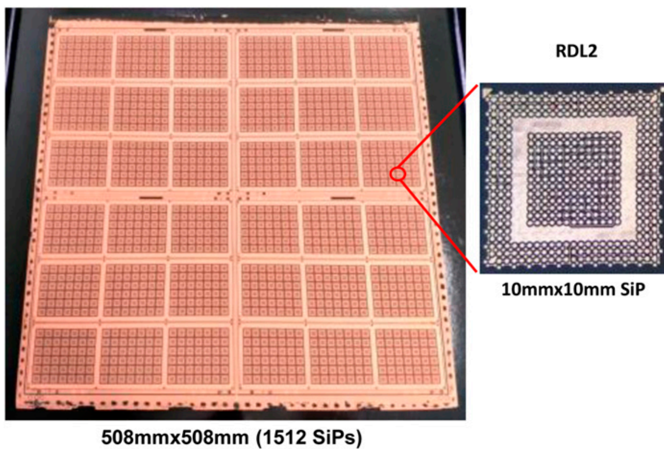

Fig. 14. RDL2 (line width and spacing = 25 μm).

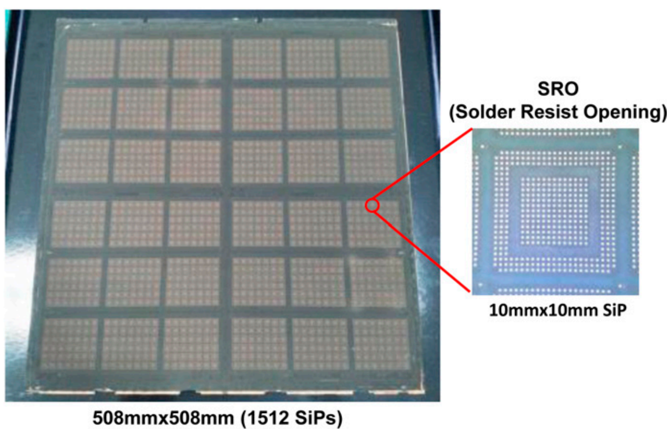

Fig. 15. SRO of the double-sided ECM panel.

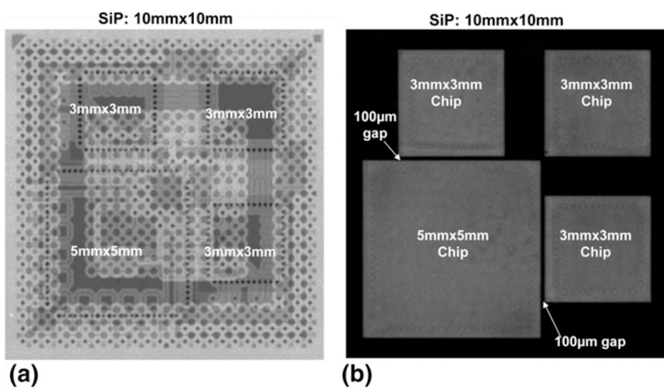

Fig. 16. (a) x-ray image of the individual SiP of four chips. (b) C-mode SAM image of the individual SiP of four chips. There is no void between the chip gaps.

reason for making the Cu pad on the device wafer). It is followed by electroless Cu seed-layer plating. Then, laminate a photoresist dry film. It is followed by LDI and dry-film development. Then, PCB Cu plating, dry-film striping, and Cu seed layer etching. RDL1 is obtained (Fig. 13).

Repeat all the processes to get RDL2 (Fig. 14). It is followed by laminating a solder mask and making the SRO (solder resist opening), Fig. 15. Then, mechanically debond the ECM panels from the core substrate.

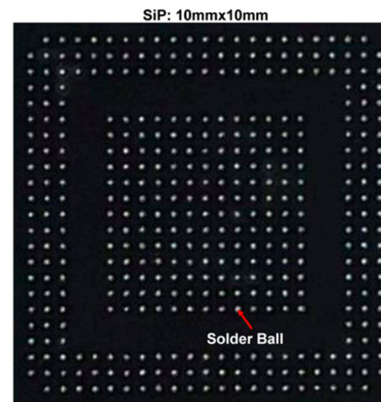

Fig. 17. Bottom view of the individual SiP showing the solder ball distribution.

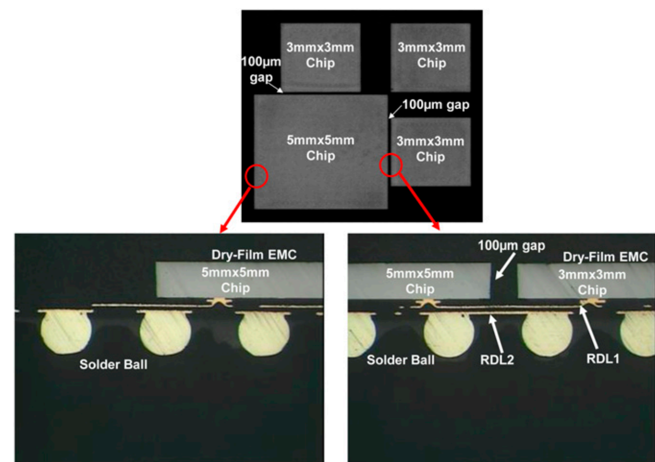

Fig. 18. Cross-sectional views of the individual SiPs.

Fig. 16a shows the x-ray image of the individual heterogeneous integration package of four chips and RDLs. Fig. 16b shows the C-mode scanning acoustic microscope (SAM) image of the individual SiP of four chips and dry-film EMC. It can be seen that: (1) the chips are properly placed and molded, and (2) there is no void in the dry-film EMC and between the gap (100 μm) of the chips.

There are two different stencils for the solder ball mounting: one is for stencil printing the flux, and the other is for stencil mounting the solder balls. The solder (Sn3wt%Ag0.5wt%Cu) balls (200-μm diameter) used are from Indium. The peak temperature for solder reflow is 245°C. Fig. 17 shows the bottom side of the individual SiP. It can be seen that there are 405 solder balls.

Fig. 18 shows the cross sections of the heterogeneous integration of four chips. It can be seen that (1) there are two RDLs, and (2) the chips, RDLs, and solder balls are properly assembled.

Summary and Recommendations

Some importat results and recommendations are summarized as follows:

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1. A very low–profile (390 μm) heterogeneous integration of four chips by a FOPLP method has been successfully designed and fabricated.
2. A very low–cost dry-film EMC has been successfully laminated on the 508 × 508-mm reconstituted panel with 1512 SiPs.
3. There are no voids in the dry-film EMC or the gaps (100 μm) between chips.
4. A very high–throughput Uni-SIP process for fabricating the RDLs has been demonstrated.
5. The de-taping of the ECM panel did not cause any EMC cracking.
6. The maximum warpage of the double-sided ECM panel (Uni-SIP structure) is .918 mm, which is less than the allowable (1 mm).
7. Thermal cycling and drop tests should be applied to the test samples to verify their reliability. These will be the next tasks of this project.

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