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Electromigration in Power Devices: A Combined Effect of Electromigration and Thermal Migration

Hao Zhuang,* Robert Bauer, and Markus Dinkel

***Abstract*—In the power semiconductor industry, there is continuous development toward higher maximum current capability of devices while device dimensions shrink. This leads to an increase in current density which the devices have to handle, and raises the question if electromigration (EM) is a critical issue here. Generally, an EM failure can be described by the Black's equation with temperature and current density as the main influencing factors. Normally, the current that the power packages need to handle lies in the range of 100 A. However, it should be noted that power devices exhibit asymmetric sizes of drain and source contacts. This may lead to higher current density at the source leads (area ratio drain/source: ~9× for PQFN 5 × 6). Nevertheless, the source lead area is still much larger than that of the flip chip bumps (i.e., 28 times larger than a 100-μm microbump). This typically enhances the safety of the power device with respect to EM. However, with regard to future development toward higher maximum current capability, we intended to investigate further on the EM of power devices. In the present work, we focused on the PQFN 5 × 6 package to study the EM behavior of a power device soldered on a printed circuit board (PCB). We employed the highest current (120 A) and temperature (150°C) that the stress test system could handle to study EM in accelerated mode. First fails occurred after ~1,200 h, which was much earlier than expected from previous flip-chip investigations. In addition, we found separation gaps in the solder joint between drain contact and PCB, which experienced the lowest current density in the whole test. Contradictorily, we observed only minor solder degradation at the source interface, regardless of the higher current density there. Nevertheless, the separating metal interfaces still correlated well with the current direction. Thermal simulations revealed that due to the self-heating of the device by the high current applied, both the drain and source leads were exposed to much higher temperatures (Tmax = 168°C) than the PCB board which was kept under temperature control at 150°C. This temperature difference resulted in a thermal gradient between the device and PCB, which, in turn, triggered thermal migration (TM) in addition to EM. As TM for the drain contact occurred in the same direction as EM, it enhanced the degradation effect and therefore led to a shorter time-to-failure at the drain. In contrast to this, such an enhanced effect did not occur at the source side. As a result, we observed higher solder degradation at the drain side, which we did confirm by switching the current direction in the test. To minimize the TM effect, a special EM test vehicle, which used a Cu plate instead of the metal-oxide-semiconductor field-effect transistor chip, was designed and fabricated. Thermal simulation verified that the device operated at similar temperatures as the PCB board. Using this setup, it was possible to study EM in an accelerated mode and, thus, investigate the pure EM behavior of the power device.**

***Keywords*—Electromigration, thermal migration, power devices, solder joint**

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Infineon Technologies AG, Am Campeon 1-15, Neubiberg 85579, Germany
*Corresponding author; email: hao.zhuang@infineon.com

Introduction

In the past years, the demand in power electronics has significantly risen because of the rapid development of data centers, electric vehicles, telecommunication, etc. All these innovations have strongly driven power device development toward higher maximum current capability while, at the same time, shrinking their dimensions [1]. Such trends have resulted in one fact: those power devices need to handle more and more increasing current density. Therefore, a natural question arises: What is the maximum current a power package can handle in the system? To answer this question, it is essential to understand the behavior of the solder joint under current flow, the more so as most package-related failures reported have been due to the failure of solder joints [2].

It is widely accepted that when current is flowing through the solder joints, the momentum transfer occurs between conduction electrons and metal ions in the solder. This leads to material transport within the solder in the direction of electron motion, an effect well known as electromigration (EM) [3]. Generally, EM-induced failures can be described by Black's equation [4]:

$$\text{Mean time to failure (MTTF)} = \frac{A}{j^n} e^{\left(\frac{E_a}{kT}\right)}.$$

Here, A is a constant, j is the current density, the exponent n is a model parameter, E_a is the activation energy, **k** is the Boltzmann constant, and T is the absolute temperature in Kelvin. The system-specific values for **A**, n, and E_a can be obtained by fitting the experimental data of a given package-solder system. Therefore, for a given material system, current density and temperature are the main influencing factors with respect to EM. In the past years, EM has been intensively studied in flip-chip solder joints. As a result, current densities of 10^3-10^4 A/cm^2 typically trigger EM in solder bumps [5]. For power packages, however, studies on EM have been rather rare so far. One limiting reason might be that because of larger connection areas of drain and source contacts in power packages, the risk for EM has been considered rather low. However, since power packages usually operate at currents of tens of

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amperes or even higher, solder joints and contact areas are exposed to relatively high current densities. Considering the widely used PQFN 5 × 6 power packages as an example (Fig. 1), operation currents of 80 A, which is one of the normal operation current of the device during application, add up to a current density of 1.2×10^4 A/cm^2 at the source leads (Fig. 1a). Even for package versions with increased source footprint area (Fig. 1b), the current density of 4.4×10^3 A/cm^2 at 80 A is considered to be high enough to trigger EM in the Sn-Ag-Cu (SAC) solder joint between device and printed circuit board (PCB).

It is noteworthy that most power devices exhibit a special configuration of the electrical contact: the drain contact is much larger than the source leads. Take the package in Fig. 1b e.g., the current density at the drain side is only ~1/9 of the current density at the source side. The drain side of the chip usually is attached directly to the die pad, whereas the source is connected to the source leads via wire bonding or a Cu clip.

Considering the future development toward higher maximum current capability of power devices, we wanted to better understand the EM limits of such power packages. In the current study, we focused on the solder joint between package and PCB. There, usually, SAC solder is used. This is because the Pb-based solder inside the package is much more resistant to EM failure [6]. The study was mainly carried out using a 5 × 6 PQFN package as the test vehicle due to its wide usage.

Experimental Setup and Analysis

A. Test setup

Fig. 2a shows the schematic cross-sectional illustration of the standard commercial PQFN package used in the current study. The product comprises the following elements: A metal-oxide-semiconductor field-effect transistor (MOSFET) chip is soldered on the Cu lead frame using Pb-Ag-Sn solder. The connection of the chip top and the source lead was established via a Cu clip. The whole device was encapsulated in an epoxy molding compound. A five-layer PCB with 1.5-mm thick Cu core was used as the test board. The device was soldered onto the test board via the SAC solder. During test, electrons flowed from the source side of the PCB through the device toward the drain side, as indicated by the dashed red line in Fig. 2a. The board temperature was regulated by a temperature sensor attached at the side of the device, as shown in Fig. 2b. In the first EM tests, we applied a current of 120 A and a temperature of 150°C to the device shown in Fig. 1b, from which we have observed the strong thermal migration (TM) effect during our test. To minimize TM effect, a special EM setup using Cu plate instead of MOSFET chip is designed. The test on this test vehicle is carried out at a current of 40 A and a temperature of 150°C.

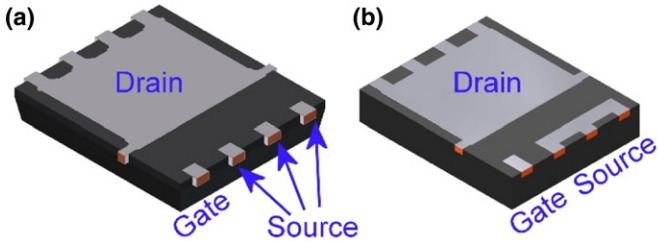

Fig. 1. PQFN power package with (a) standard leads and (b) fused leads.

B. Analysis

During the EM test, the resistance of the solder joint increased as the test progressed. There are two reasons behind this: on the one hand, the formation of Kirkendall voids at the interface reduced the cross-sectional area available for electrical conduction. On the other hand, the extended formation of Cu-Sn intermetallic phases with higher electrical resistance inhibited current flux. However, it was not feasible to use the increase in resistance of the whole system alone to evaluate solder degradation, because the resistance of solder joints only contributes to a small portion of the overall system resistance, whereas it varies from device to device [7]. The most practical way to notice a solder degradation turned out to be detecting electrically open contacts, at the solder contact between board and device, that is, the device failing the electrical test. However, once the device would have been driven into this stage, a sudden local increase in the temperature would occur because of the said increase in resistance. This would lead to local damage of the device and melting of the solder. Fig. 3 depicts one device that electrically failed after the EM test. The clip and chip were completely damaged/molten. The same applied to the solder joint between device and test board. In this context, the

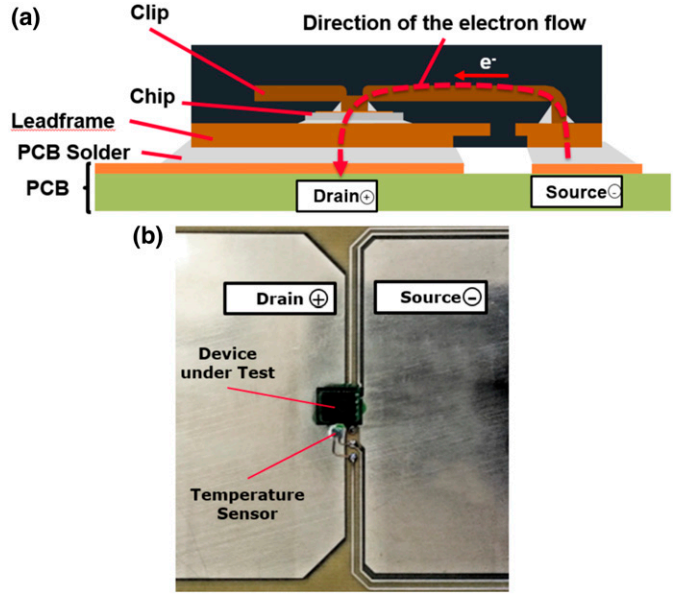

Fig. 2. (a) Schematic illustration of PQFN package used in the current study and (b) a photo of the test system including the device and the temperature sensor on the board.

Fig. 3. Cross-sectional image of an electrically failed device after the EM test.

information on the status of the solder before device failure, i.e., intermetallic phase formation and voiding, was no longer available. In this regard, whenever a sample failed in the test, we inspected those samples that were still functioning. Of course, this procedure was not equivalent to the desired direct observation of the solder joint before failure, but it shed some light on the overall status of the solder joints at this stage. Cross-sectional samples were prepared by embedding the samples in a resin for mechanical polishing, followed by Ar ion milling [7]. In this way, we were able to better distinguish the intermetallic phases. SEM and optical microscopy were employed to record cross-sectional images of the samples.

Finite element method (FEM) simulations were conducted to analyze the temperature distribution within the device during EM testing. The simulation was based on the assumption of free convection while the current was fixed at 120 A. Different board temperatures were simulated to analyze the temperature distributions inside the package and at the leads.

Results and Discussion

In the first EM test, we used a PQFN 5 × 6 package with fused leads (Fig. 1b). We applied a current of 120 A and a temperature of 150°C to the device to obtain maximum acceleration according to Black's equation. The first device failure was observed at 1,200 h when the electrical resistance increased drastically and an open circuit was observed. Surprisingly, the failure is at the drain side, which will be discussed in the next paragraph in detail. Actually, at a testing duration of 1,100 h, there is slight increase in resistance. Afterward, the resistance increases continuously until fail at ~1,200 h, as shown in the inset of Fig. 4. The board temperature is regulated by the temperature sensor to be constant at 150°C. In one of our previous studies of EM in flip-chip solder bumps, no failures had been observed until the end of the test after 4,800 h at a current density of 6.7 kA/cm^2 and testing temperature of 150°C. In the current study, the application of 120 A corresponded to a current density of 6.6 kA/cm^2 at the source leads where the highest current density would be expected. In this context, an early failure at 1,200 h was a very surprising finding. As mentioned in the previous section, this device was severely damaged because of high temperature associated with the failure, for which reason little information about the actual condition of the solder joints could be obtained. As a result, we inspected another sample from the same group, which had been retained after 740 h of testing time.

The results from cross-sectional analysis on the retained samples are shown in Fig. 5. The positions of the cross-sections in Figs. 5b-d are marked in Fig. 5a. The arrows indicate the directions of electron flux. In the solder underneath the drain and source contacts, significant growth of intermetallic phases is observable. To qualitatively identify the composition of the intermetallic phase in the solder joint, elemental mapping of Sn, Cu, and Ag by means of energy-dispersive X-ray spectroscopy (EDX) was carried out in the selected area (indicated by blue rectangles) in Fig. 5b. The results hereof are depicted in Figs. 5e-h. Three regions with different Sn and Cu contents can be observed. In the area directly adjacent to the source contact of the device, marked by a blue line, the intermetallic phase was identified to Cu3Sn, exhibiting the highest Cu percentage. Adjacent to this region, the Cu6Sn5 intermetallic phase is present, marked by a red line. The remaining solder was identified as Sn. This observation strongly indicates that Cu migrates from the board to the device on the source side, that is, along the direction of electron flux, and in good agreement with the predictions of EM modeling [8]. In addition to the growth of intermetallic phases, the formation of voids was also observed in the solder region close to the board. These voids, also known as Kirkendall voids [8], form because of the high concentration of vacancies existing at the Cu/Cu3Sn interface. During the diffusion of Cu, coalescence of those vacancies leads to void formation [8]. In general, the formation of the Kirkendall voids in the solder is driven by diffusion. In the current study, EM, TM

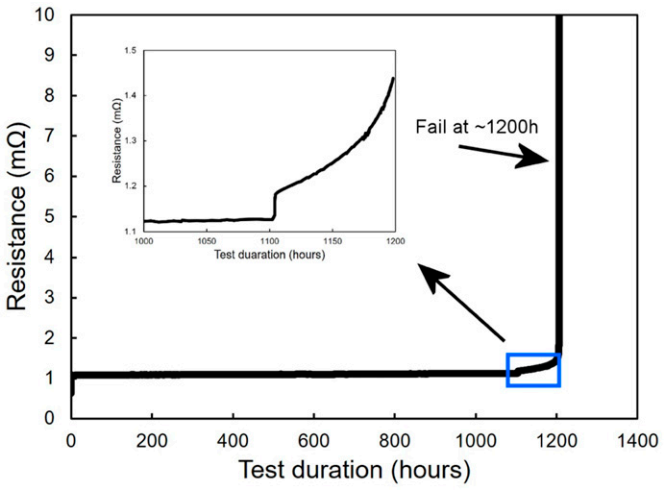

Fig. 4. Electrical response of the first device in the test group that shows electrical failure during the test. Inset shows the enlarged curve for the test duration between 1,100 and 1,200 h.

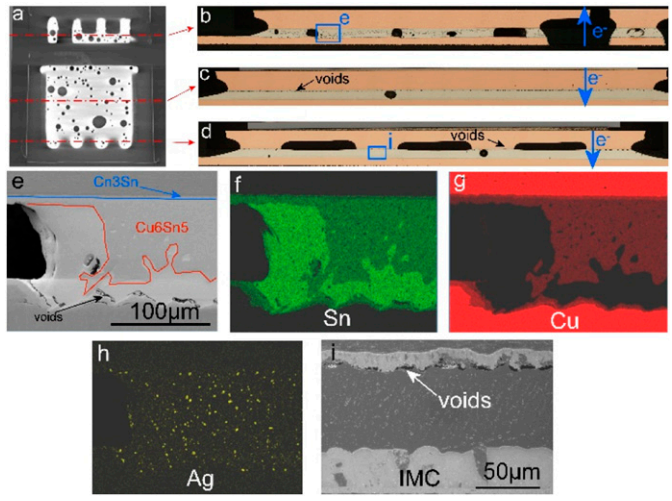

Fig. 5. Physical inspection of the sample after 740 h EM test. (a) X-ray image. The red line indicates the position of the cross-section: (b) through the gate and source leads, (c) in the center of the drain pad, and (d) across the drain fingers; (e) SEM image of the selected area in (b); (f)-(h) EDX mapping of (e); (i) SEM image of the selected area in (d). The package here is PQFN 5 × 6 with fused leads.

(will be explained later), as well as the high temperature during the test would lead to the diffusion in the solder joint, which in turn results in the formation of the Kirkendall voids. Kirkendall voids play an important role in determining the lifetime of the solder joint. At the source side, they only appear in certain regions while most of the source areas are still void-free. Similar phenomena—void formation and enhanced growth of intermetallic phases—were also observed on the drain side, as indicated in Figs. 5b, 5c, and 5i. Since the electrons flow from the device to the board in the drain solder region, the Cu6Sn5 phase grows close to the PCB board, and the voids are present directly below the drain contact of the device, as expected. However, a large amount of Kirkendall voids was also observed in the drain solder, and the solder nearly fully degraded underneath the drain pad (Figs. 5c and 5d). This finding was significantly different from the amount of Kirkendall voids expected in source solder, in which most of the solder area turned out to be void-free (Fig. 5b). Moreover, this finding was very surprising and unexpected because the current density at the source contact was 9.15 times higher than that at the drain contact. According to our previous study and the literature, the model parameter n for current density in the Black's equation ranges in between 1.7 and 2.1 for SAC solder [9-11]. Even if we assumed a conservative model parameter n of 1.7, the EM impact at the source contact is 43 times stronger than that at the drain contact, on a condition that the temperatures of both contacts be similar. In this context, the stronger Kirkendall void formation in the drain solder was unexpected.

To verify whether the aforementioned phenomenon was a one-time or systematic effect, we performed scanning acoustic tomography (SAT) analysis on the devices at earlier stages of the EM test. The results are depicted in Fig. 6. SAT is known of its high sensitivity in detecting voids at interfaces. In SAT images, dark regions typically indicate good interface adhesion without any voids, whereas white regions represent an interface with delamination and/or voids. As shown in Fig. 6a, at the very early stage of the test (44 h), regions of voids readily formed at the drain contact. In Fig. 6a, one of those regions is marked by a thin red line. The contrast, however, is quite low, implying the small amount of the voids. When the test was continued up to 216 h, the area of voiding at the drain and the observed contrast increased significantly, indicating a drastic increase in voids. Further continuation of the test up to 310 h lead to a further growth of voids, which eventually almost covered the whole drain area (Fig. 6c). Nevertheless, the device still did not fail the EM test because there were still some areas without voids available for current flux. In contrast to the drain contact, the source leads were all free of voids. This observation confirmed that there was indeed stronger solder degradation and void formation at the drain contact in our current EM test, regardless of the much lower current density there.

Based on Black's equation, two factors determine the EM failure of a given system: current density and temperature. Therefore, better understanding of the temperature differences in the solder joint between the source and drain would help one to understand the significant differences in solder degradation characteristics there. In the current study, the board temperature was regulated by a temperature sensor placed next to the device (Fig. 2b). However, it turned out to be very difficult, if not impossible, to accurately measure the solder temperature directly without disturbing the test. In this regard, FEM simulations were used to shed some light on the temperature distribution within the tested system. Table I summarizes the highest temperatures of the chip, source lead, and drain lead at different test temperatures while keeping the current constant at 120 A. Because of this high current, considering the electrical resistance of the MOSFET chip, its power dissipation resulted in higher device temperatures. The chip temperature is in general ~20 K higher than that of the set board. As a consequence, a higher temperature at the source and drain leads was to be expected in comparison with the board. Both the peak temperatures at the source and drain leads were at a similar level: 169°C at the drain leads and 168°C at the source leads, which means the impact of temperature solely on the EM in both drain and source solder was at the same level. However, the significant differences in temperature between board and device resulted in a temperature gradient in the solder joint, with higher temperature on the device side and lower ones on the board side. It is well understood that a temperature gradient induces TM in the solder [12]. A gradient of 400°C/cm or even lower is sufficient to trigger TM at a driving force comparable to EM at a current density of 10^3 A/cm^2 [12-14]. This corresponds to a temperature gradient of only 4°C for a bond line thickness of 100 μm. In this context, TM was not negligible at all in the present EM test because the device was at a significantly higher temperature than the board. TM rather drove Cu material in the solder from the hotter side (device) toward the cooler side (board) [12], for both drain and source contacts. Not to mention, this additional TM effect significantly complicated an interpretation of the intended EM test. As illustrated in Fig. 7, the TM-induced Cu migration occurred into the opposite direction of EM in the source solder, which annihilates the effects of EM expected there. On the other hand, Cu migration induced by TM occurred in the same direction as that of EM in the drain solder, effectively enhancing the EM-induced diffusion. This effect eventually led to stronger Cu migration at the drain side than that at the source side.

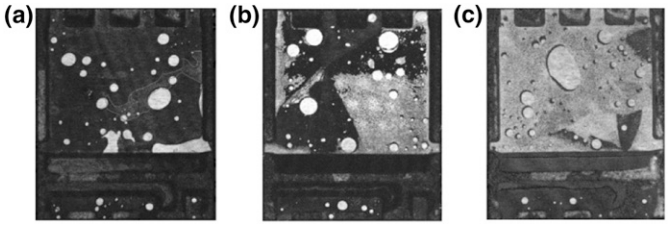

Fig. 6. SAT pictures of devices after certain EM test duration: (a) 44 h, (b) 216 h, and (c) 310 h.

Table I
Maximum Temperatures at Different Locations with Different Test Temperatures; the Current Is Kept at 120 A

T_{test} (°C)	T_{chip} (°C)	$T_{source\ lead}$ (°C)	$T_{drain\ lead}$ (°C)
50	70,79	68,99	68,26
80	100,86	99,01	98,27
120	140,91	139,02	138,27
150	170,99	169,06	168,29

Consequently, Kirkendall voids form earlier at the drain side despite the lower current density.

From the aforementioned discussion, it could be concluded that the drain contact, where electrons flow from the device toward the PCB board, would experience enhanced Cu migration by TM and EM, which in turn would lead to earlier formation of Kirkendall voids there. This effect occurs independently of whether the current density at the drain pad is higher or lower than that at the source contact. This is a systematic consequence of the current test setup: if we changed the current direction in our test device, we would observe the early formation of Kirkendall voids at the present "source" contact that has smaller area. To further confirm this, we used a QFN 3×3 package with flip-chip configuration for the EM test. Fig. 8 shows the cross-sectional analysis of the device after 550 h EM test. As expected, a large amount of Kirkendall voids again formed in the solder underneath the drain contact, which now featured a smaller area and thus higher current density in comparison with the source contact. By contrast, the source solder only exhibited a very small amount of Kirkendall voids, confirming our hypothesis.

In field applications, devices such as our test vehicle normally operate at relatively low current levels, e.g., 50 A in the server application for the PQFN 5×6 devices. Under this condition, the temperature gradients in the solder joint and the resulting TM are negligible. In this context, the high TM induced in the current test setup would lead to the misinterpretation of test results and could not deliver a correct guidance for EM behavior of that power device in the field application. To solve this dilemma, a special EM test vehicle was designed and fabricated. A PQFN 5×6 package with standard leads, as shown is Fig. 1a, was used to this end. Fig. 9a shows the cross-sectional image of the device. A Cu plate was built into the package instead of a MOSFET chip. By doing so, the electrical resistance of the device was reduced to .16 mΩ, which is around seven times lower than that of the initial testing device. Moreover, instead of all three source leads, only the central source lead was connected to the board to enable electron flux. In this way, a lower current of 40 A could be applied to the device while keeping the current density at the source lead still relatively high at 1.8×10^4 A/cm^2. By doing so, we were able to reduce the self-heating and thus TM effects of the device during the EM test. Thermal-electrical simulation was carried out to analyze the temperature of the leads at a board temperature of 150°C. The results are shown in Fig. 9b and 9c. Because of the current crowding effect, the highest temperature appeared at the clip area close to the lead that carries the current. Nevertheless, this hotspot was not in direct contact with the solder. The maximum temperature at the source lead that carried a current was 154°C, whereas the highest temperature at the drain contact was 152°C. This was indeed very close to the board temperature of 150°C and should therefore be able to significantly reduce the TM. The improved EM test has run so far up to 1,000 h without any electrical fails. Results of an intermediate check of the cross-sections after testing times 500 and 1,000 h are shown in Fig. 10. As expected, enhanced formation of intermetallic phases can be observed at

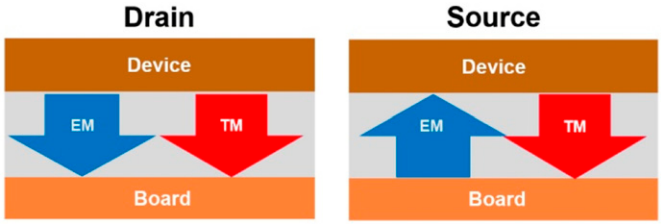

Fig. 7. Illustration of the EM- and TM-induced Cu migration at the drain and the source solder.

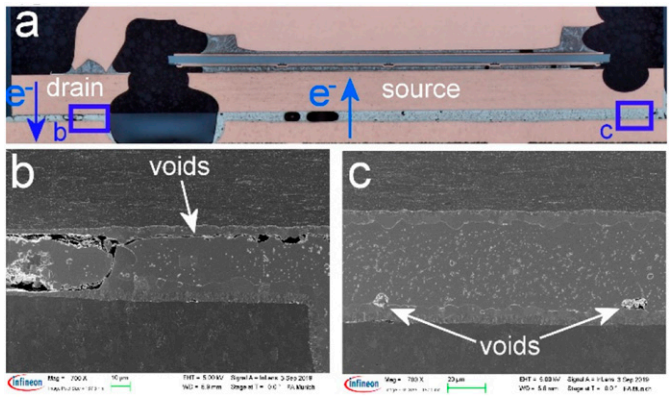

Fig. 8. QFN 3×3 package with flip-chip configuration after 550 h EM test. (a) Overview of the cross-section and the arrows indicates the directions of the electron flow, and (b) and (c) SEM images of the selected area in the drain and the source solder.

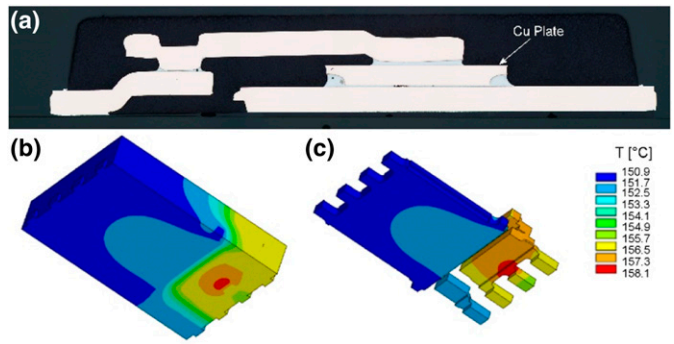

Fig. 9. (a) Cross-sectional image of the special EM test vehicle. (b) A Cu plate was used instead of the MOSFET chip to lower the electrical resistance of the device. (c) FEM simulation of the temperature distribution of the device under test.

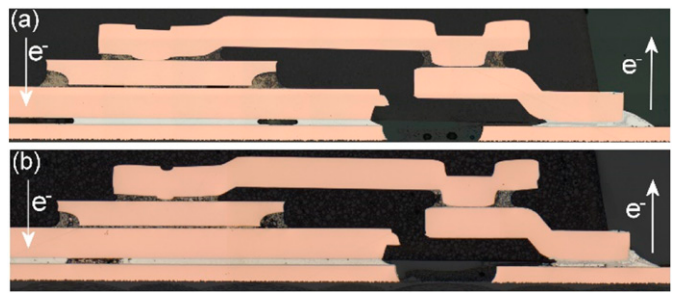

Fig. 10. Cross-sectional images of the EM test vehicle after (a) 500 h and (b) 1,000 h EM test.

the source solder. Sporadic formation of voids in the source solder is also observable. With the test continuing to 1,000 h, the intermetallic phases grow further in the source solder, and more voids are observed. By contrast, the drain solder remains nearly unchanged with very moderate growth of the intermetallic phase being visible. This observation confirms that the pure EM behavior of the power device can be studied using this special EM test vehicle. Making use of such vehicles could therefore pave the way to providing guidelines for the future development of EM-robust power devices. Further studies are currently ongoing to better understand the limitations of EM on the current rating of the power devices based on the present test vehicle.

Conclusions

In this study, we used QFN packages to study the EM behavior of power devices on PCB. In a first set of experiments, active devices with MOSFET chips in the package were used. A significant amount of Kirkendall voids were observed in the solder under the drain pad after the EM test by 150°C@120 A. Surprisingly, only sporadic Kirkendall voids were observable in the source solder. Thermal simulations were carried out to understand the temperature distribution in the test vehicle. It was shown that drain and source leads were at similar temperatures (Tmax ~168°C for both drain pad and source leads) during the EM test, with the board temperature settled at 150°C. The higher temperatures at the drain and source leads created a temperature gradient in the solder between the device and PCB, resulting in TM within the solder. At the source side, TM compensated the effects of EM, whereas it enhanced the EM-induced diffusion at the drain side, which in turn leads to the enhanced formation of Kirkendall voids in the solder there. As a result, for the current EM test setup, the drain side always failed earlier than the source side. This was further confirmed by switching current direction during the test. Nevertheless, in field applications, corresponding devices seldom work under conditions as extreme as in our EM test. In particular, such large temperature gradients in the solder joint usually do not exist in standard applications. Therefore, the accelerated EM test in the current study was judged not to be representative. To solve this dilemma, a special EM test vehicle, which uses a Cu plate instead of the MOSFET chip, was designed and fabricated to minimize self-heating and thus TM in the test device. Thermal electrical simulation revealed that the drain and source leads were only slightly heated up to a maximum temperature of 154°C at a board temperature bound to 150°C. During the first EM test on this device, it turned out that the source leads with higher current density are more sensitive to EM, as expected. In the current study, we could only qualitatively identify the EM and TM behavior of the power device on the PCB board. By employing the EM test vehicle of Cu plate, we expect that we can suppress the TM effect by keeping the temperature gradient as low as possible so that we can obtain the "pure" EM behavior of the solder joint. By doing so, we hope it is possible in the future to quantitatively estimate the EM and TM contribution in the application. This forms the target of our future work.

Acknowledgments

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