Journal of Microelectronics and Electronic Packaging (2020) **17**, 99-105

ISSN: 1551-4897

High-Temperature Double-Layer Ceramic Packaging Substrates

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***Abstract*—A double-layer ceramic electronic packaging technology that survives the Venusian surface temperature of 465°C was developed using a ceramic interlayer dielectric with gold conductors. A 60-μm ceramic interlayer dielectric served as the insulator between the top and bottom gold conductors on high-purity ceramic substrates. Test devices with AuPtPd metallization were attached to the top gold pads using a thick-film gold paste. Thermal aging for 115 h at 500°C and thermal cycling from room temperature to 450°C were performed. Dielectric leakage tests of the interlayer ceramic layer between the top and bottom gold conductors revealed a leakage current density of less than 50×10^{-7} A/cm^2 at 600 V after thermal cycling. Gold conductor resistance increased slightly after thermal cycling. The die shear test showed a 33% decrease in die shear strength after thermal tests and its 6.16 kg-F die shear strength satisfies the Military Standard Product Testing Services (MIL-STD) method.**

***Keywords*—High-temperature electronics packaging substrate, ceramic insulator, double-layer packaging substrate**

Introduction

High-temperature resilient electronics are desired to process, amplify, and transfer reliable data under extreme operating conditions. Specifically, high-temperature electronics that can survive 500°C require special material and packaging considerations. For high-temperature electronic systems, multilayer packaging substrates are desired to improve its packaging density. The specific objectives are to develop a multilayer high-temperature capable ceramic packaging architecture using metal-interconnect technology for harsh environment applications at 500°C. Besides hot planet applications, this high-temperature packaging technology is applicable in various industries, such as geothermal energy production, oil and gas exploration, and nuclear energy. The available packaging technology and electronics which are currently being used in these industries are limited by operational temperature (typically below 300°C) and the package's reliability issues [1].

There are numerous types of substrate for high-temperature applications: the commonly used are high temperature cofired ceramics (HTCCs), high-purity alumina substrates, and low temperature cofired ceramics (LTCCs) [2]. Each of these high-temperature substrates has its advantages and disadvantages, such as different conductivities, parasitic noises, and dielectric constants at high-temperature and high-frequency operations. For example, having numerous choices of electrical conductors for the cofiring process and low cofiring temperature (875°C) are advantages of LTCC alumina substrates. Also, the LTCC alumina consists of glass constituents being able to be cofired with a conductor with a melting temperature below the alumina sintering temperature [3]. However, the glass constituents cause degradation in dielectric constant at high temperatures. The high-purity (96-99%) alumina substrates have a smaller conductivity and dielectric changes at high temperatures (above 400°C). The dielectric constant of 96% alumina substrate is higher than that of the LTCC alumina substrate from room temperature (RT) to about 300°C, but the dielectric constant of the LTCC suddenly increases at the temperatures above 300°C [4]. Among high-temperature substrates, the 96% alumina substrates have a higher dielectric performance at higher temperatures [5]. So, the high-purity alumina substrates have been selected as the high-temperature substrates because these substrates are capable of withstanding 500°C operation temperature. However, the conventional HTCC process requires extreme high firing temperatures around 1,600°C that renders only certain refractory metals be used as their electrical conductors. Table I briefly shows the pros and cons of HTCCs, LTCCs, and their applications.

These refractory metals have low conductivities and require extensive investigations of the suitability of the conventional wire bonding, die-attach, and encapsulation materials and processes.

There are different types of substrate and low-temperature bonding techniques that are capable to withstand high temperature. The low-temperature glass powder was directly bonded to ZnS ceramic at a temperature between 400°C and 450°C which was subjected to have a low mechanical strength, but Xu et al. [7] suggest doping the $PbTiO_3$ particle to enhance the bonding mechanical strength. There are different applications for ZnS ceramic substrates, such as aerospace and aircraft window which used to yield poor safety and reliability results. but Zhang et al. [8] used Ni-P coating on ZnS transparent ceramic and soldered that with Sn-3Ag-05Cu at low temperature to increase the mechanical and bonding strength reliability. Different types of die attach material can be used for high-temperature electronic packaging, such as nano-silver, nano-solder, surface plasma, nano-welding, and carbon nanotubes [9]. Each die-attach material and technique have their advantages and disadvantages, and it varies depending on the package's application, operating temperature, and atmospheric condition.

The manuscript was received on April 26, 2020; revision received on June 27, 2020; accepted on July 2, 2020

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doi:10.4071/imaps.1123535

Table I
HTCC and LTCC Comparison and Their Application [3, 6]

	LTCC	HTCC
Pros	Low cofiring temperature Stable permittivity (ε_r = 3-10) More cofired conductor choices	Higher stability at high-temperature and high-frequency applications Relatively lower conductivity
Cons	Low thermal conductivity (3-4 W/m-K) Higher shrinkage rate during the firing Higher dielectric constant (>300°C)	Higher firing temperature (>1,600°C) Fewer cofired conductor choices
Application	Microelectronic packaging Microwave	High frequency and high temperature Aerospace

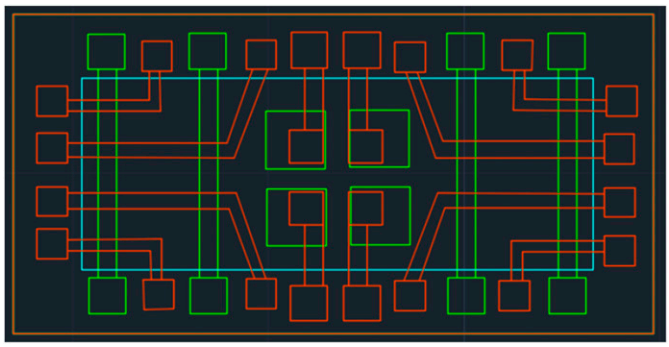

Fig. 1. Mask layout: red (bottom conductors), green (top conductors), and blue (interlayer ceramic).

For instance, at high-temperature applications, there are common issues that affect the package's performance, such as thermo-migration, delamination, mechanical strength, and degradation of material properties which could be respectively due to the coefficient of thermal expansion (CTE) mismatch, grain boundaries growth, high-temperature, and harsh environment exposure [10].

In this work, a double-layered ceramic packaging technology using gold die-attach, gold conductor, ceramic substrate, and ceramic interlayer is investigated. The die-attach materials (alumina-based ceramic and thick-film gold pastes) were evaluated on the double-layered ceramic substrates. The ceramic interlayer was used to serve as the interlayer insulator between the top and bottom gold interconnects. Thermal cycling from RT to 450°C and 500°C exposure for 115 h (additional test was performed for 1,540 h) was performed to evaluate the reliability of these double-layered ceramic substrates. Die shear tests were carried out on the packaging substrate to evaluate the mechanical properties of the ceramic interlayer. A dielectric test was performed to evaluate the ceramic interlayer insulation properties before and after environmental exposure.

Experimental Approach

A. Materials Overview

The 98% alumina substrates (CoorsTeK, Golden, CO) and the high-temperature ceramic adhesive (503 VFG [very fine grain], Aremco Products, Inc., Valley Cottage, NY) were used. The 8835 gold cermet (8835 gold paste) conductor (ESL 8835 [520C] 9802A, Electro-Science Laboratories, King of Prussia, PA), 3066 fireable gold thick-film paste (3066/3068N Wire-Bondable Au Conductors), and 4007 Brazeable Au conductor were purchased from Ferro corporation (Mayfield Heights, OH). Also, the electrical-grade adhesive back Kapton® polyimide film (50 μm thick) was purchased from McMaster-Carr (Robbinsville, NJ).

B. Substrate Fabrication

Fig. 1 shows the three mask layers for the double-layered ceramic substrate test vehicle. There are two conductor layers; the red conductors are on the bottom of the ceramic substrate, whereas the green conductors are on the top of the ceramic interlayer dielectric (blue). The main goal of these interconnect patterns is to check for the interlayer insulation between the top and bottom interconnects. Four die-attach sites were designed as a part of the top gold conductor for die-attach and die shear tests. An aluminum frame mesh screen was used to screen print the 3066 gold paste onto the alumina substrate to create the gold interconnects for interconnecting electronic components. The process flow for the ceramic packaging substrate preparation is shown in Fig. 2.

After the 3066 gold paste screen printing, the gold interconnects were fired using a three-step firing profile: 3-4-min leveling at RT, 10-15 min at 100-120°C in an air-circulated box furnace, and final firing at a peak temperature of 850°C for 10 min with a heating up and cooling down rate of 45°C/min. The first-layer gold interconnects after firing are shown in Fig. 3a. A promising adhesion was observed for these gold conductors on the ceramic substrate based on the shear test results. After screen printing the 3066 gold paste, the ceramic pastes 503 VFG were screen printed on the packaging substrate as an interlayer ceramic insulator. The ceramic layer was cured using a four-step profile: 1-h RT settling time followed by 2 h at 94°C, 260°C, and 372°C sequentially.

Before screen printing, the 3066 gold paste on top of the ceramic interlayer, a diluted 503 VFG ceramic paste layer (503 VFG:503 VFG thinner [503 VFG-T], 5:1), was printed on the top of the ceramic interlayer to mitigate voids or crevices to prevent gold diffusion into the ceramic interlayer dielectric. This thin diluted 503 VFG layer also helps enhance the adhesion of the top gold conductors to the ceramic interlayer dielectric and mitigates the delamination of the top gold conductors. The diluted 503 VFG ceramic paste has a similar four-step curing profile as the nondiluted 503 VFG paste: 1-h RT settling time followed by 2 h at 94°C, 260°C, and 372°C, sequentially. The

ceramic interlayer thickness including the additional 503 VFG thinner is 60 μm as shown in Fig. 3b. As shown, the bottom gold conductors can be vividly seen through the interlayer ceramic dielectric.

Next, the 3066 gold paste was screen printed on the cured ceramic interlayer using aluminum frame screen printing mesh with a stencil and was followed by the same three-step firing profile: 3-4-min leveling at RT, 10-15 min at 100-120°C in an air-circulated furnace, and final firing at a peak temperature of 850°C for 10 min with a heating up and cooling down rate of 45°C/min. The top fired 3066 gold conductor thickness is about 25 μm Fig. 4a shows the top gold conductor layer after fabrication.

To increase die shear strength for the dice, an additional layer of a 4007 Brazeable conductor was printed on 3066 gold conductors to provide an Au-rich barrier layer on the substrate for the die-attach pads. A three-step firing profile was used: 3-4-min leveling at RT, 10-15 min at 100-120°C in an air-circulated furnace, and final firing at a peak temperature of 850°C for 10 min with a heating up and cooling down rate of 45°C/min. A gold/platinum/palladium (AuPtPd) thick film was screen printed on the backside of the silicon wafer and then diced to 2.6 mm by 2.6 mm test dice. The gold paste was cured using a two-step curing profile: 10-min RT settling time and 15-min drying step at 125°C, followed by 15-min firing at a temperature of 580°C with a temperature ramp-up rate of 25°C/min. The fabricated substrate with the four attached dice is shown in Fig. 4a and 4b.

The step coverage of the top gold conductors is an important consideration given the thickness of the interlayer ceramic dielectric is 60 μm Figs. 5a and 5b show a good step coverage of

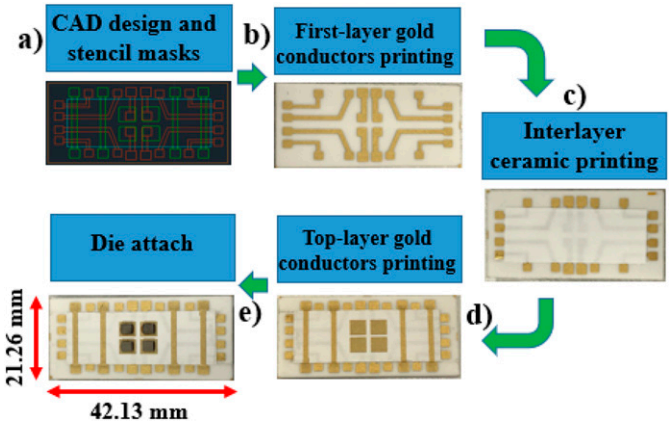

Fig. 2. Process flow for the ceramic packaging substrate fabrication.

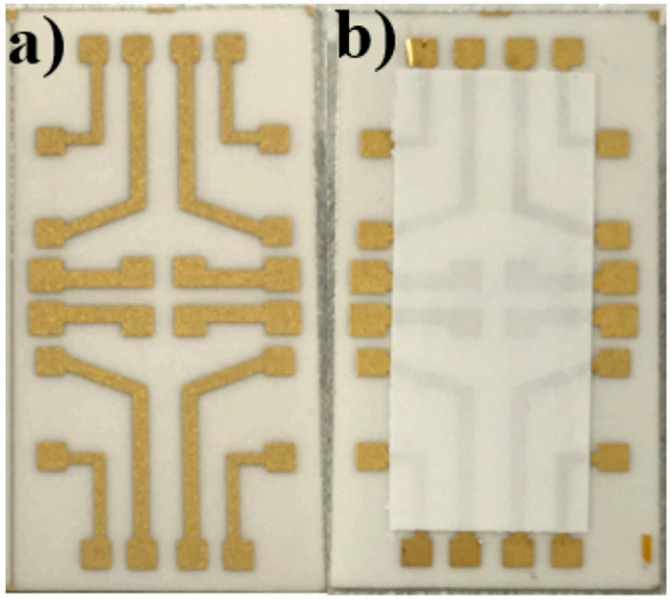

Fig. 3. (a) Gold thick-film interconnects on the alumina substrate, (b) with a top ceramic interlayer.

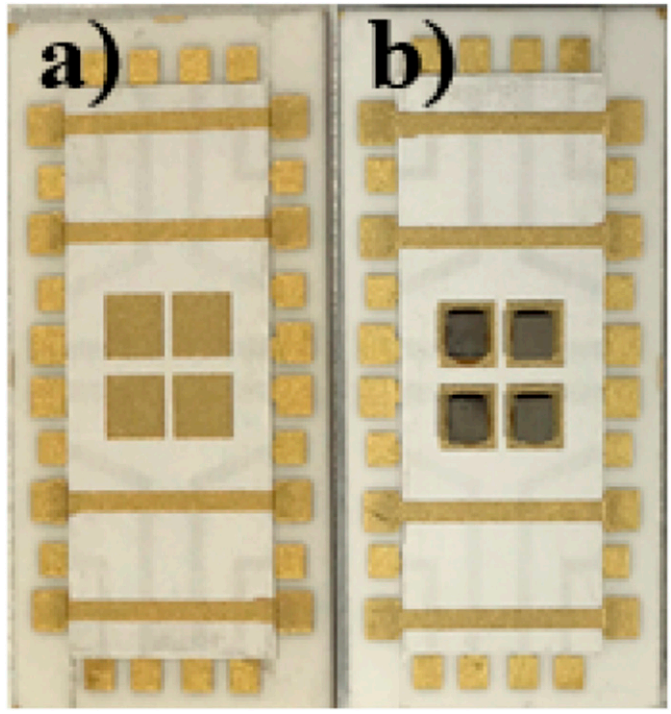

Fig. 4. (a) Top gold conductors, (b) after die-attached to the substrate.

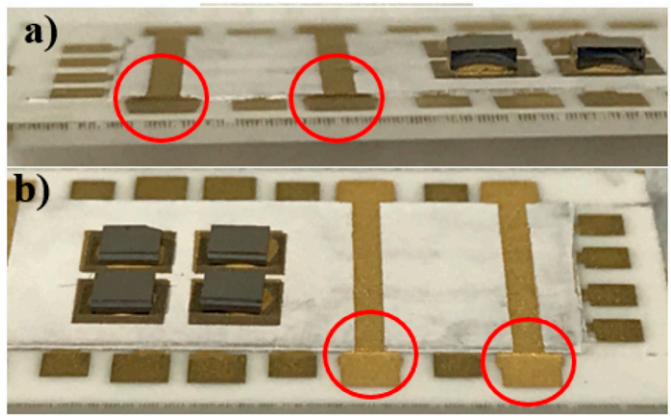

Fig. 5. (a and b) Continuity of the top gold conductors.

two of the top gold conductors. A continuity test was performed on these top gold conductors to compare their resistances, which is an indirect indication of the gold step coverage on both sides of the top ceramic layer.

C. Dielectric and Die Shear Tests

Dielectric tests were performed on the double-layer ceramic packaging substrates before and after thermal tests. A direct current (DC) voltage was applied across the bottom and top gold conductors to measure its leakage current using a Valhalla Scientific Automatic HIPOT tester (model no. 5880A). The DC voltage was applied at a ramp-up rate of 10 V/s up to 600 V with a maximum current limit (current trip-out limit) of .1 mA and a test duration of 10 s at the maximum applied voltage. All possible test combinations of top and bottom conductors were performed. The resistances between the top and bottom gold conductors were measured before and after thermal tests using a BK precision model 880 LCR meter. Die shear tests were performed on the four attached dice before and after thermal tests using a Dage 4000 shear and pull bond tester. Temperature cycling was performed on a ceramic top hot plate with a temperature range from RT to 450°C.

Results and Discussion

A. Dielectric and Resistance Test

The double-layer packaging substrates were subjected to 115 h of thermal aging at 500°C and 30 cycles of temperature cycling from RT to 450°C with a temperature ramp-up/down rate of 267°C/min. An aluminum cooling plate was used to cool down the ceramic substrates after each temperature cycle. A Fluke 52 K/J thermometer was used to monitor instant temperature at both the hot plate and heat sink. Fig. 6 shows the temperature excursion during the temperature cycling test. To facilitate tracking of test results, the top and bottom gold conductors were labeled as shown in Fig. 7.

After thermal aging and temperature cycling, dielectric tests were performed. A 100 V DC voltage was applied on the substrate between "probe #1" at conductor #3 and various routes #1-4 at RT in 37% humidity. Fig. 8 shows the leakage current densities measured at 100 V DC. The leakage current density drops after each thermal test (thermal aging and cycling) except route 1 after thermal aging which could be a random error. The random error can be a combination of human and equipment error, and/or material defects (imperfections and voids in the ceramic interlayer) which affect the dielectric behavior. The leakage current density drop is probably due to the increase in electrical resistance of the ceramic interlayer dielectric. The measured leakage current density at 100 V DC was between 1 nA and 64 nA.

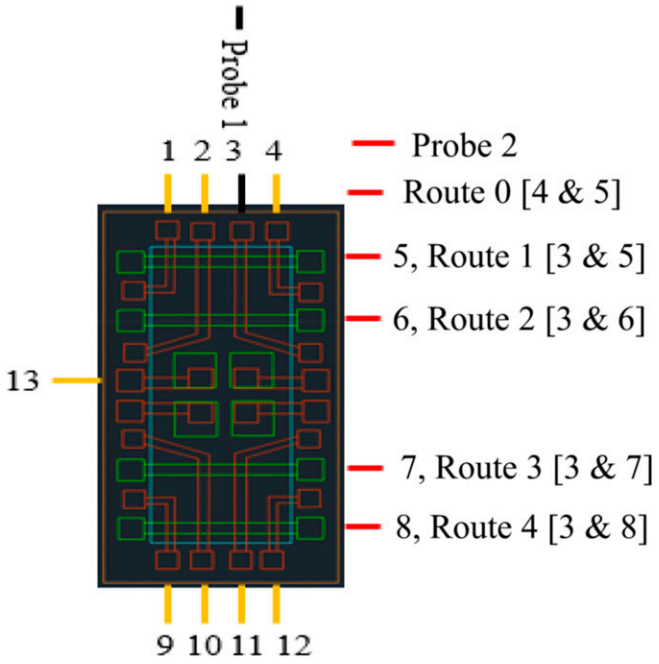

Fig. 7. Conductor and route labeling for double-layered substrate.

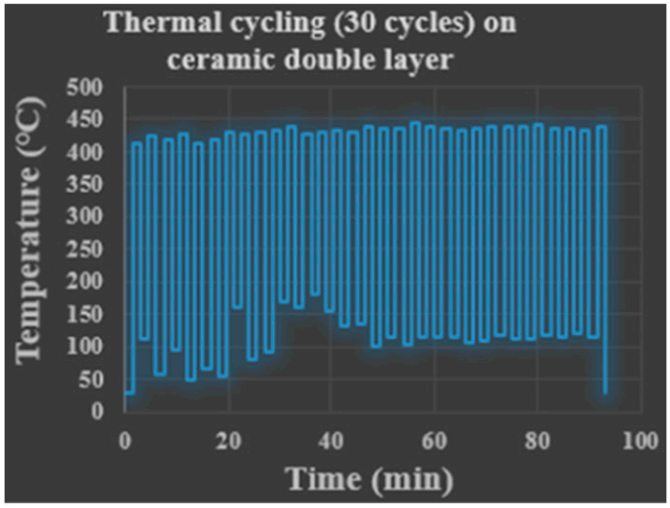

Fig. 6. Thermal profile during temperature cycling.

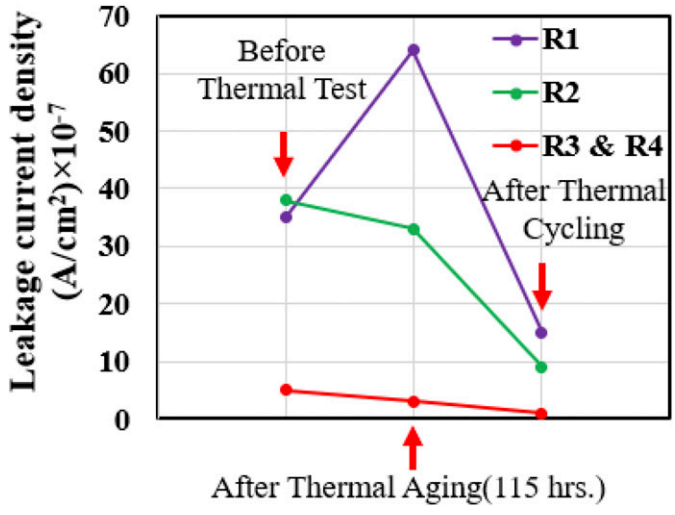

Fig. 8. Leakage current densities on the double-layered substrate by applying 100 V DC.

As is shown in Fig. 7, the distances between the top and bottom conductors on route #1 (the voltage difference is between conductors #3 and #5) and route #2 (the voltage difference is between conductors #3 and #6) are the same height as ceramic interlayer thickness (60 μm), but the distances between the voltage probes on route #3 (the voltage difference applies between conductors #3 and #7) and route #4 (the voltage difference applies between conductors #3 and #8), which is about 2-3 cm, are larger than probe's distance on routes #1 and 2. When the voltage applies between the top and bottom conductors by having a ceramic interlayer, the structure is similar to a parallel plate capacitor with an insulator. Based on the electric field and current charge equations ($E = V/d = qV$ and $I = \mathrm{d}q/\mathrm{d}t$), by increasing the distance between charged plates, the electric field strength reduces which results in a smaller leakage current density value. From a material perspective, in a larger distance between the electrodes, the electric field should travel a longer distance, and ceramic material's dislocation density might be lower which yields a lower leakage current density [11].

Gold conductor resistances were measured before and after temperature cycling. The conductors with the same length are grouped for better consistency. Three groups were created as group # 1 (conductors #1, 4, 9, and 12 with the same length of 8.5 mm), group #2 (conductors #2, 3, 10, and 11 with the same length of 16.3 mm), and group #3 (conductors #5, 6, 7, and 8 with the same length of 17.1 mm). Resistances were measured for each group before and after temperature cycling and average of resistances increased for groups #1, 2, and 3 with a rate of 7.92%, 9.85%, and 10.42%, respectively (the percentages increased by conductor length). The bottom gold traces (groups #1 and 2) had higher initial resistance than the top gold conductors (group #3) that can be because the bottom gold conductors faced more heating and firing process during the fabrication than the top gold conductors. An overall increase in gold conductor resistance after the thermal test (thermal aging and cycling) might be due to the annealing, aging, or structural changes of these conductors [12]. Figs. 9a-c shows resistance changes for groups #1, 2, and 3, respectively.

Interlayer dielectric tests were performed on the double-layer ceramic packaging substrates before and after temperature cycling by applying a direct voltage from 100 V DC to 600 V DC with a 10 V/s rate and a 10-s dwell time. As shown in Fig. 10, the leakage current density increases with increasing applied voltage before and after temperature cycling. At 600 V DC, the initial leakage current density before thermal cycling is 158 × 10^{-7} A/cm^2. The leakage current density calculated for the 1-mm^2 cross section area. However, the leakage current decreases to 50 × 10^{-7} A/cm^2 after temperature cycling. As shown, the

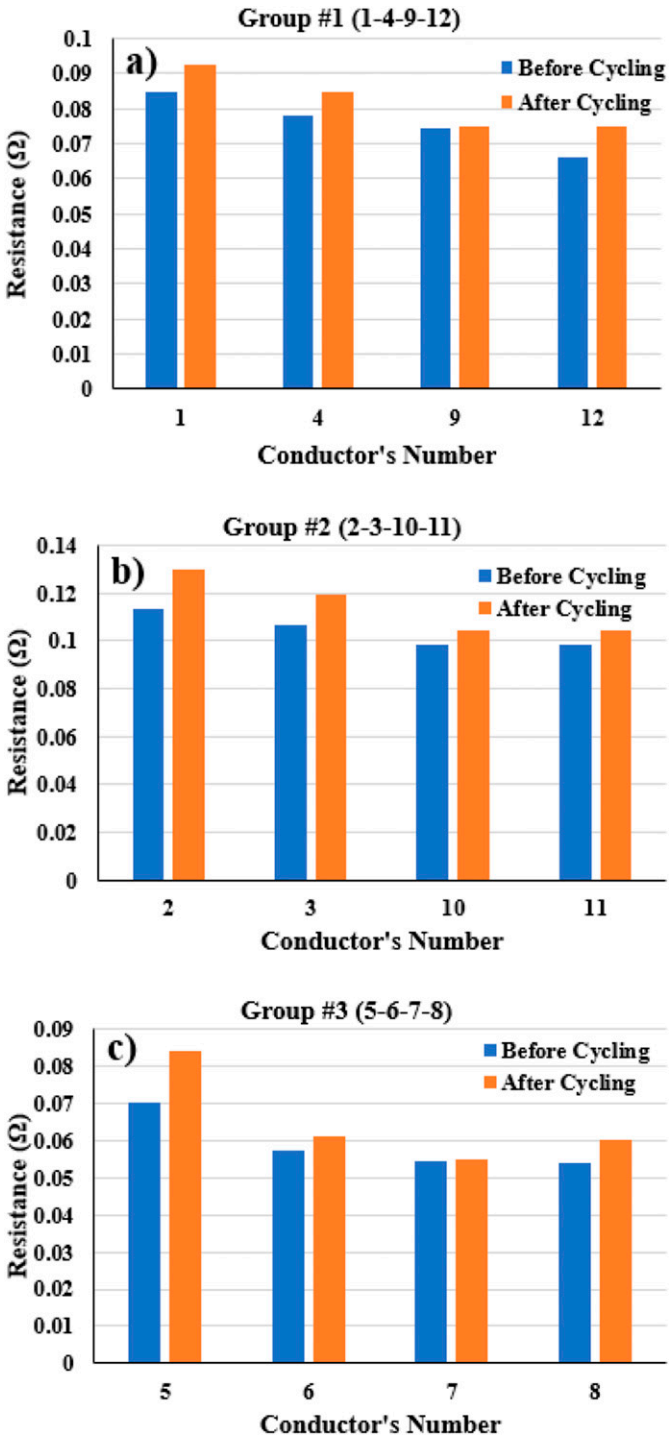

Fig. 9. Resistance plots of the gold conductors before and after the thermal test for (a) group #1 (1-4-9-12), (b) group #2 (2-3-10-11), and (c) group #3 (5-6-7-8).

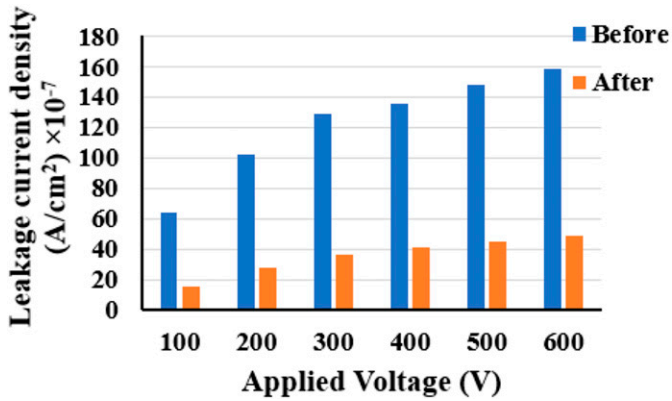

Fig. 10. Dielectric leakage current density versus applied voltage before and after temperature cycling.

leakage current densities decreased by an average of 71.61% after temperature cycling. By thermal annealing the interlayer ceramic at about 450-500°C, the alumina ceramic interlayer starts to transform to polycrystalline structure and becomes denser, and then the dislocation (imperfections) density starts to reduce (less void), which leads to lower leakage current density, higher electrical, and thermal stability [13].

The dielectric test was performed on the ceramic interlayer (distance between probes was 1 cm), and the current reached out the current trip-out limit of .1 mA at 3,921 V DC. The maximum voltages that the substrate could withstand to reach the current trip-out limit of .1 mA was 4,421 V DC and 2,673 V DC (on route # 1) for before and after the thermal test (1,540 h thermal aging at 500°C and 30 thermal cycles from RT to 450°C).

B. Die-Attach Evaluation

Die shear tests were performed to evaluate the integrity and quality of the die-attach before and after thermal tests. The MIL-STD-883 2019.9 die shear strength standard method was adopted. The die shear test was based on the measurement of the force applied perpendicular to the side of the test device to assess various failure modes. Based on the MIL-STD 2019 method, all devices with a surface area of 64×10^{-4} in.^{2} and larger shall withstand a minimum force of 2.5 kg-F. The die shear strength values versus die area can be categorized into three shear strength levels: poor (<2.5 kg-F), medium (between 2.5 kg-F and 5 kg-F), and excellent (>5 kg-F). Based on a die size of 2.6×2.6 mm^2 or 105×10^{-4} in.^{2}, a die shear strength between 2.5 kg-F and 5 kg-F was considered acceptable. The additional 4007 Brazeable conductor gold layer has been shown to increase the die shear strength and reduce the gold delamination from the ceramic substrate. A 36.95% increase in die shear strength was found on those dice with the additional 4007 gold layer compared with those on a single layer of 3066 printed gold layer.

The die shear strengths of the test die-attached on the double-layer ceramic packaging substrates were evaluated after annealing at 500°C for 115 h and after 30 thermal cycles from RT to 450°C. Fig. 11 shows the die shear strength before and after thermal aging at 500°C. As shown, the die shear strength decreases from 9.16 kg-F to 6.16 kg-F, a 32.75% reduction, after the thermal aging. However, the reduced die shear strength is still above the 2× line or 5 kg-F. The decrease in die shear strength after thermal aging could be due to the mismatch in the CTE between the bonded layers. Based on the grain growth law [14], by increasing the annealing time and temperature, growth in grain size of the die-attach may be another reason as a larger grain size allows a larger imperfection movement to reduce its shear strength [15]. The top dice are made of Si, and the CTEs of gold thick film and Si die are 14.4×10^{-6}/°C and 2.6×10^{-6}/°C, respectively [16, 17]. In theory, the induced length difference between Si and gold material when the Si/gold interface's temperature reaches 500°C is about 15.34 μm due to their CTE mismatch, and this causes degradation in shear strength.

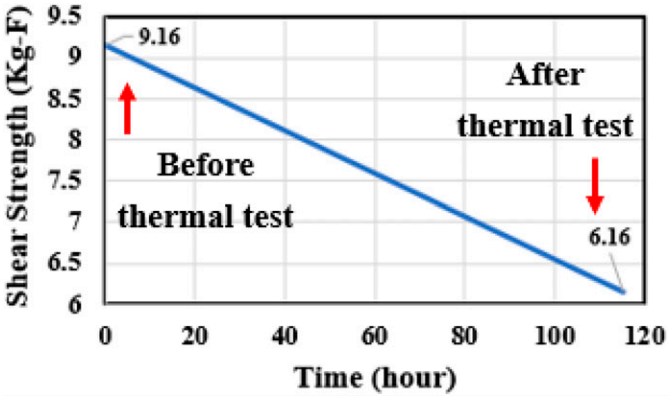

Fig. 11. Die shear strength value before and after thermal reliability test.

C. Morphology and Surface Roughness

The atomic force microscopy (AFM) pictures of the gold surface before (Fig. 12a) and after (Fig. 12b) the thermal test at 500°C are shown in Fig. 12. The surface roughness reduced 19.62% after thermal reliability tests (thermal aging and cycling) which could be due to the thermally induced changes in the gold surface and this results in a larger surface grain size and smaller average roughness amplitude on the gold surface [18].

Conclusions

A double-layer ceramic packaging substrate with gold conductors and a ceramic interlayer dielectric was successfully fabricated using a 96% high-temperature alumina substrate. The packaging substrates were subjected to thermal aging at 500°C for 115 h and 30 temperature cycles between RT and 450°C. Both resistance and dielectric measurements were performed before and after thermal tests. The leakage current densities decreased after thermal tests, whereas the gold conductor resistances increased by 8.2%. A dielectric leakage current density of 158×10^{-7} A/cm^2 at 600 V DC was measured with an average decrease of 71.61% of leakage current density after temperature cycling. The die shear test strengths before and after

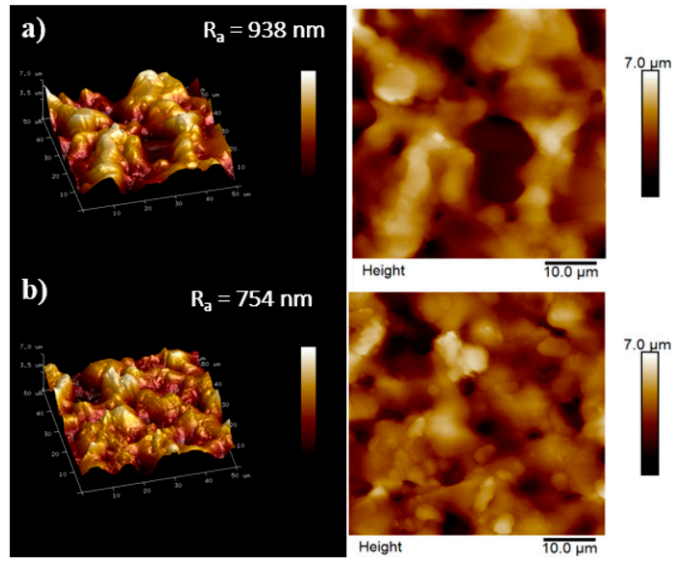

Fig. 12. AFM images of the gold surface (a) before and (b) after the thermal test at 500°C.

thermal aging and temperature cycling were higher than the MIL-standard value of 5 kg-F.

Acknowledgments

This work was funded by the National Aeronautics and Space Administration (NASA) under the HOTTech program Grant # NNX17AG42G and Arkansas NASA EPSCoR Rapid Response Research (R3) Cooperative Agreement # NNH18ZHA005C.

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