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State-of-the-Art and Outlooks of Chiplets Heterogeneous Integration and Hybrid Bonding

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***Abstract*—In this study, the recent advances and trends of chiplet design and heterogeneous integration packaging will be investigated. Emphasis is placed on the definition, kinds, advantages and disadvantages, lateral interconnects, and examples of chiplet design and heterogeneous integration packaging. Also, emphasis is placed on the fundamental and examples of hybrid bonding.**

***Keywords*—Chiplet design, chip partition, chip split, heterogenous integration packaging, hybrid bonding**

Introduction

Chiplet design [1-14] and heterogeneous integration packaging [1-31] have been very popular since DARPA's CHIPS (common heterogeneous integration and IP reuse strategies) program initiated in 2017 [32]. Microprocessors such as AMD's EPYC [1-3] and Intel's Lakefield [4-6], and FPGA (field programable gate array) such as Xilinx's Virtex [14] have been in high volume manufacturing with chiplet designs and heterogeneous integration packaging. One of the horizontal (lateral) communications (interconnects) between chiplets is bridge [17, 33-42]

Hybrid bonding has been getting lots of attention [17, 43-87] since Sony extended their license of "Zibond" to include Ziptronic's DBI (direct bond interconnect) in 2015 and used for manufacturing the complementary metal oxide semiconductor (CMOS) image sensors and other image-based devices in 2016 [45, 46].

In this study, the state-of-the-arts and outlooks of chiplet design and heterogeneous integration packaging as well as hybrid bonding will be presented. Rigid bridges embedded in organic package substrate and epoxy molding compound (EMC) and flexible bridges will also be discussed. System-on-chip (SoC) will be briefly mentioned first.

System-on-Chip (SoC)

SoC integrates ICs with different functions such as central processing unit (CPU), graphic processing unit (GPU), memory, etc. into a single chip for the system or subsystem. The most famous SoC is Apple's AP (application processor), which are simply shown in Fig. 1 for A10 through A14. The number of transistors vs. y with various feature size (process technology) is shown in Fig. 2. It can be seen the power of Moore's law, which increases the number of transistors and functionalities with a reduction of feature size.

Unfortunately, the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC. According to International Business Strategies, Fig. 3 shows the advanced design cost vs. feature size through 5nm. It can be seen that it will take more than $500 million to just design the 5nm feature size. For the 5nm process technology development to high-yield manufacturing it will take another $1 billion. The effect of chip size on semiconductor manufacturing yield is shown in Fig. 4. It can be seen that the larger the chip size the lower the semiconductor manufacturing yield.

Chiplet Design and Heterogeneous Integration Packaging

A. Integration Packaging

Chiplet design and heterogeneous integration packaging contrast with SoC. As pointed out in [23, 31] that heterogeneous integration uses packaging technology to integrate dissimilar chips, photonic devices, or components (either side by side, stacked, or both) with different sizes and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem on a common package substrate. These chips can be any kind of devices and don't have to be chiplets. On the other hand, for chiplets, they have to use the heterogeneous integration to package them [17]. A chiplet is a functional integrated circuit block that is often made of reusable IP (intellectual property) blocks.

There are at least two different chiplet designs and heterogeneous integration packaging as shown in Fig. 5, namely chip partition and integration (driven by cost and technology optimization) and chip split and integration (driven by cost and yield). In chip partition and integration, the SoC such as the logic and I/Os are partitioned into functions: logic and I/O (chiplets). These chiplets can be stacked (integrated) by the frontend CoW (chip-on-wafer) or WoW (wafer-on-wafer) methods [17] and then assembled (integrated) on the same substrate of a package by using heterogeneous integration techniques (Fig. 6). It should be emphasized that the frontend chiplets integration can yield a smaller package area and better electrical performance but is optional. In chip split and integration, the SoC such as logic is split into smaller chiplets such as logic1, logic2, and logic3. These chiplets can be stacked (integrated) by the frontend CoW or WoW methods and then

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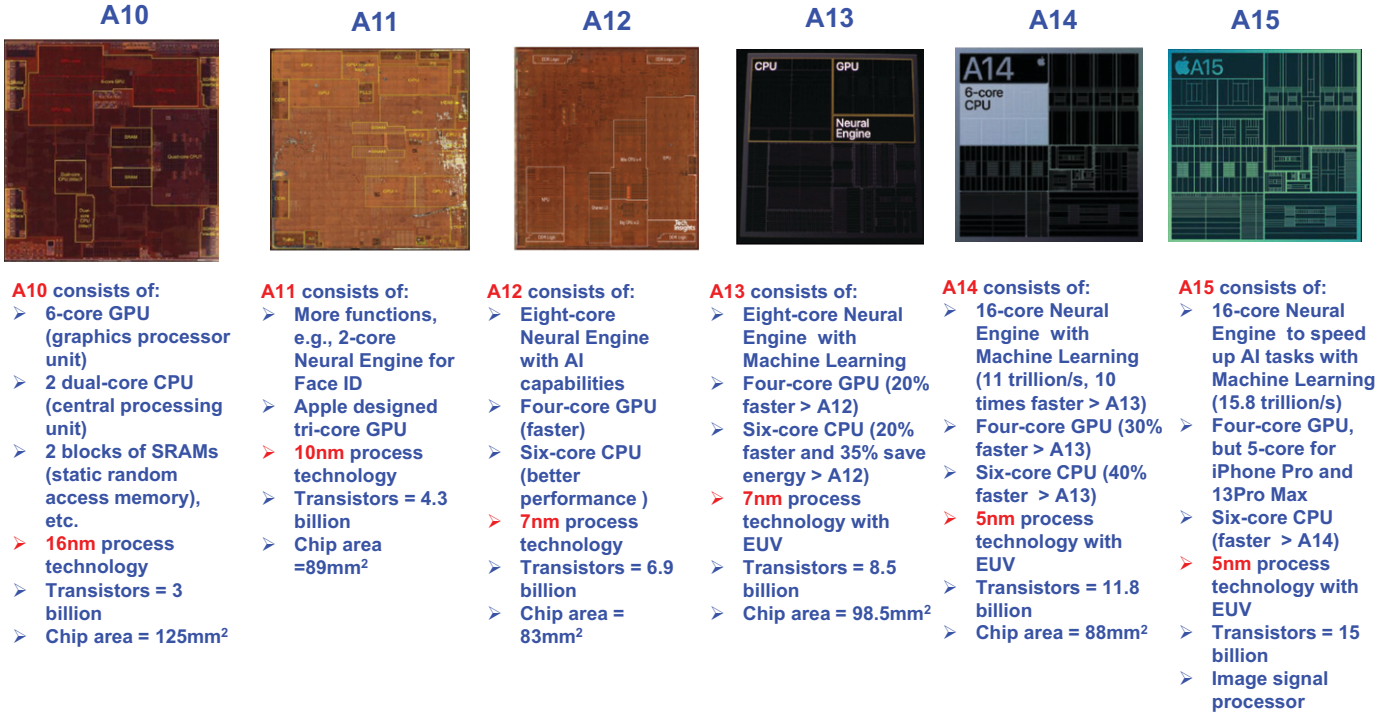

Fig. 1. Apple's SoC (application processor).

assembled (integrated) on the same substrate of a package by using heterogeneous integration (Fig. 6). Again, the frontend integration of chiplets is optional.

Advantages and Disadvantages of Chiplet Design and Heterogeneous Integration Packaging

The key advantages of chiplet design and heterogeneous integration packaging, comparing with SoCs, are yield improvement during manufacturing. For chip partitioning and/or splitting, the size of the chiplet is smaller than the SoC and thus it leads to higher semiconductor manufacturing yield, which translates to lower manufacturing cost. Fig. 5 shows the plots of yield (percent of good dice) per wafer vs. chip size for monolithic design and 2-, 3-, and 4-chiplet designs [88]. It can be seen that a 360mm^2 monolithic die will have a yield of 15% while a 4-chiplet design (each 99mm^2) more than doubles the yield to 37%. The total die area of the 4-chiplet design incurs a ~10% area penalty (36mm^2 for a combined silicon area of 396mm^2) but the significant improvement in yield which directly translates to lower cost. Also, chip partitioning will enhance the time-to-market. Furthermore, the use of chiplets with CPU cores can reduce silicon design and manufacturing costs. Finally, there is also thermal benefit to using chiplets as the chips are spread out across the package. The disadvantages of chiplet design and heterogeneous integration packaging are: (1) additional area for interfaces, (2) higher packaging costs, (3) more complexity and design effort on packaging, and (4) past methodologies are less suitable for chiplets.

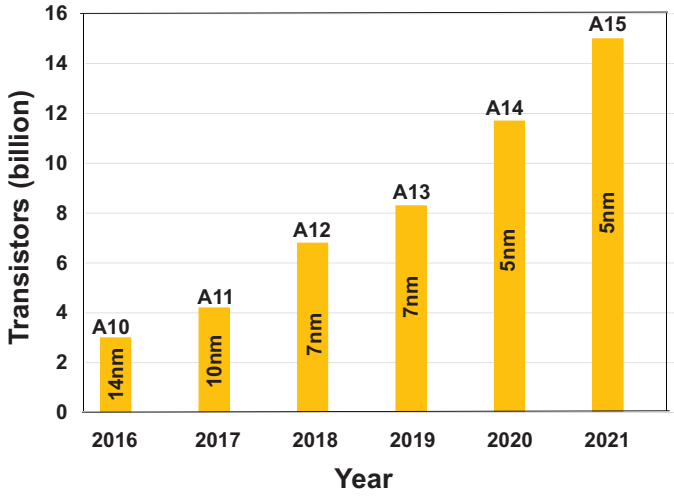

Fig. 2. APs: Transistors vs. y in terms of feature size.

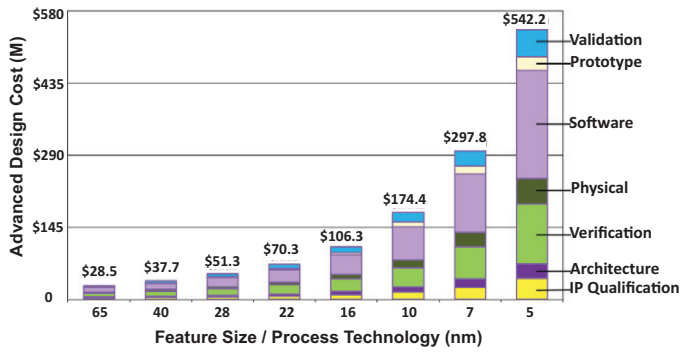

Fig. 3. Advanced design cost of semiconductor chip.

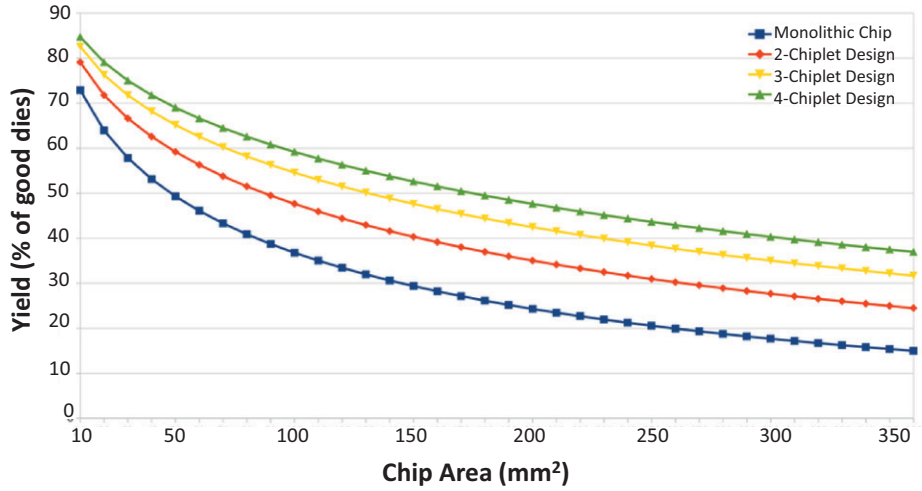

Fig. 4. Yields vs. chip area for various chiplet designs.

Xilinx's Chiplet Design and Heterogeneous Integration Packaging

In 2011 Xilinx asked TSMC to fabricate their FPGA SoC with the 28nm process technology. Because of the large chip size the yield was very poor. Then, Xilinx redesigned and split the large FPGA into four smaller chiplets as shown in Fig. 7 and TSMC manufactured the chiplets at high yield and packaged them on their CoWoS. On October 20, 2013 Xilinx and TSMC [14] have jointly announced production release of the Virtex-7 HT family with 28nm process technology, what the pair claims is the industry's first chiplet design and heterogeneous integration package in production.

AMD's Chiplet Design and Heterogeneous Integration Packaging

In mid2019, AMD shipped the 2nd-generation EPYC (extreme performance yield computing) server processors, 7002-series, codename Rome which doubled the number of cores to sixty-four. In [1, 2], it shows that Rome server product makes use of a 9-2-9 package substrate for signal connectivity with 4 layers above the package core for signal routing, Fig. 8a.

For high-performance servers and desktop processors the I/Os are very heavy. Analog devices and bump pitches for I/Os benefit very little from leading edge technology and is very costly. One of the solutions is to partition the SoC into chiplets, reserving the expensive leading-edge silicon for CPU core while leaving the I/Os and memory interfaces in n-1 generation silicon [1, 2]. Another solution is to split the CPU core into smaller chiplets. In this case, each CCD (core complex die or CPU compute die) is split into two smaller chiplets. AMD used the expensive 7nm process technology fabricated by TSMC (in early 2019) for the core CCD chiplets and moved the DRAM and logic to a mature 14nm I/O die fabricated by GlobalFoundries. The 2nd-generation EPYC is a 2D chiplets IC integration technology, i.e., all the chiplets are side-by-side on the 9-2-9 build-up package substrate.

AMD's future chiplet design and heterogeneous integration packaging [3, 10, 11] will be 3-D chiplets integration, i.e., the chiplets are (stacked) on top of the other chiplet such as logic, so called the active TSV (through-silicon via)-interposer as

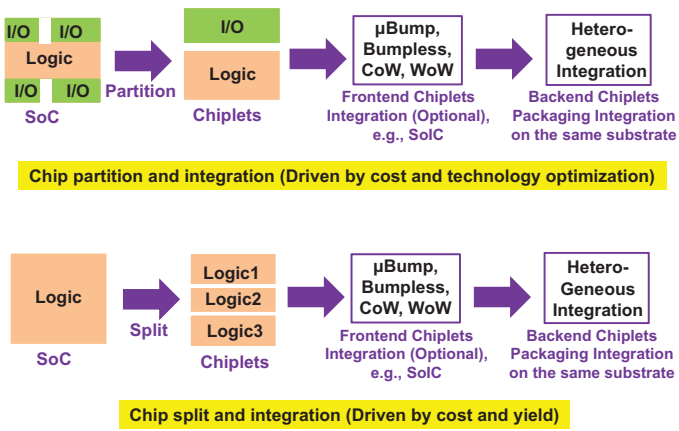

Fig. 5. Chiplet designs and heterogeneous integration packaging.

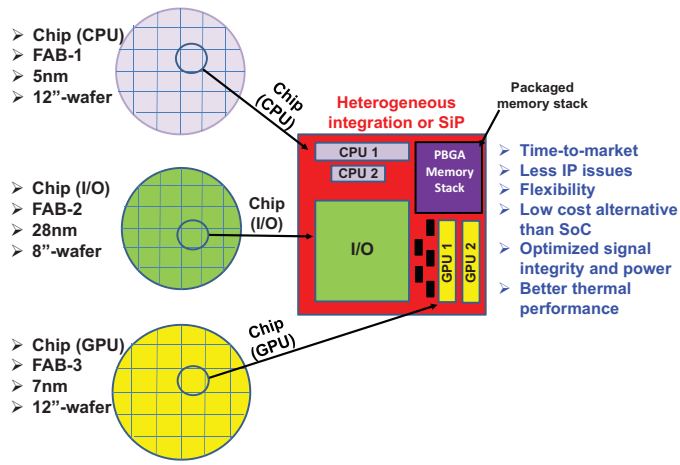

Fig. 6. Heterogeneous integration (packaging) for chiplets, discrete, and etc.

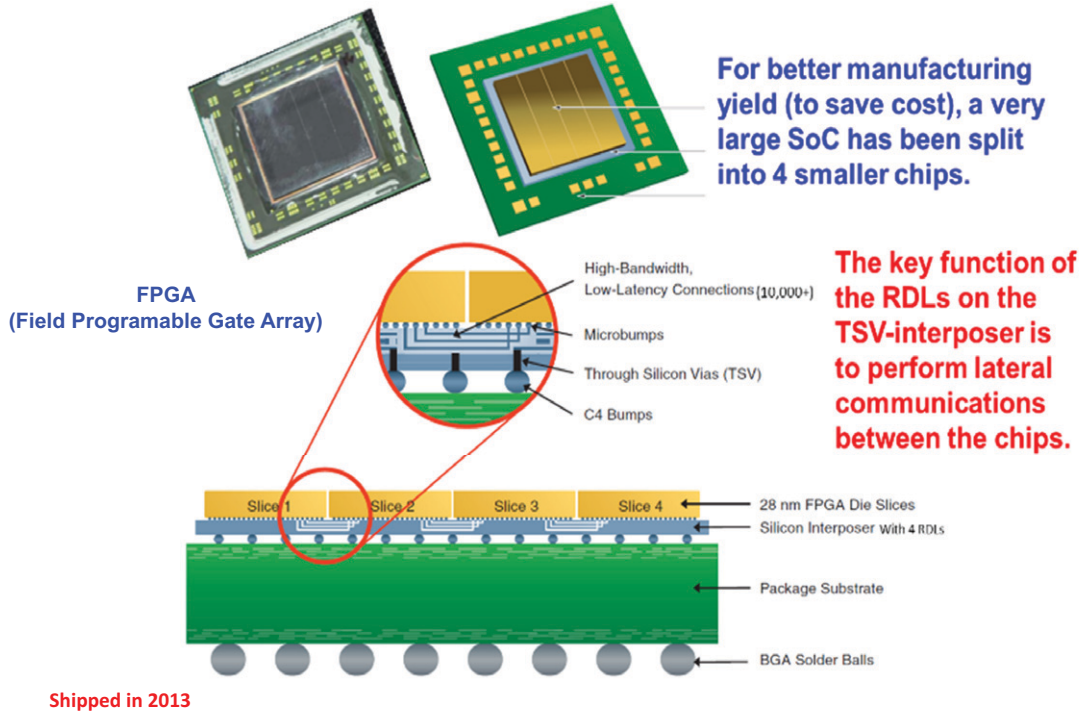

Fig. 7. Xilinx's chiplet design and heterogeneous integration packaging.

shown in Fig. 9. It is a special Ryzen 9 5900X prototype chip leveraging a 3-D V-Cache stack, which enables triple the amount of cache that its cores normally have access to (32MB vs. 96MB of L3 cache). The first Ryzen chips with 3-D chiplet design and heterogeneous integration packaging is scheduled for release by early 2022, which will offer 15 precent faster gaming on average at minimum.

Intel's Chiplet Design and Heterogeneous Integration Packaging

In July 2020, Intel shipped their mobile (notebook) processor "Lakefield", which is based on their FOVEROS technology. The SoC is partitioned (e.g., CPU, GPU, LPDDR4, etc.) and split (e.g., the CPU is split into one big CPU and 4 smaller

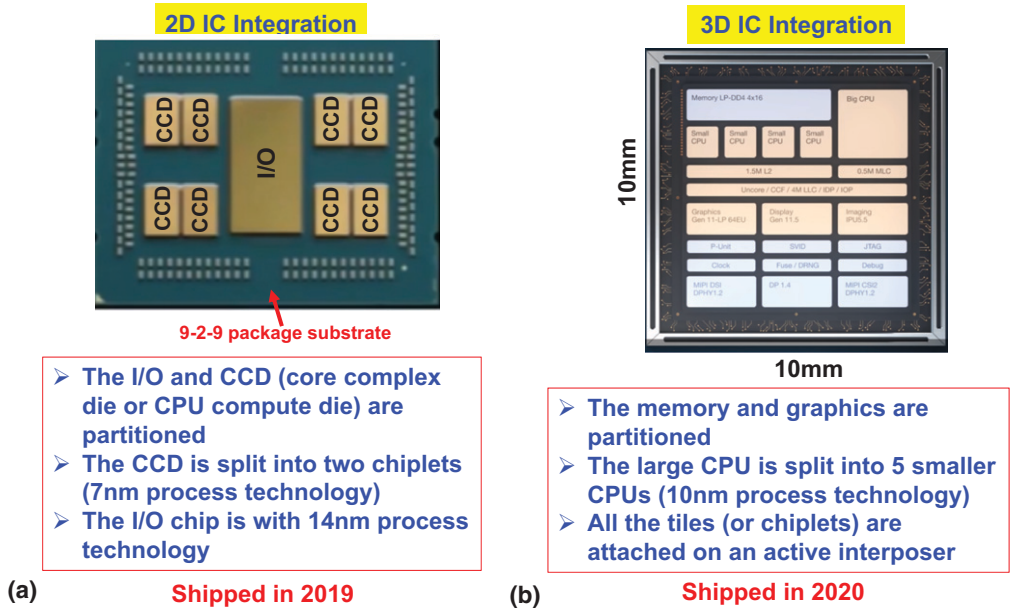

Fig. 8. Chiplet designs and heterogeneous integration packaging. (a) AMD's EPYC. (b) Intel's Lakefield.

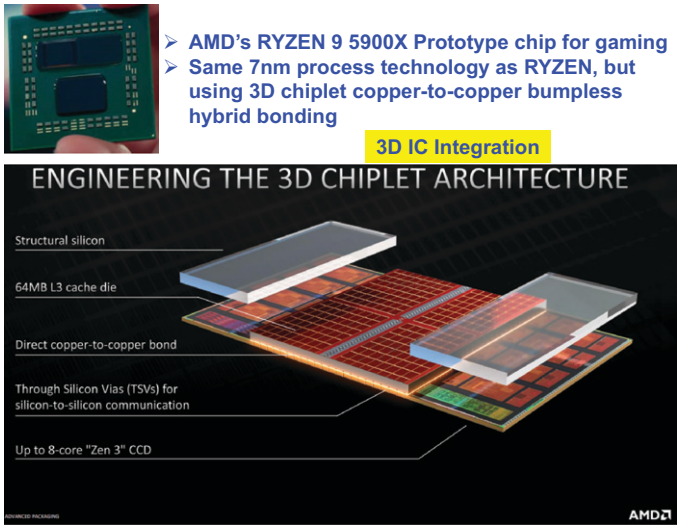

Fig. 9. AMD's future 3-D chiplets design and heterogeneous integration packaging.

CPU) into chiplets as shown in Figs. 8b, 10, and 11. These chiplets are then face-to-face bonded (stacked) on an active TSV-interposer (a 22nm FFL base chip) with a CoW process. The interconnect between the chiplets and the logic base chip is micro bump (Cu pillar + SnAg solder cap) as shown in Figs. 10 and 11. The interconnect between the base chip and the package substrate (only 4 layers coreless) is C4 bump and between the package substrate and PCB is solder ball. The final package formant is a 12 × 12 × 1mm package-on-package (PoP) as shown in Fig. 10. The chiplet design and heterogeneous integration packaging are in the bottom package and the upper package is housing the memories with wire bonding technology.

The fabrication of the chiplets is with Intel's 10nm process technology and of the base chip is 22nm. Since chiplets' size is smaller and not all the chips are using the 10nm process technology, the overall yield must be higher and thus it translates to lower cost.

It should be noted that this is the very first high-volume manufacturing (HVM) of 3-D chiplets integration. Also, this is the very first HVM of processors for mobile products such as the notebook by 3-D IC integration.

One of Intel future chiplet designs and heterogeneous integration packaging is called FOVEROS Direct [12]. Basically, it is a Cu-Cu bumpless hybrid bonding technology announced during Intel Architecture Day (August 13, 2020), Fig. 12. It can be seen that since the bumpless pad pitch reduces from 50µm (for microbumps) to 10µm, the density increases from 400 bumps/mm^2 to 10,000 pads/mm^2.

Another Intel future chiplet designs and heterogeneous integration packaging is called Ponte Vecchio GPU, or the "Spaceship of a GPU" [12, 13], which is planned to be the largest and most chip designed to date. The Ponte Vecchio GPU will be making use of several key technologies which will power 47 different compute chiplets based on different process nodes and architectures as shown in Fig. 13. While the GPU

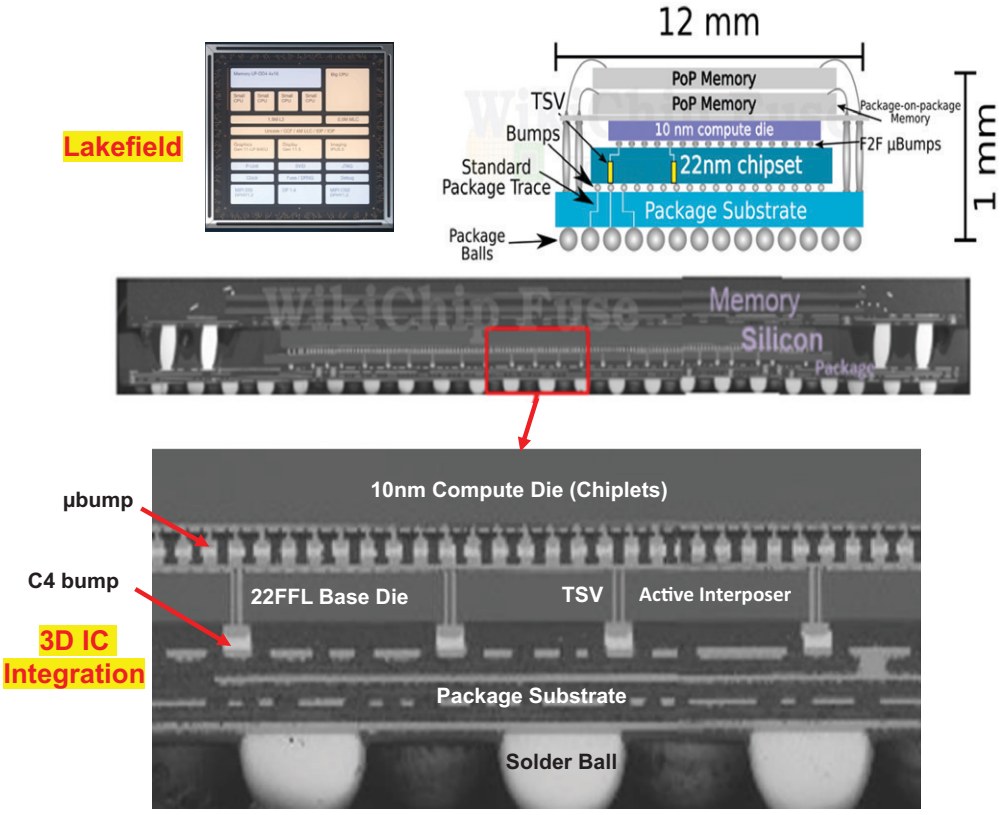

Fig. 10. 3-D IC integration: Intel's chiplet design and heterogeneous integration packaging.

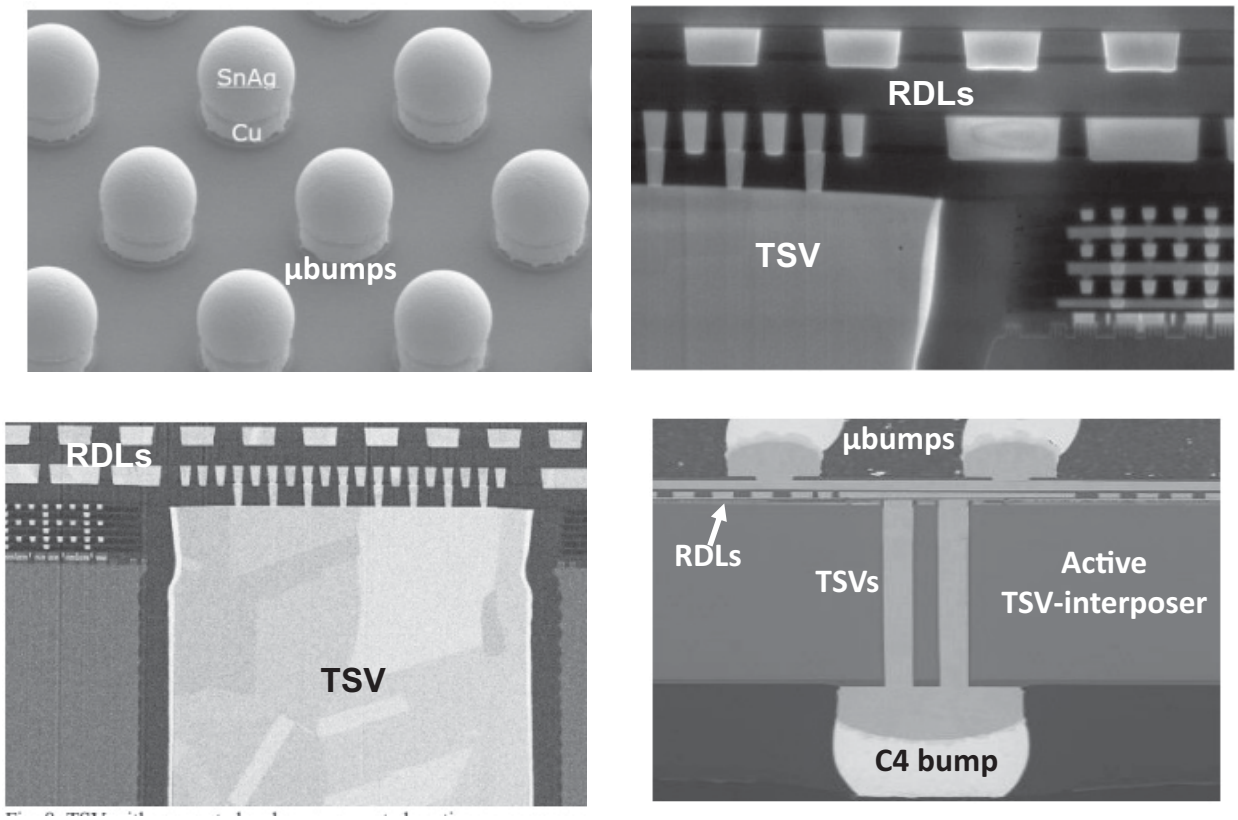

Fig. 11. Intel's 3-D IC integration: chiplets, microbumps, RDLs, and active TSV-interposer.

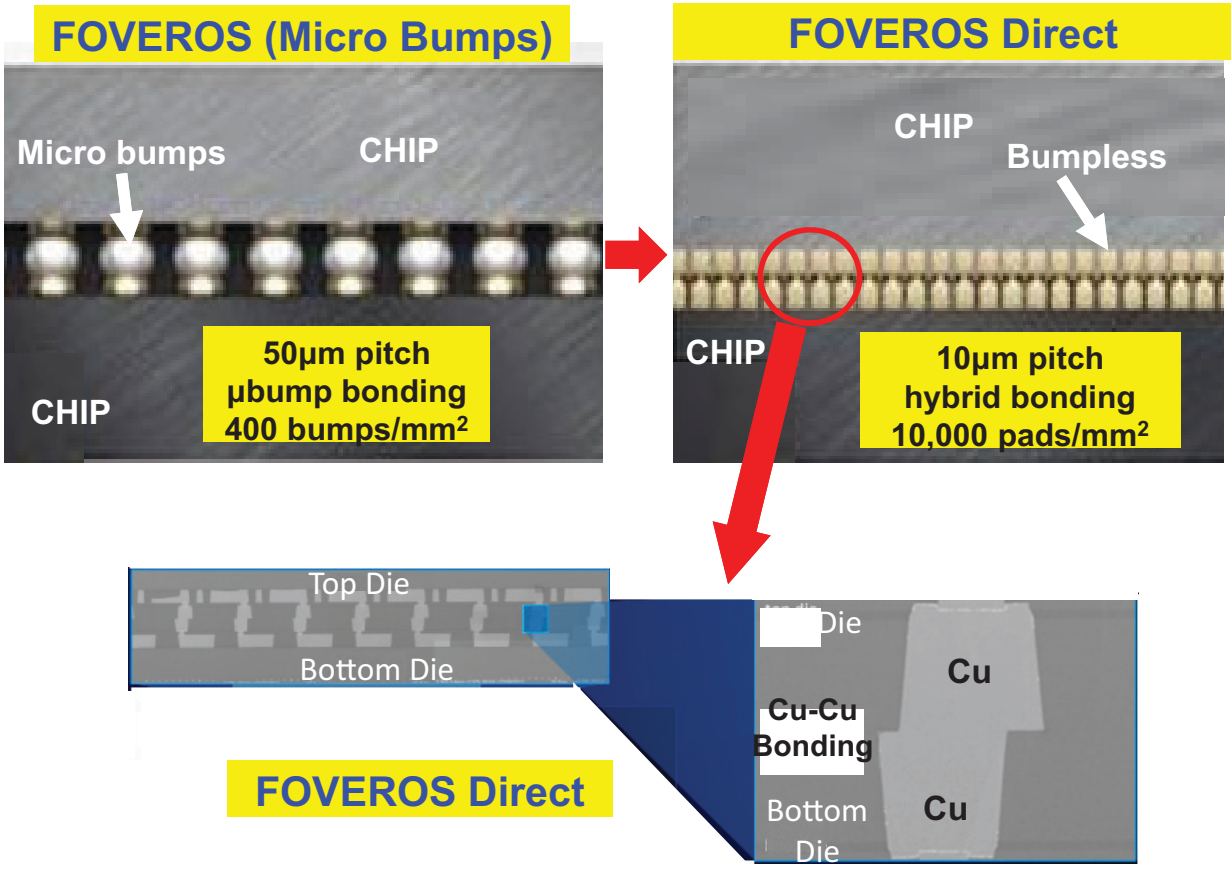

Fig. 12. Intel's FOVEROS Direct.

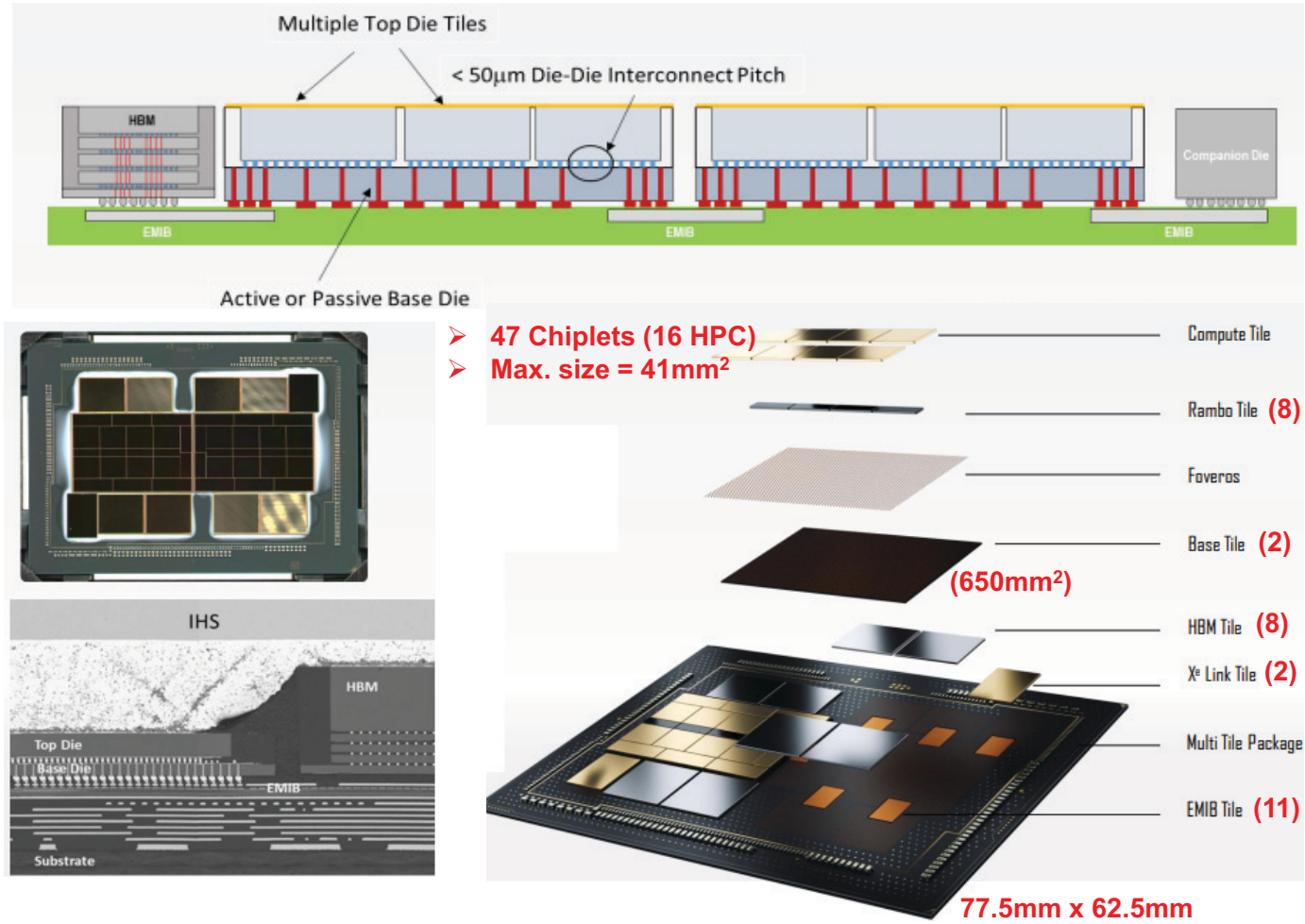

Fig. 13. Intel's Ponte Vecchio GPU.

primarily makes use of Intel's 7nm EUV (extreme UV lithography) process node but Intel will also be producing some Xe-HPC compute dice through external fabs (such as TSMC's 5nm process technology). To be precise, the 47 chiplets consist of: 16 Xe-HPC (internal/externa); 8 Rambo (internal); 2 Xe-Base (internal); 11 EMIB (internal); 2 Xe-Link (external); and 8 HBM (external). The maximum top-die (chiplet) size = 41mm^2; the base-die size = 650mm^2; die-to-die pitch = 36µm; and package size = 77.5mm × 62.5mm.

TSMC's Chiplet Design and Heterogeneous Integration Packaging

During TSMC Annual Technology Symposium (August 25, 2020) TSMC announced their 3DFabric (3-D fabrication) technology for mobile, high-performance computing (HPC), automotive, and IoT (internet of things) applications, e.g [7-9]. 3Dfabric provides chiplet design and heterogeneous integration packaging that are fully integrated from front to back. The application-specific platform leverages TSMC's advanced frontend wafer technology such as SoIC (system on integrated chips), open innovation platform design ecosystem, and 3DFabric for fast improvements and time-to-market. Fig. 14a shows the frontend TSMC's SoIC [7-9] along with the conventional 3-D IC integration with flip chip technology. It can be seen that the key difference between SoIC and the ordinary 3-D IC integration is that SoIC is bumpless and the interconnects between the chiplets is Cu-to-Cu hybrid bonding. The assembly process of SoIC can be either WoW or CoW hybrid bonding.

The SoIC technology has a better electrical performance than the flip chip technology as shown in Fig. 14b. (The SoIC chiplets are vertically hybrid bonded and the flip chips are 2D side-by-side assembled.) It can be seen that the insertion loss of SoIC technology is almost zero and is far smaller than that of the flip chip technology. Fig. 14c shows the bump density from various bonding assembly technologies such as flip chip, 2.5D/3-D, SoIC, and SoIC+. It can be seen that SoIC can go down to ultra-fine pitch with extremely high density. Another advantage of SoIC is free of the chip-package-interaction reliability issue from fine-pitch flip chip assembly.

In 3-D backend heterogeneous integration (Fig. 15), the CoWoS (chip-on-wafer-on-substrate) increased envelope and

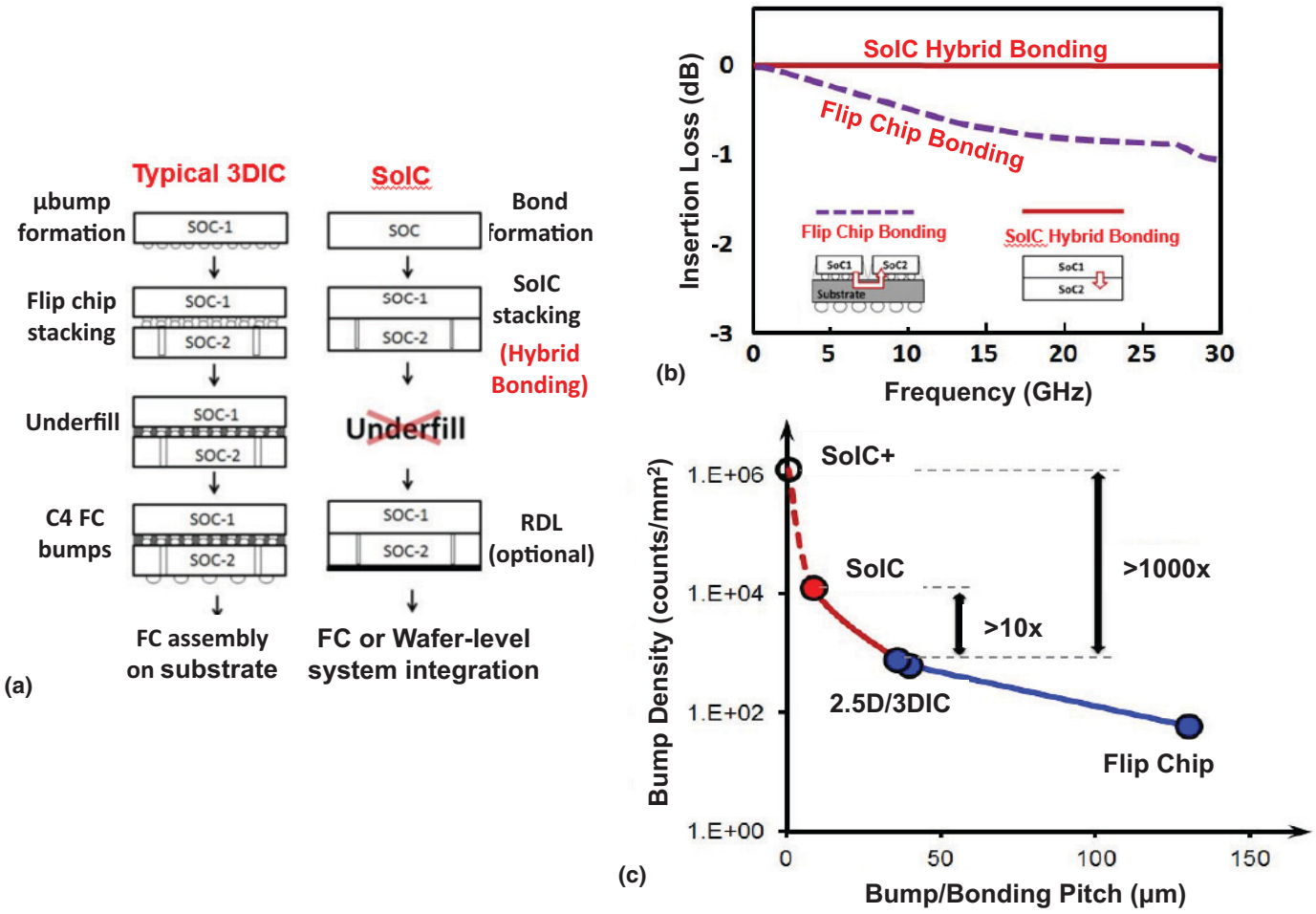

Fig. 14. TSMC (a) Chiplets. (b) Performance. (c) Density.

enriched technology content offers exceptionally high computing performance and high memory bandwidth to meet HPC needs on clouds, data center, and high-end server.

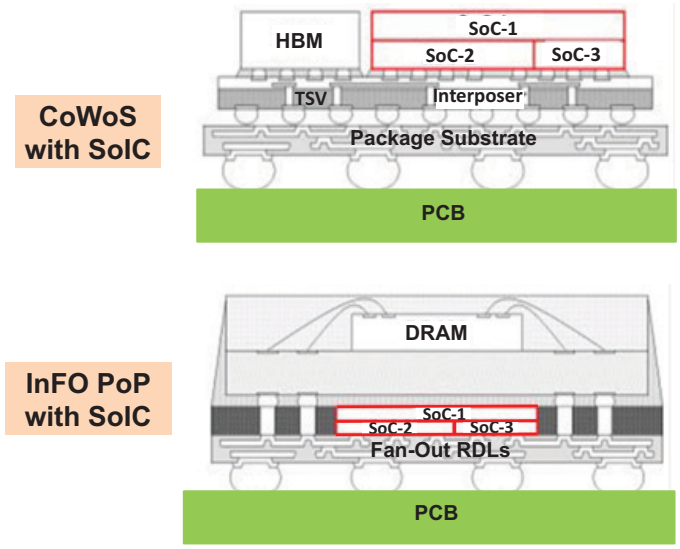

Fig. 15. TSMC's chiplets packaging.

In another 3-D backend heterogeneous integration, InFO (integrated fan-out) derivative technology offers memory-to-logic, logic-to-logic, PoP, etc. applications. The HVM of SoIC, SoIC+CoWoS, and SoIC+InFO is expected in 2022.

Chiplets Lateral Interconnects

One of the horizontal communications between chiplets in a chiplet design and heterogeneous integration package is through bridges [17] such as Intel's EMIB (embedded multidie interconnect bridge). Fig. 16 shows one of Intel's patents and the Agilex FPGA (field programmable gate array) module. The FPGA and other chips are attached on top of a build-up package substrate with EMIB [34, 35] with fine metal line width and spacing (L/S) RDLs (redistribution-layers). The C4 (controlled collapse chip connection) bumps and C2 (chip connection or micro) bumps are on the chiplets. One of the challenges of the EMIB technology is to fabricate the organic build-up package substrate with cavities for the silicon bridges and then laminate (with pressure and temperature) another build-up layer on top (to meet the substrate surface flatness requirement) for chiplets (with both C2 and C4 bumps) bonding.

Very recently, IBM proposed a method called DBHi (direct bonded heterogeneous integration) [36]. They make a cavity

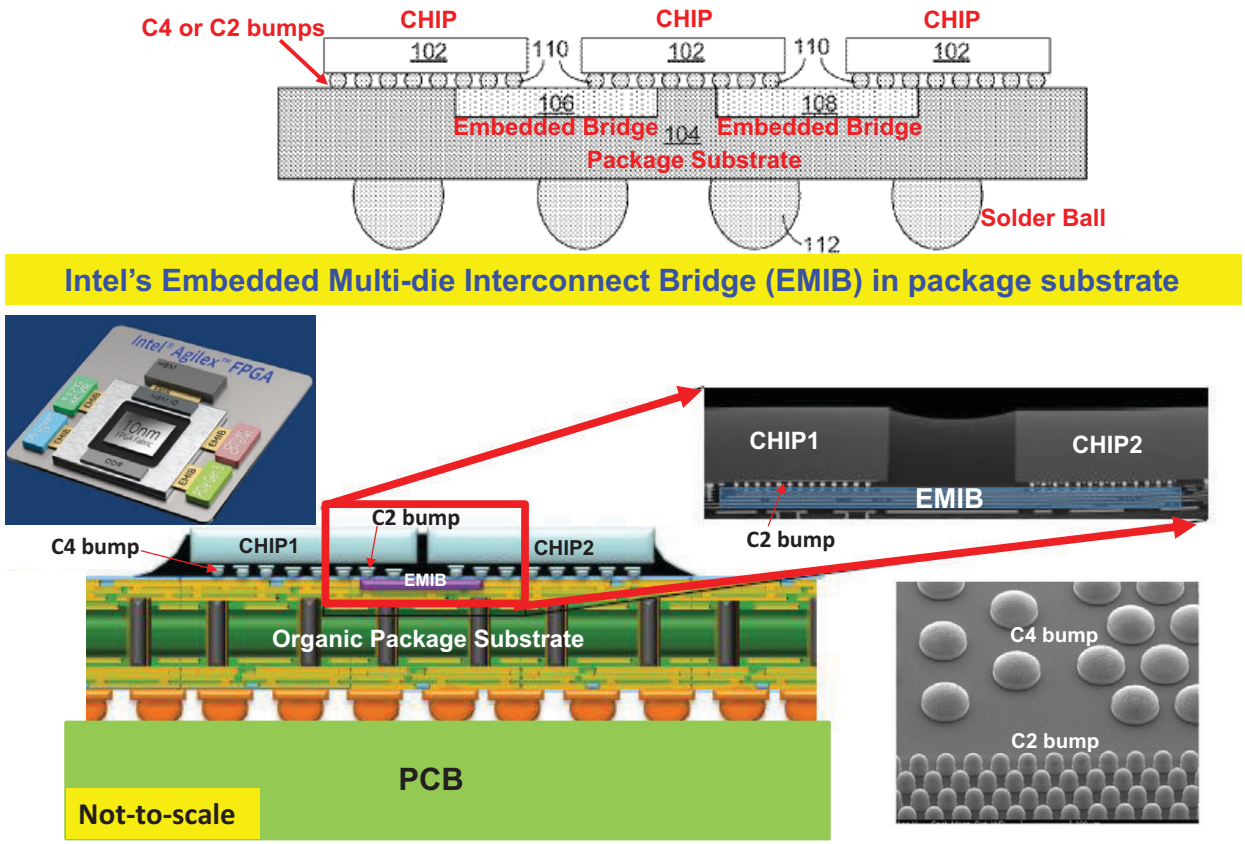

Fig. 16. Intel's EMIB patent and Agilex FPGA module.

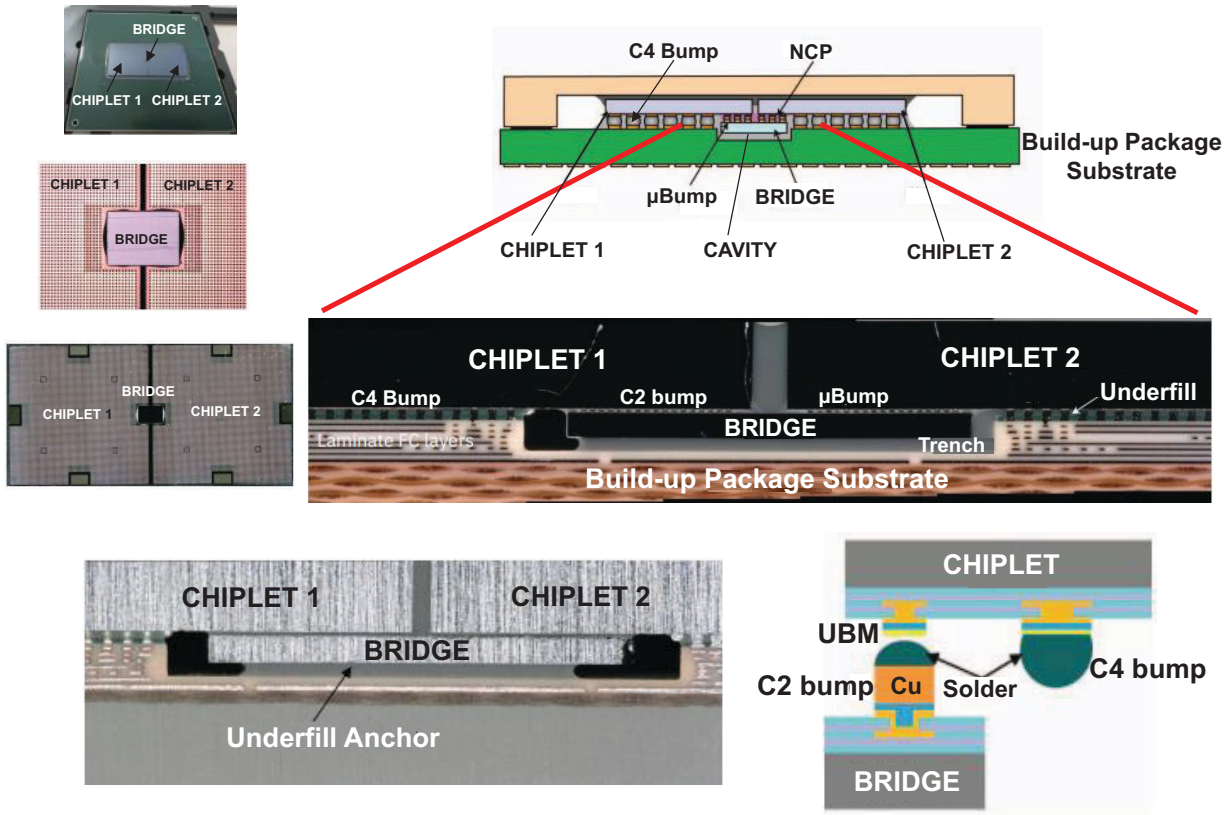

Fig. 17. IBM's direct bonded heterogeneous integration.

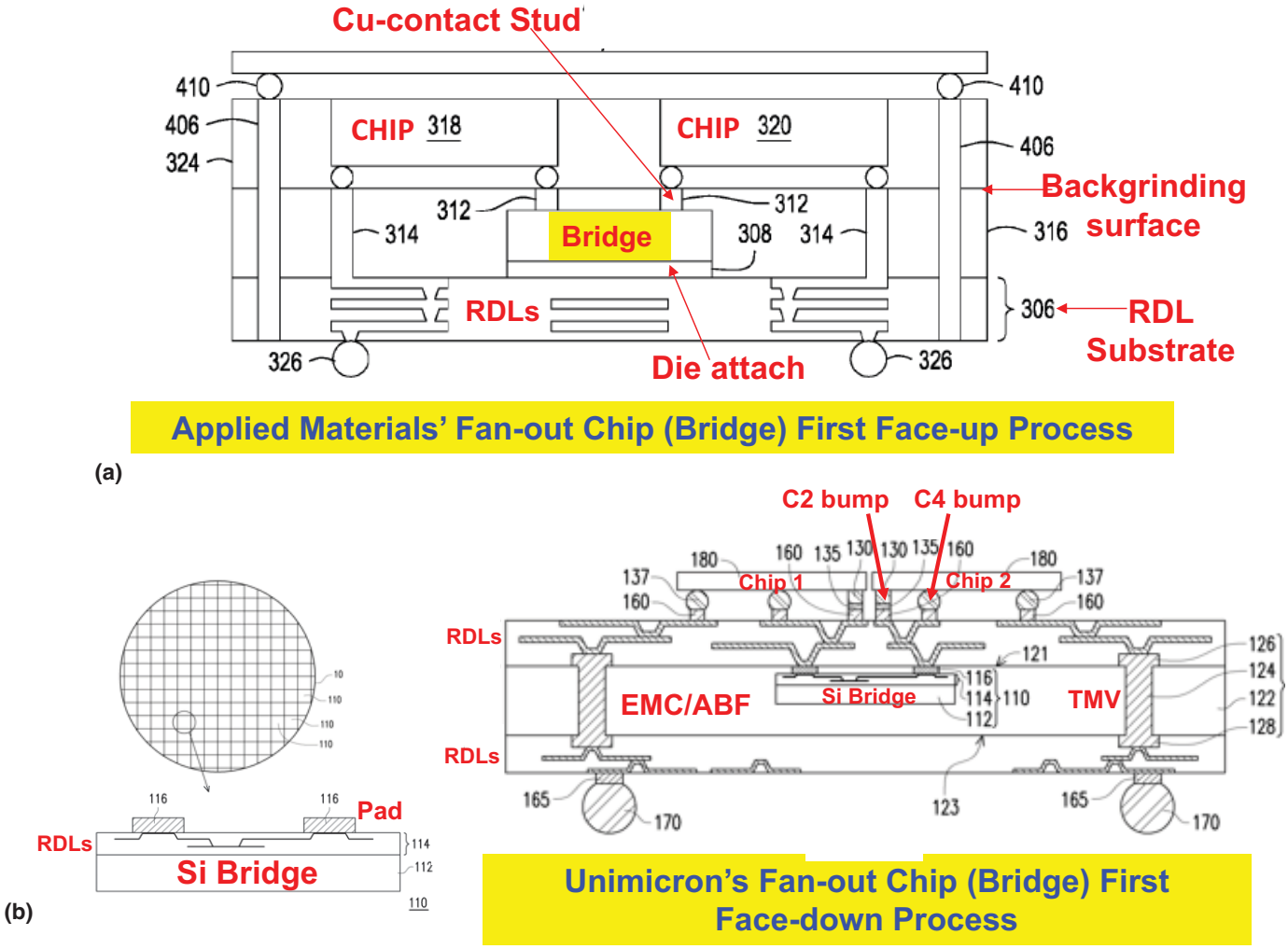

Fig. 18. Bridges embedded in EMC. (a) Fan-out chip (bridge)-first face-up process. (b) Fan-out chip (bridge)-first face-down process.

on an ordinary package substrate (Fig. 17). In parallel, they do the wafer bumping and bonding of the chiplets and bridges and then assembly the whole module in the cavity by reflowing the C4 solder bump on the package substrate as shown in Fig. 17. The key step in IBM's method is to do C4 bumping on the chiplet and C2 (Cu-pillar + solder cap or micro) bumps on the bridge. In this case there are two different UBMs (under bump metallurgies) on the chiplet wafer, which are fabricated by a double lithography process [36]. The key challenges of DBHi are when there are more than one bridge on a chiplet and there are more than two chiplets on a package substrate such as the Ponte Vecchio GPU module.

The fine metal L/S RDL bridges can also be embedded in EMC (epoxy molding compound) of fan-out packaging. Fig. 18a shows the Applied Materials' patent [37] with fan-out chip (bridge) first face-up process, while Fig. 18b shows the patent application of Unimicron with fan-out chip (bridge) first face-down process. Recently, there are many publications in these areas such as those given by TSMC's LSI (local silicon interconnect) [38], SPIL's FO-EB (fan-out-embedded bridge) [39], Amkor's S-Connect fan-out interposer [40], ASE's sFO-CoS (stacked Si bridge fan-out chip-on-substrate) [41], and IME's EFI (embedded fine interconnect) [42] as shown in Fig. 19a–efig19, respectively.

All the foregoing bridges are called rigid bridge in which all the RDLs are fabricated on a silicon wafer substrate. There is the flexible bridge [33], which is the RDL itself. The flexible bridge consists of the fine metal L/S conductors in a dielectric polymer such as polyimide film. The very first flexible bridge patent US 2006/0095639 A1 was filed by SUN Microsystems on November 2, 2004, Figure 20. The bonding assembly process is very similar to IBM's DBHi. However, the C4 bumps and C2 bumps should be on the chiplets like Intel's EMIB. The key challenge is the handling of the flexible bridge during bonding, especially there are more than one bridge on a chiplet and there are more than one chiplet with multiple flexible bridges. For high-speed and high-frequency applications such as millimeter wave frequencies, the dielectric layer (polyimide) can be replaced by the LCP (liquid crystal polymer) so called the LCP-flexible bridge.

Hybrid Bonding

Hybrid bonding (that combines a dielectric bond with a metal bond to form an interconnection) is known

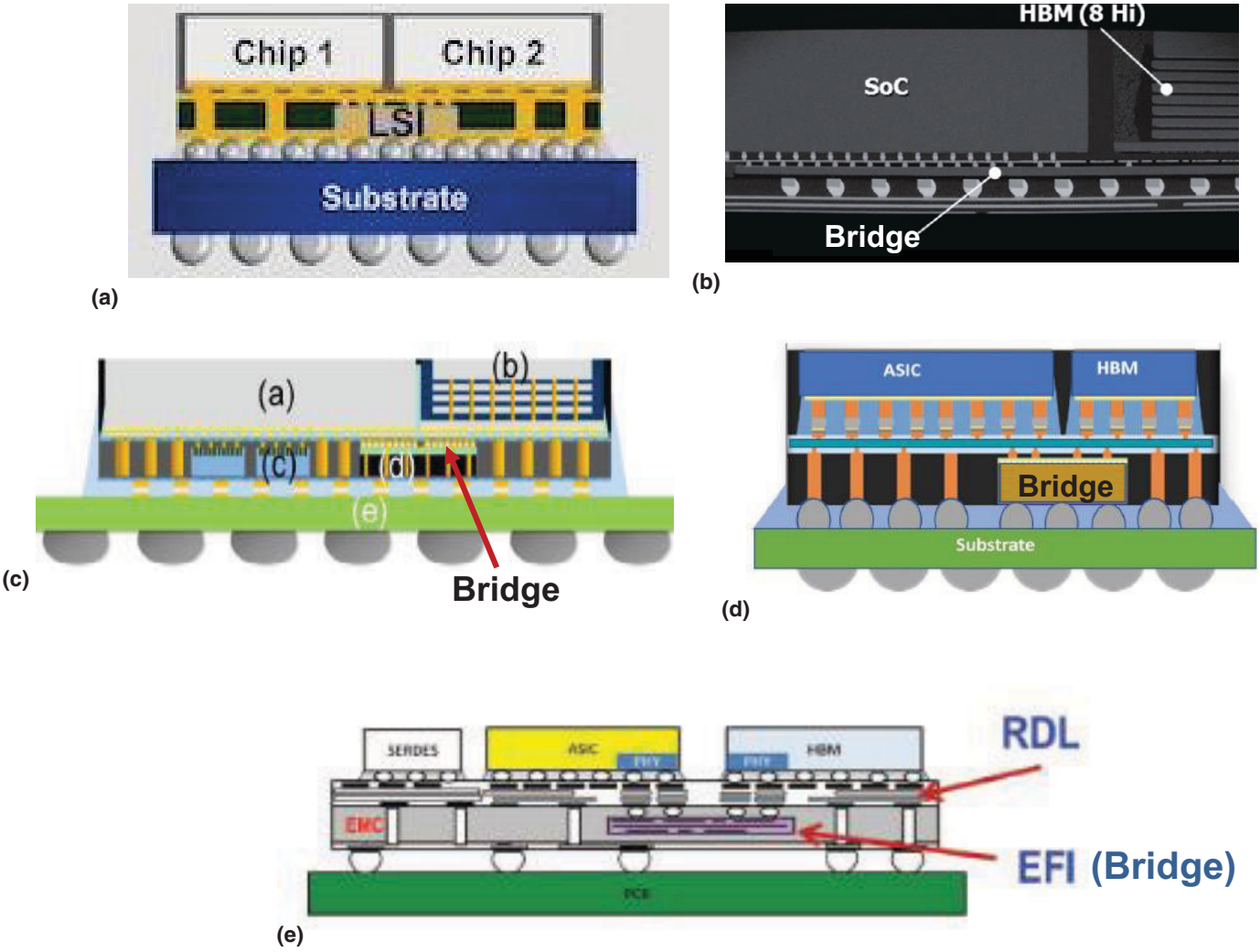

Fig. 19. Bridges embedded in EMC. (a) TSMC's LSI. (b) SPIL's FO-EB. (c) Amkor's S-Connect. (d) ASE's sFOCoS. (e) IME's EFI.

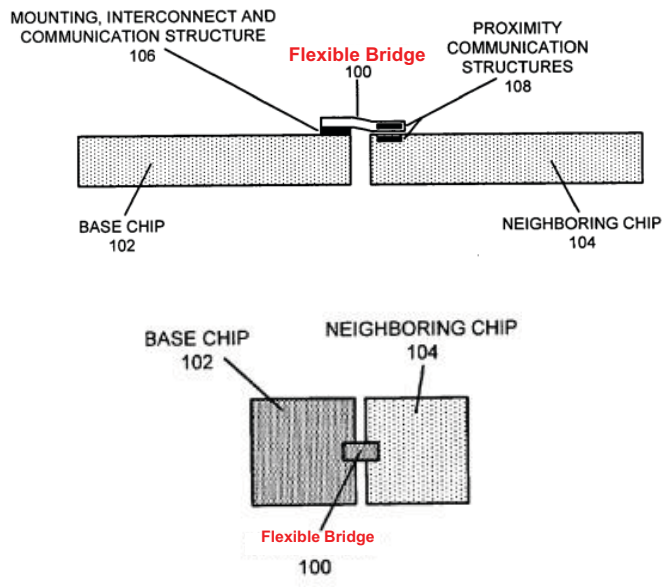

Fig. 20. SUN Microsystems patent application: flexible bridge

industry-wide as low-temperature DBI (direct bond interconnect), which operates at room temperature and then anneal at 150-300°C. DBI was invented by Research Triangle Institute (RTI) and patented it as ZiBond (a direct oxide to oxide bonding that involves wafer-to-wafer processing at low temperatures to initiate high bond strengths). Between 2000 and 2001, Fountain, Enguist, Tong, and several other colleagues founded Ziptronic as a spin-out of RTI. Between 2004 and 2005, based on their ZiBond technology, Ziptronic combined the dielectric bond with embedded metal to simultaneously bond wafers and form the interconnects at low temperature (so called DBI) [43, 44]. Ziptronic was acquired by Tessera on August 28, 2015. Tessera has changed its name to Xperi on February 23, 2017.

The breakthrough for Ziptronic DBI technology came in the spring of 2015 when Sony, already using its "Zibond" oxide to oxide bonding technology extended its license to include DBI. DBI is now being used for much of the complementary metal-oxide-semiconductor (CMOS) image sensor (CIS) market in the world's smartphones and other image-based devices.

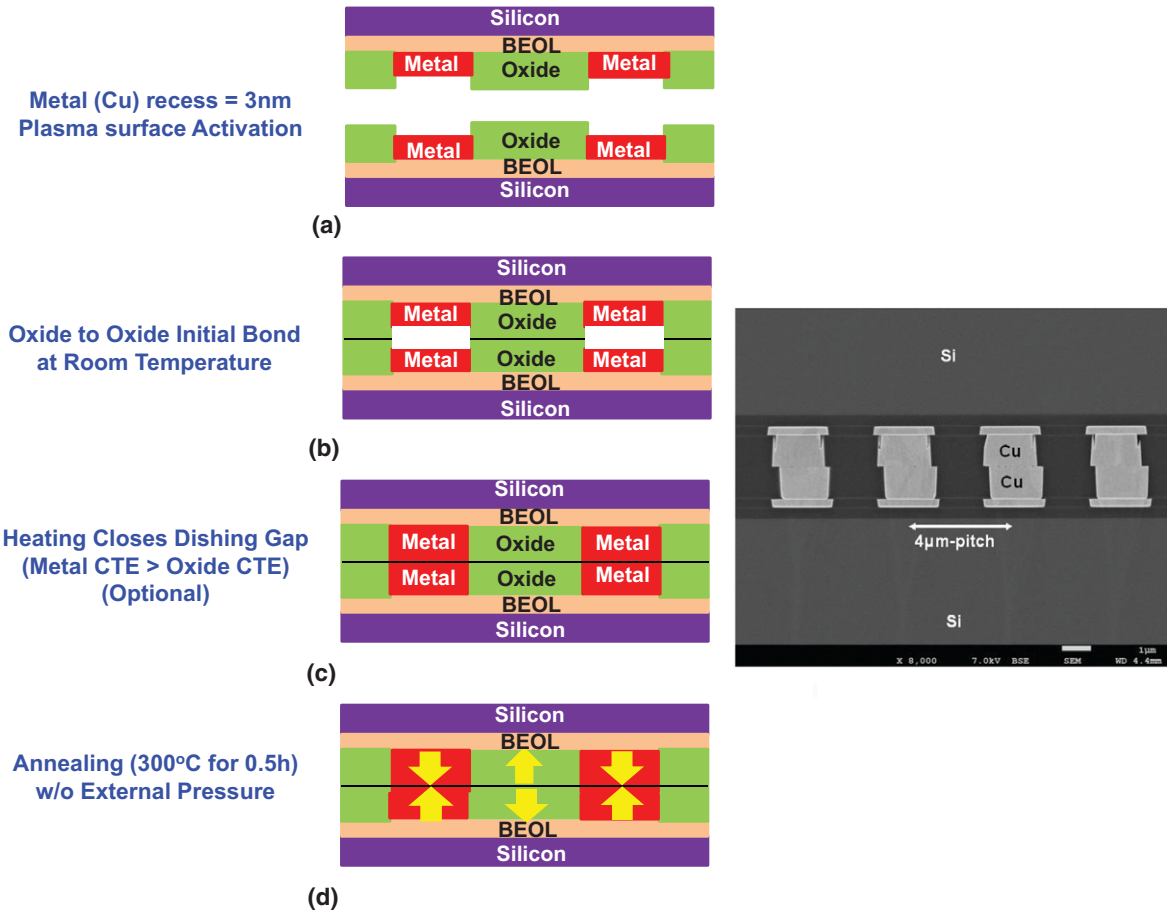

Fig. 21. Key process steps (fundamental) of hybrid bonding.

Some Fundamental on Hybrid Bonding

Fig. 21 shows the key process steps for the bumpless low temperature DBI [17, 43-52]. First of all, controlling nano-scale topography is very important for the DBI technology. The dielectric surface should be extremely flat and smooth before activation and bonding. Chemical-mechanical polishing (CMP) should achieve a very low dielectric roughness ($<$ 0.5nm RMS) and a certain recess of metal areas below the dielectric surface as shown in Fig. 21a. Upon contact, the dry plasma-activated dielectric surfaces bond together instantaneously as shown in Fig. 21b at room temperature. (Very high bond energies can be obtained at very low temperatures as shown in [48].) The dishing gap can be closed by heating as shown in Fig. 21c. (This step is optional because the dishing gap can also be closed by the following annealing step.) Metal-to-metal bond occurs during a subsequent batch annealing. The coefficient of thermal expansion of metals are typically far larger than dielectrics. The metal expands to fill the gap and then build up the internal pressure as shown in Fig. 21d. It is under this internal pressure and annealing temperature that metal atoms diffuse across the interface, making good metal-to-metal bond and hence electrical connection [48]. External pressure is optional for this type of bonding. In this case, the copper oxidation during bonding is minimized. Because the bonded oxide layer surrounding the copper interconnect protects the interconnect from oxidation in the annealing oven, thus minimizing Cu oxidation during the anneal. The bonded oxide surface also hermetically seals the Cu interconnect during operation.

Optimizing the CMP condition is the key to produce the right amount of surface characteristics such as metal recess, dielectric roughness, and dielectric curvature for DBI [48]. Fig. 21 shows an optimal DBI with 4μm-pitch and 2μm-diameter pads.

Sony's CIS with Hybrid Bonding

Sony is the first to use bumpless low temperature Cu-Cu DBI in high volume manufacturing [45, 46]. Sony produced the IMX260 backside illuminated CMOS image sensor (BI-CIS) for the Samsung Galaxy S7, which shipped in 2016. Electrical test results showed that their robust Cu-Cu direct hybrid bonding achieved remarkable connectivity and reliability. The performance of the image sensor was also super. A top view and cross section views of the IMX260 BI-CIS are shown in Fig. 22. It can be seen that, unlike in [88, 89] for Sony's ISX014 stacked camera sensor, the TSVs are eliminated and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu-Cu DBI. The signals are coming from the package substrate with wire bonds to the edges of the processor chip.

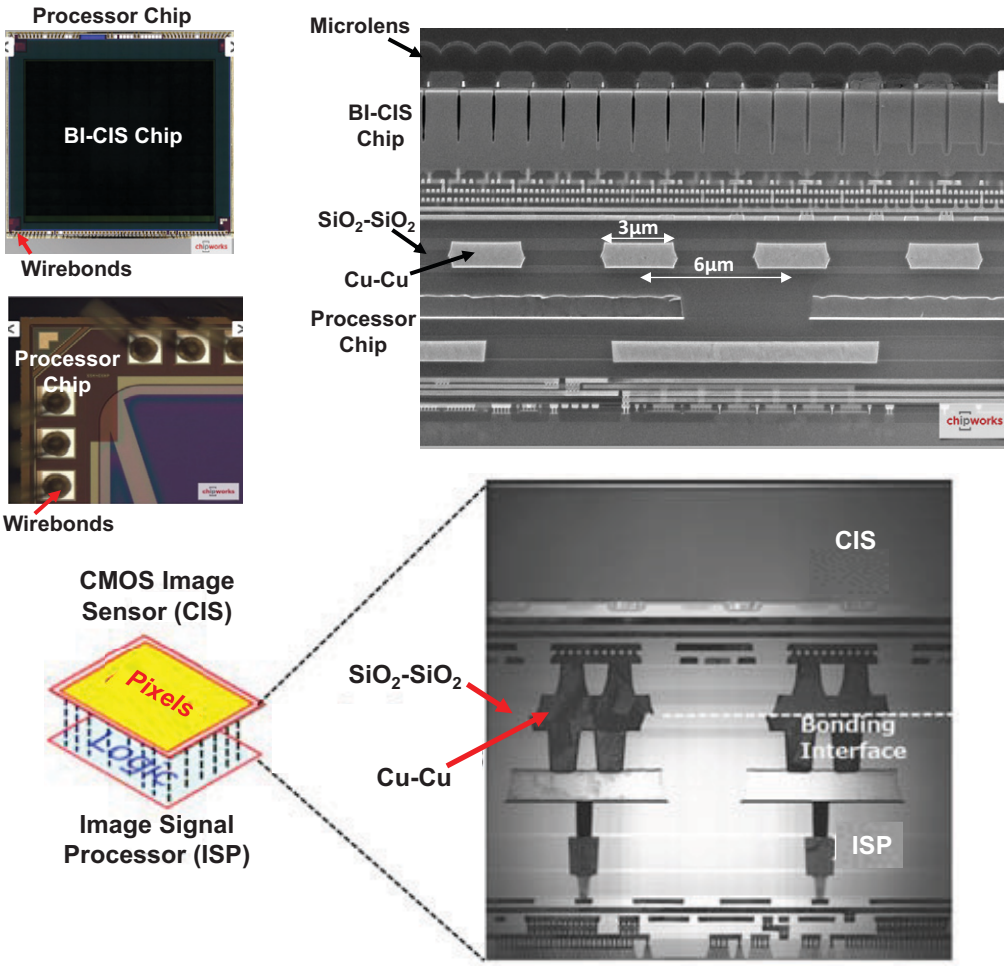

Fig. 22. Sony's CMOS image sensor manufactured by hybrid bonding.

Usually, wafer-to-wafer bonding is for the same chip size from both wafers. In Sony's case, the processor chip is slightly larger than the pixel chip. In order to perform wafer-to-wafer bonding, some of the area for the pixel wafer must be wasted and the additional peripheral area of the processor chip can be used for the wirebonding pads.

The assembly process of Cu-Cu DBI starts off with surface cleaning, metal oxide removal, and activation of SiO_2 (by wet cleaning and dry plasma activation) of wafers for the development of high bonding strength. Then, use optical alignment to place the wafers in contact at room temperature and in a typical cleanroom atmosphere. The first thermal annealing (100-150°C) is designed to strengthen the bond between the SiO_2 surfaces of the wafers while minimizing the stress in the interface due to the thermal expansion mismatch among the Si, Cu, and SiO_2. Then, apply higher temperature and pressure (300°C, 25kN, 10-3Torr, N2atm) for 30 min to introduce the Cu diffusion at the interface and grain growth across the bond interface. The postbond annealing is 300°C under N2atm for 60 min. This process leads to the seam-less bonds (Fig. 22) formed for both Cu and SiO_2 at the same time.

Other Hybrid Bonding

Besides Xperi and Sony, there are many others [7-13, 51-87] who are also working on hybrid bonding. In this paper, only AMD, TSMC and Intel's works are briefly mentioned.

AMD's 3-D chiplet design and heterogeneous integration packaging for Ryzen 9 5900X (Fig. 9) is fabricated by TSMC's 7nm process technology. The chiplets will be SoIC stacked as shown in Fig. 14a by bumpless Cu-Cu hybrid bonding and the chiplet SoIC module will be packaged (bonded) on an active TSV-interposer as shown in Figs. 9 and 15a. It is scheduled to be released by the end of 2021 or early next year.

During Intel Architecture Day (August 13, 2020), Intel presented a hybrid bonding technology with their FOVEROS (also called FOVEROS Direct in [12]) along with the conventional µbump flip chip technology as shown in Fig. 12. It can be seen that with the hybrid bonding technology the pad pitch can go down to 10µm and with 10,000 bumpless interconnects per mm^2. This is many times more than the one with 50µm-pitch µbump flip chip technology. FOVEROS Direct is one of Intel major packaging innovations in the near future [12].

Summary

Some important results and recommendations are summarized as follows.

- SoCs with finer feature sizes are and will be here to stay. Chiplet designs and heterogeneous integration packaging provide alternatives to SoCs, especially for advanced nodes which most companies cannot afford.
- Chiplet is a chip design method while heterogeneous integration is a chip packaging method.
- There are at least two different chiplet designs and heterogeneous integration packaging, namely (1) chip partition and integration (driven by cost and technology optimization) and (2) chip split and integration (driven by cost and yield).
- The key advantages of chiplet design and heterogeneous integration packaging comparing with SoCs are: (1) yield improvement (lower cost) during semiconductor manufacturing, (2) fast time-to-market, (3) cost reduction during design, (4) better thermal performance, (5) reusable of IP, and (6) modularization. The key disadvantages are: (1) additional area for interfaces, (2) higher packaging costs, (3) more packaging complexity and design effort, and (4) past methodologies are less suitable for chiplets.
- Rigid bridge technology such as EMIB for chiplets' horizontal interconnects in organic substrate has been in production. Recently, there are many publications on rigid bridges embedded in fan-out EMC. LCP-flexible bridge could be very useful for millimeter wave high-frequency applications.
- Hybrid bonding can be applied to very fine pitch (as low as 4μm) pads and used for extremely high-density and high-performance applications.
- Hybrid bonding is only suitable for silicon-to-silicon assembly such as CoC, CoW, and WoW. Because of the throughput issue, CoC bonding will not be popular. Because of the chip-size and yield issues, WoW bonding is limited even it will be used more than today. Because of the flexibility, CoW will be the mainstream and it is the most challenge such as the edge effects, contaminants, and particles due to singulation and the requirement of higher accuracy pick & place (P&P) machines and slightly larger pads to compensate the P&P tolerance.

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