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Design and Architecture Definition for Advanced 3D Fan-Out Wafer-Level Packaging

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***Abstract*—Advanced 2.5D/3D wafer-level fan-out packaging technologies have been studied widely in literature and industry in recent years. Miniaturization, reduction in manufacturing costs, improvement in performance, and lower power consumption using packaging technologies drive increase in interconnect density and pitch scaling. Heterogeneous systems in package used in advanced packaging often include a combination of silicon, epoxy underfill or mold compounds, and organic or inorganic passivation or redistribution layers. This heterogeneity poses challenges with manufacturability, process selection, package architecture, and test vehicle design. The coefficient of thermal expansion mismatch, wafer warpage, and wafer yield are some of the critical process challenges. Delamination of silicon side wall or passivation to epoxy underfill or mold compound, joint fatigue are critical reliability challenges. This article explores various processes and reliability challenges with 3D wafer-level fan-out packaging and provides package design and architecture guidelines to overcome these failure modes. Stacked die-to-wafer test vehicles have been used for data collection. Different assembly materials, processes, and tooling have been evaluated to define comprehensive design rules.**

***Keywords*—Fan-out wafer level, advanced packaging architecture, Foveros, 3D stack, underfill, epoxy mold compound, package design, reliability**

Introduction

Recent advances in microelectronics packaging have been propelled by increasing requirements for high performance, smaller size, lower costs, higher reliability, and end-use-based optimization of the product solution. These solutions involve customizing product architecture to include higher bandwidth, reduced power consumption, and higher functionality. These requirements cannot be met with single-die architectures due to yield, inability to accommodate different silicon nodes, and lack of scalability. To enable the product requirements, heterogeneous integration of components onto a single package is essential. Heterogenous integration architectures have become necessary to allow for multifunctional dice on the same package at tight pitches with fan-out capability, at low cost and high flexibility based on end use. Thus, the role of packaging has gained prominence to meet performance needs [1, 2]. Intel is leading the development and high-volume manufacturing of various advanced packaging architectures such as Embedded Multi-die Interconnect Bridge (EMIB), Foveros, CoEMIB, hybrid bonding, and copackaged optics, as seen in Figs. 1 and 2.

This article will focus on 3D Foveros architecture which involves 3D die stacking allowing for thousands of direct 3D die-to-die interconnects. An example of wafer-level assembly architecture is shown in Fig. 2. The base die and top dice can be of different process nodes, to allow for integration of multifunctional components in the package. The base die and top dice are sorted before 3D stack bonding, thus reducing die and wafer wastage, ensuring only known-good top dice are bonded onto known-good base die/wafer. This improves the yield significantly and reduces processing costs. The short interconnect length arising from 3D stacking results in low signal loss thus enabling high performance at lower power. Foveros architecture also allows for integrating different types of thermal solutions. Additionally, the ability to integrate external silicon into the architecture along with compatibility with other types of architectures, such as EMIB, copackaged optics, and glass core substrates, makes Foveros one of the most flexible and versatile architectures in the market.

This article will discuss the key factors impacting processability and reliability and will provide design guidelines to consider while designing a 3D heterogeneous architecture. The section "Design Considerations" will summarize the key factors impacting package performance, processing, and reliability and will provide recommendations for designing a 3D heterogeneous packaging solution. The section "Process and Reliability Challenges" will focus on the failure modes associated with dimensional, material, and process parameters, such as die/package dimensions, Re-Distribution Layer (RDL) and through silicon vias (TSVs) density, underfill, mold compound, and carrier adhesive materials, and leverages the learnings to propose potential solution paths to overcome these failure modes.

Design Considerations

The fundamental understanding of materials, process, and tool interactions is key to design a reliable package [4, 5], especially with complex wafer-level heterogeneous architectures described in this article. A simplified process flow for constructing a Foveros die complex is shown in Fig. 3. Presingulated top die are attached using microbumps to a silicon interposer containing TSVs. The silicon interposer can be active or passive silicon and can have multiple routing or redistribution layers that are not shown in the figure. The package facing bumps on the

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Fig. 1. Intel packaging technology portfolio.

interposer can be plated either at the beginning or end of the process flow; carrier wafers are used for support accordingly.

After the top die are attached, an underfill is dispensed to encapsulate the microbumps. This is then followed by a wafer level molding process to overmold the die. The mold compound and the top die are then planarized to create a level surface. Finally, a wafer saw is used to singulate the wafer into individual die complexes.

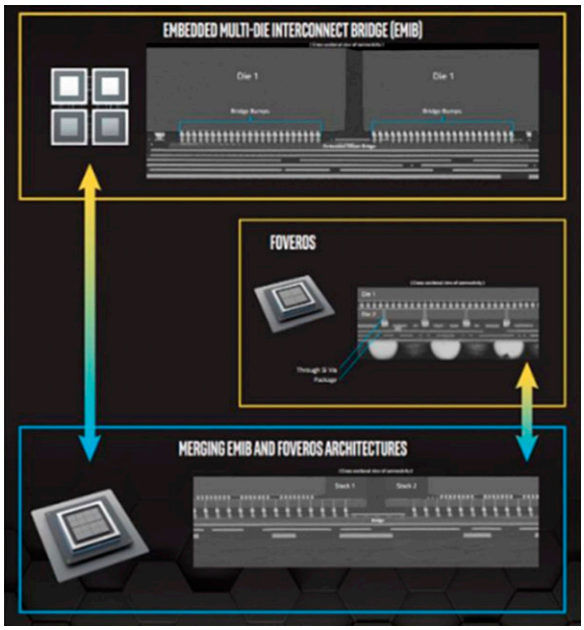

Fig. 2. Schematic and cross-section view of wafer-level advanced packages [3].

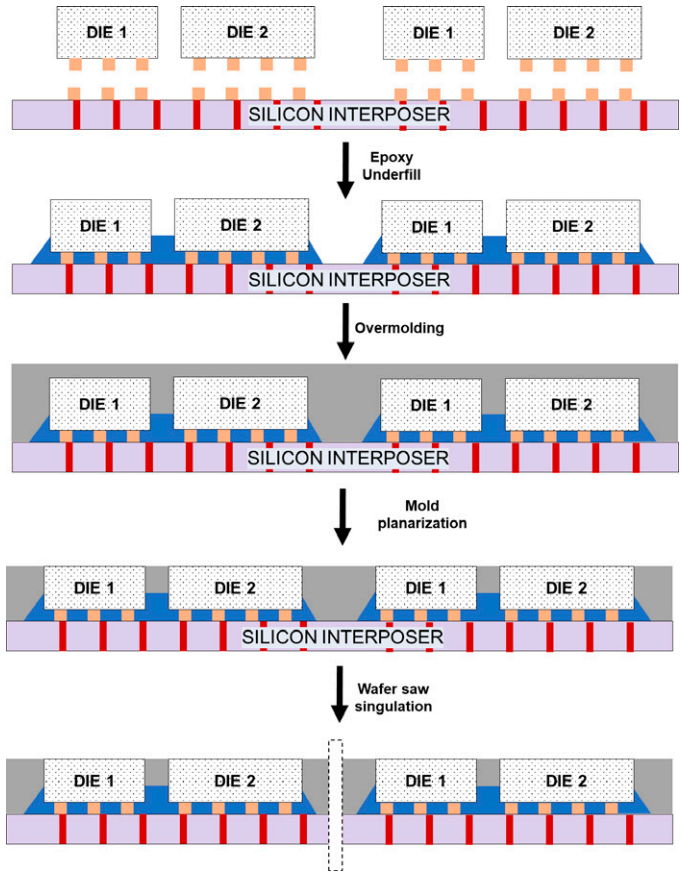

Fig. 3. Simplified process flow for Foveros construction.

Fig. 4 shows the final design of a typical Foveros die complex. Three important design elements in Foveros construction: (1) mold shelf, (2) top die-to-die (D2D) spacing, and (3) dummy die, will be discussed in this section.

A. Top D2D Spacing

When the top D2D spacing becomes too small and approaches the pick and place tolerance of the die attach tool, die collision can occur where the die being attached can collide with the adjacent die that have already been attached. This can cause silicon chipping and cracking leading to electrical failure within the die.

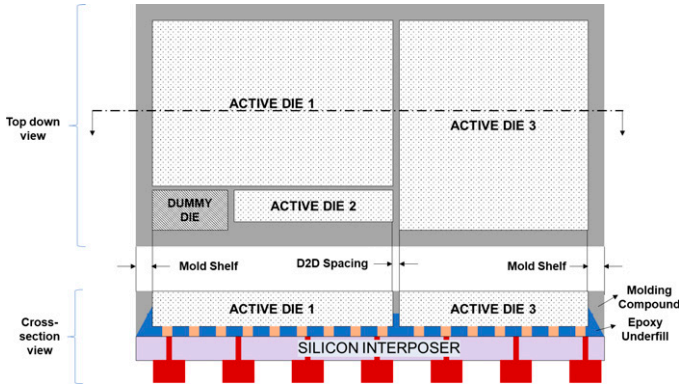

Fig. 4. Construction of a Foveros die complex.

Hence, the spacing must be wide enough to accommodate the pick and place tolerance of the die attach tool with enough of a tolerance margin to account for process and tool-to-tool variations in a high-volume manufacturing environment.

Another fail mode observed when the D2D spacing becomes larger was delamination of the wafer epoxy material from the silicon sidewall during epoxy cure (Fig. 5). During the curing process, a peeling stress is induced at the epoxy-silicon interface due to a combination of cure shrinkage of the epoxy material as well as the coefficient of thermal expansion (CTE) mismatch between the silicon and the underfill. This delamination can propagate into the active silicon because of thermomechanical stresses induced during the subsequent assembly process steps or customer end use of the package.

Finite element modeling was performed to simulate the peel stress at this interface at various D2D spacings. The normalized results are shown in Fig. 6. As D2D spacings become larger, the stress at the wafer-epoxy interface was found to increase and start to exceed the peel strength of the interface.

In summary, while low D2D spacings are needed to avoid the wafer epoxy to silicon sidewall delamination, too low of a spacing leads to die collision. Hence, the ideal D2D spacing for current Foveros construction falls within a very narrow band of ~20μm. The mechanical properties of the epoxy material such as CTE and elastic modulus, its cure kinetics as well as the silicon-epoxy interface adhesion strength modulate this allowable D2D spacing. At the same time, modifying these properties can have detrimental effects on multiple downstream process steps along with important characteristics such as wafer warpage at these steps (discussed in the section "Warpage"). So, it is not straightforward to modify the epoxy material to increase the allowable D2D spacing band. Interesting, extremely large spacings, of the order of several hundred microns, were also found to be viable as this causes less epoxy material to fill the D2D space, thereby reducing the peel stress. However, this is not desired in general as it greatly increases the die-to-die routing lengths.

B. Mold Shelf

The mold shelf (shown in Fig. 4) is the distance from the edge of the top die to the edge of the silicon interposer. This shelf exists primarily to ensure that the top die do not interfere with the wafer saw blades during the final singulation step that creates individual Foveros die complexes after the top die to silicon interposer attach and epoxy steps. Aside from this, the shelf provides flexibility to optimize individual top die sizes without requiring their edges to precisely line up. Finally, circuitry in the active base die may require the base die size to exceed the size needed to accommodate all the top die. The size of this shelf is critical to various fail modes. Fig. 7 illustrates how the shelf size influences the amount of underfill and mold compound at the edges of the die complex.

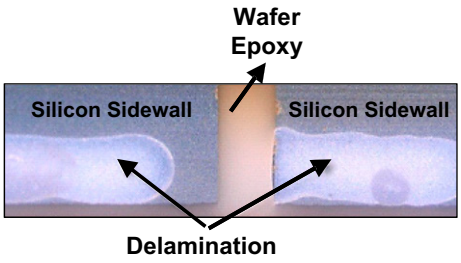

Fig. 5. Cross-section image of wafer epoxy to silicon sidewall delamination.

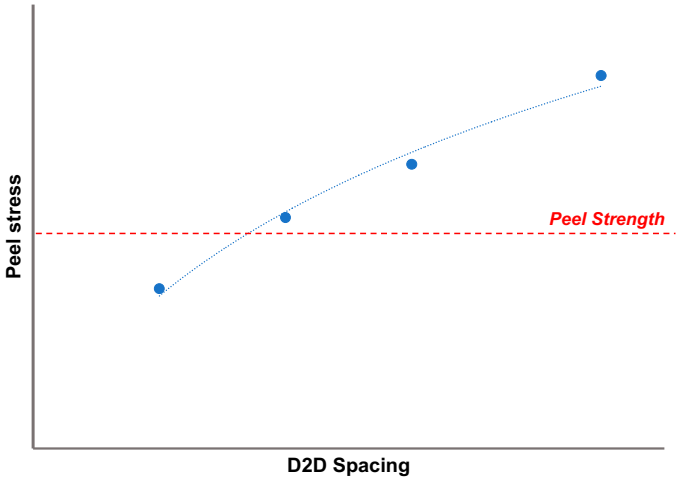

Fig. 6. Finite element modeling results for peel stress at the silicon-wafer epoxy interface at various D2D spacings. The modeling does not cover spacings of several hundred microns where the peel stresses are expected to decrease again.

On the lower side, too small of a mold shelf provides insufficient space for dispense and spread of the underfill material. This leads to a poorly formed underfill fillet as shown in Fig. 7a which was found to cause cracking during the mold planarization process. This is because the softer underfill material gets ground away faster than the mold compound and silicon which get removed at similar rates. This creates an uneven surface during the planarization process and can cause the grind wheel to make contact with the silicon at an angle, leading to cracking. The smaller mold shelfs also lead to very little mold at the shelf region which increases the risk of mold delaminating and falling off the die complex. Fig. 7b shows a more ideal geometry for underfill and mold compound at the edges of the die complex.

Larger mold shelf on the other hand leads to high localized die warpage due to CTE mismatch between the mold and the silicon as illustrated in Fig. 8. This can cause package solder bump bridging during the die-to-substrate bonding process. The uneven die-to-substrate standoff height caused by this localized warpage can also affect the flow of the package-level epoxy leading to epoxy voiding. For thermal compression die-to-substrate bonding processes, excessive mold also reduces heat transfer to the solder bumps which can lead to noncontact opens. This is because mold compounds are poor conductors of heat with thermal conductivities typically <10 W/mK compared with ~148 W/mK for silicon. Active base die may also run into heat dissipation challenges for the same reason. Recent developments include use of filler materials that have high thermal conductivity and form stable dispersion with mold compound material matric [6-9].

Current Foveros construction has an allowable mold shelf range of several hundreds of microns which is far more flexible compared with the allowable range of D2D spacing. As will be explained next, one of the current challenges in Foveros

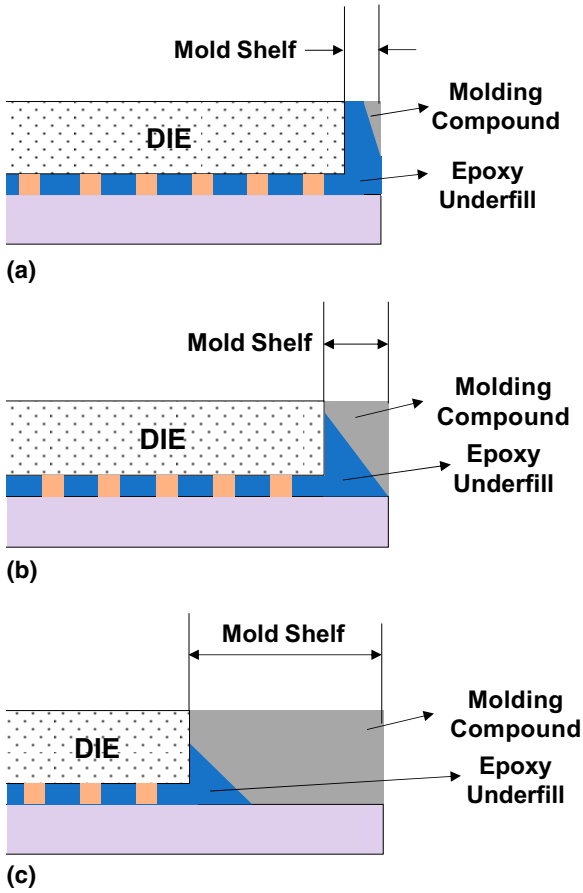

Fig. 7. Illustration of epoxy underfill and mold compound profiles with (a) low, (b) medium, and (c) large mold shelf.

construction is to determine how to enable even larger mold shelfs to keep silicon area and thus, costs down to a minimum.

C. Dummy Die

To keep silicon costs at a minimum, one of the main goals of silicon design is to minimize silicon area while maintaining performance targets. As the design of each top die gets optimized over time and various IP blocks get positioned to meet desired route lengths and other targets, the resulting top die edges do not line up exactly as shown in Fig. 9. This effect is

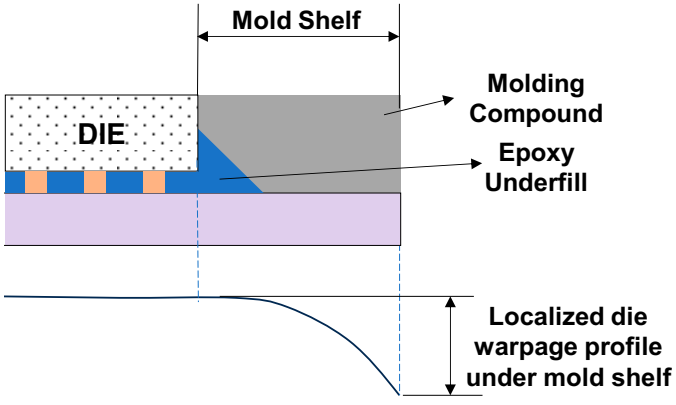

Fig. 8. Localized die warpage under a large mold shelf region.

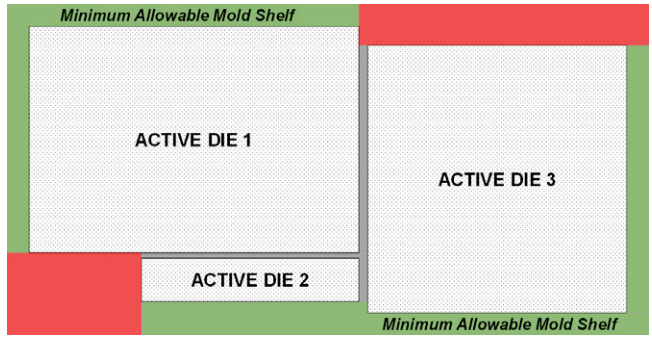

Fig. 9. Mold shelfs after optimizing and laying out active top die. (Areas in green shading are within the allowable mold shelf window while areas in red shading exceed the maximum allowable mold shelf.)

also exacerbated by the tight die to die spacing requirement discussed in the section "Top D2D Spacing".

When the top die-to-die edge misalignment becomes excessive, one or more of the top die-to-base die distances will violate the mold shelf limits described in the prior section. Violations of the lower limit can only be fixed by increasing the base/interposer die size or reducing the top die size (not likely to be possible without losing features or performance). Base die size growth is not prohibitively expensive when passive interposers are used. Violation of the upper mold shelf limit, however, needs to be fixed either by adding dummy silicon to fill up the space or by growing the top die size. Top die size growth is generally cost-prohibitive, especially when newer and more advanced silicon nodes are used for the top die.

There are also minimum size requirements for this dummy silicon to ensure they can be handled by the various pick and place tools during wafer prep and die-to-wafer attach. In cases where the misalignment is less than the minimum dimension and the upper mold shelf limit is exceeded, then the only possible solution is to either grow the top die or the base die (i.e., add "white space") to allow the smallest possible dummy silicon to be fitted.

Figs. 10 and 11 illustrate these various scenarios. In Fig. 10, the mold shelf violation in the bottom left edge is corrected by adding a dummy die. However, the violation in the top right edge cannot be similarly fixed as it would require a dummy die size smaller than the minimum dimension.

Fig. 11a shows how this scenario would be fixed by growing the top die until the top right edge mold shelf meets the maximum allowable value. This is typically the more expensive option especially when passive interposers are used. Fig. 11b

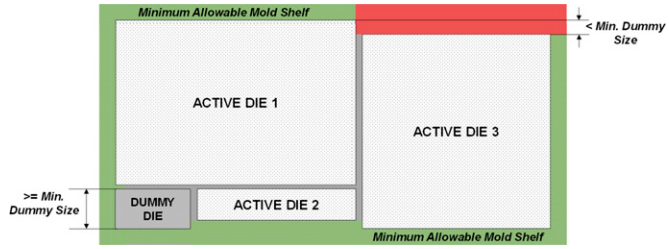

Fig. 10. Fixing the excessive mold shelf at the bottom left edge by adding a dummy die.

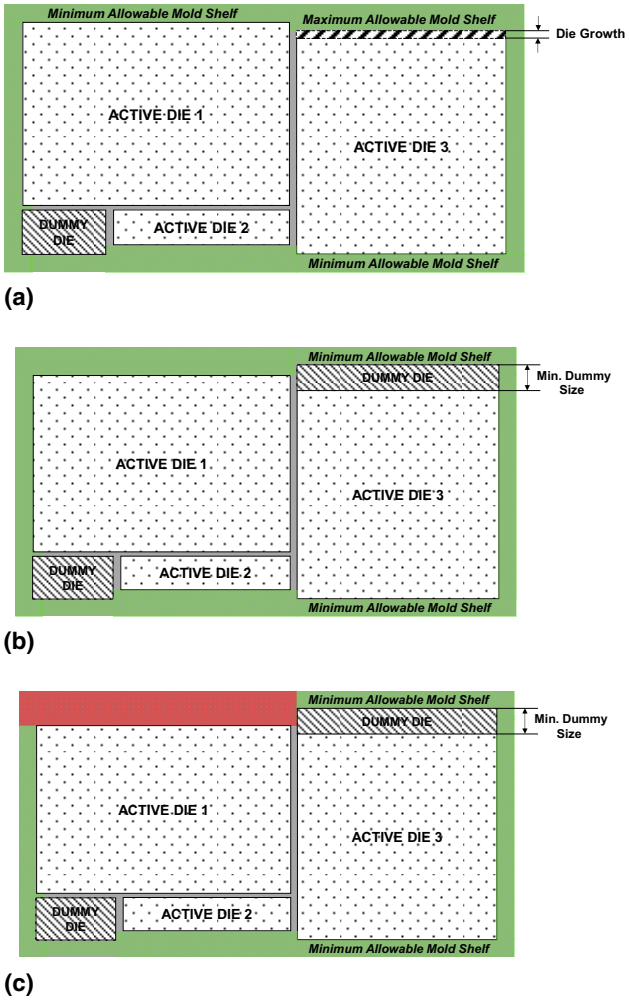

Fig. 11. Approaches to fixing the excessive mold shelf in the top right edge by (a) growing one of the top die, or (b) growing the interposer die without causing other violations. However, (c) growing the interposer die growth can cause excessive mold shelf in other parts of the die.

shows an alternative way to fix this by growing the interposer die until there is enough space to fit a dummy die. However, this would only work if the interposer can be grown without causing the mold shelf in the top left edge to exceed the maximum allowable mold shelf which can happen depending on the amount of top die edge-to-edge misalignment as shown in Fig. 11c. In such circumstances, top die growth is the only way to stay within the mold shelf limits.

The dummy silicon that are added to meet mold shelf limits can hence best be categorized as "design waste" as they provide no value to the overall functionality of the product. They are needed only to satisfy the D2D spacing and mold shelf limits of the Foveros construction. They add cost in multiple ways: (1) cost of the dummy silicon itself, (2) processing cost of dummy silicon (primarily wafer prep and die to wafer attach), and, in some cases (3) unnecessary interposer or top die growth to be able to fit the smallest possible dummy die. In general, designs should strive to minimize the quantity of dummy silicon. One of the focus areas of future Foveros development is to widen the mold shelf and D2D spacing limits to increase design space to avoid dummy silicon.

Process and Reliability Challenges

Process and reliability modulators for advanced packages, such as delamination, warpage, and die/wafer cracks, are impacted as a result of the key design parameters described in the section "Design Considerations". Modeling at a system level for reliability and known failure modes is critical to design a robust package [10, 11].

A. Warpage

Wafer warpage is a function of CTE and different inorganic and organic materials that are used as building blocks for heterogeneous architecture. These building blocks include both direct and indirect material sets. Direct materials, such as silicon, underfill and mold compound, and organic and inorganic RDLs, drive the warpage based on their contribution to the design and architecture. Indirect materials, such as carrier-bond adhesives, can similarly impact modes, such as wafer warpage during processing.

Within direct materials, process parameters, such as—(1) thermocompression bonding conditions; (2) underfill and mold compound material shot weight and total weight per die complex; (3) top die thickness during processing, act as key modulators. Top die thickness enables a larger Si content per unit area of the wafer during processing, which drives the overall stacked wafer CTE to match silicon and in turn drives down the warpage to be closest to silicon. Underfill and mold compound material composition (based on overall content, % of silicon di-oxide or SiO_2-based fillers, glass transition temperature or Tg, and CTE of the epoxy polymer complex) have a significant modulation not just warpage or delamination but also to product reliability and end-use. Process material selection is not straightforward, and it is imperative to optimize process warpage and tool capabilities, along with product end-use reliability, certifiable stress requirement, and yields.

Optimizing D2D spacing with die height and Si content on the x/y axis and thickness on the z-axis is a significant modulator. D2D spacing impacts the routing distance between the top die while underfill or mold compounds modulate the resultant bending moment of the die complex. Both factors in turn drive the overall wafer warpage. D2D spacing and mold shelf additionally impact the delamination stress against the silicon sidewall. It is critical to optimize D2D spacing, mold shelf, and material properties of underfill and mold compounds to best define product design and architecture while balancing electrical as well as thermomechanical performance requirement packages.

Additionally, local and global copper density in the base/interposer wafer is a key modulator for wafer warpage during processing. Population density of TSVs and copper plane or location of focused features in organic/inorganic RDL impacts local undulation of interposer/base wafer as well as global warpage of the Foveros complex. Local undulations have a significant impact on wafer-level processing steps, such as interposer wafer package side bump etch, seed layer deposition, or copper pad plating, whereas global TSV density has a significant impact on process tooling handling capability. There cannot be a specific TSV density recommendation locally or globally, it needs to be optimized with modeling and process data collection for a specific wafer level architecture based on

the parameters described in the section "Design Considerations". Beyond design or architecture considerations, warpage is also impacted during processing via indirect materials such as carrier wafer bond adhesives and debond process. Recent studies have also focused on processing sequence such as mold-first or RDL/interposer-first approaches, RDL/interposer design, direct and indirect material selections as well as post process warpage correction [12-17].

Warpage can be monitored via optical metrology focused on wafer top-to-bottom delta as a process in-line methodology. TSV reveal is impacted by the overall wafer warpage. Wafer warpage may lead to over or under-reveal of TSVs within areas of the wafer. The impact of such defects on specific die located on the wafer can be captured by collecting electrical leakage or resistance data.

B. *Wafer Break*

Wafer break is driven by design-to-process dependencies and inline defects. Design-to-process dependencies can be addressed during product architecture, whereas defect-driven fail modes need to be addressed via tool enhancements and manufacturing excellence. Die design and die singulation process are intimately related to address this issue. Die design dictates the amount of copper layers present in between die or test pads needed to test the die performance. Singulation processes, such as laser and mechanical saw interact with the copper, remain within the interdie area during the process. Interaction of laser with copper layers in the interdie region can lead to local cavitation and subsequent formation of pits or defect initiations in wafers [18]. Similarly, mechanical saw blades can interact with remnant copper layers and cause chipping defects along the Si sidewall as well as tool damage [19]. Remnant copper in the interdie region can be optimized via die and wafer frame design. Process parameters, such as laser fluence and intensity, number of passes and overlap; or saw blade width, blade grit size, and speed, can all be optimized to identify a process range with minimal defects.

Wafer cracks can also be driven by defect-induced failure beyond the scope of design and architecture, such as—foreign material (FM) on processing tools, or deformation or degradation of tool components over time. High-pressure processing steps, such as wafer molding or wafer grind, can cause direct wafer failure if FM is present on the processing surface. FM integration for conventional packaging is well understood; however, it is relevant to understand the impact of FM on advanced packaging architectures [20]. Trim and saw tool components interact with remnant copper in the wafer architecture and tend to wear off over time which can also cause a significant impact on wafer yields (as shown in Fig. 12). The impact of this type of failure is not just to the wafer in process, but also extrapolates to subsequent wafers in the tool, as well as cost associated with part change on the tool and manufacturing down time. Secondary defects, such as chipping at wafer notch, cause false detection in tool optical systems also leading to manufacturing challenges [19]. Wafer-based advanced packaging design and architecture needs to consider the sensitivity of tooling to Si versus complex fluids (such as underfill or mold compounds direct materials, and temporary bond/debond indirect materials) as well as the propensity of tool interaction

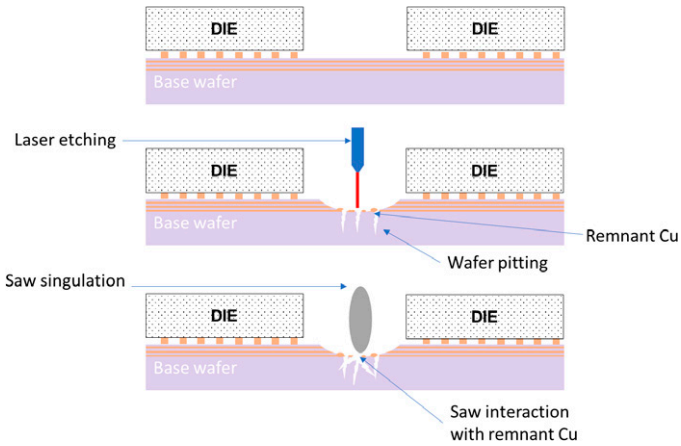

Fig. 12. Wafer crack/break driven by base wafer metal layer design and interaction with singulation process.

with heterogeneous complexes as a part of the design rules or guidelines [15, 21]. Both types of defects lead to direct full wafer loss, which has a significant impact on product yield. These defects can be captured via in-line optical imaging analysis or laboratory-level failure analysis, such as depth profile, infra-red laser scanning confocal microscopy, scanning electron microscopy, focused ion beam cut, and imaging [21].

C. *Solder Volume and Intermetallic Compound Content*

Solder volume is a significant technology driver especially as the focus of future heterogeneous technologies shifts toward tighter bump pitch, lower signal loss, and higher performance. It is also critical to design the wafer-level solder composition compatible with package and board-level solders as they directly impact the warpage of the system. At the package-level, low-temperature solders are gaining prominence to reduce warpage and thermal stresses in the package [22]. For die-to-wafer or wafer-to-wafer bonding technologies that use aggressive solder base bump pitch and limited total solder volume, optimizing solder volume to suit manufacturability as well as reliability becomes critical [23, 24]. As explained in Fig. 13, intermetallic compound versus free solder content can be optimized by modulating solder volume as well as thermal exposure during the process, based on the end use both at wafer and package level interconnects with aggressive pitch. Higher free solder content is preferred for use cases in consumer electronics that require higher thermal cycling and drop/shock performance [25-27].

Key risks, drivers, or modulators and dependencies are summarized in Fig. 14.

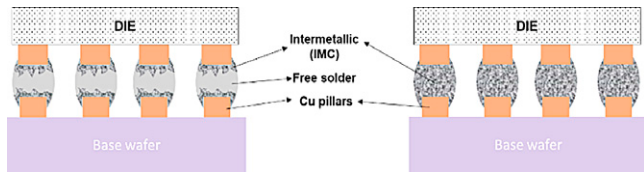

Fig. 13. Die-to-wafer joint based on solder content—free solder focused joint (left) and full IMC joint (right).

Key risks	Driver/Modulator	Dependencies
Warpage	1. Underfill and mold material composition/CTE 2. Silicon to organic ratio, including top die height and die to die spacing for top die (driving die coupling/ bending moment) 3. Local and global copper/TSV density in base wafer.	1. Overall organic material down selection for underfill/mold compound and processibility through downstream fabrication steps (TSV reveal, bumping, singulation etc.) 2. Overall stacked die complex warpage and impact on process window for thermocompression bonding to package. 3. Overall package warpage impacting board level surface mount (SMT) and system level yield and reliability
Wafer break	1. Foreign material (FM) driving creation of defect on the stacked wafer. 2. Laser or saw based singulation process leading to creation of local "sensitive" area on the wafer that are susceptible to crack or break.	1. FM or process defect-based factors leading to yield loss of a full stacked wafer (includes expensive compute, graphics, AI and BIOS IPs). 2. Defects that do not result within process yield loss, could remain as a walking-wounded time zero reliability marginality in the field.
IMC content	1. Solder plating volume for top die to base die interconnect is dependent on wafer level interconnect pitch target and signal/power integrity(SI/PI) requirements. 2. Degree of IMC/time zero metallurgy of interconnect is dependent on end use condition of the package or system.	1. Higher performance (SI/PI) requirements translate to tighter pitch and lower solder volume to minimize electrical loss. 2. Consumer electronic requirements drive a higher temperature cycling reliability requirement where was server/GPU systems drive a higher requirement for high temperature bake. Degree of IMC in the package technology can be optimized based on this end use delta.

Fig. 14. Summary table for process and reliability challenges with dependencies.

Conclusions

Design and architecture are critical knobs to enable an optimum output for processability, yield, and reliability while developing 3D wafer-level fan-out packaging and other advanced packaging approaches. Key wafer level design parameters and their impact on over all process, yield and reliability are discussed in the article. This path of research can further explore the impact of design and process for next-generation architectures such as hybrid bonding, multilevel wafer stacking, and copackage optics.

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