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Fine-Pitch Copper Pillar Flip Chips in High Reliability Applications

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***Abstract*—To keep up with the demands for smaller antennas with increased performance and decreased costs, most next-generation architectures mandate higher integrated circuit (IC) chip integration. Compared to conventional packaging configurations, advanced chip packaging technologies, such as 2.5D and 3D, offer greater chip compatibility and lower power consumption. Given these advantages, the adoption of advanced packaging is inevitable. Within advanced packaging, the copper pillar interconnect is a key enabling technology, and the next logical step. This technology offers several benefits, including improved electromigration resistance, improved electrical and thermal conductivity, simplified under bump metallization (UBM), and higher input/output (I/O) density. The fine pitches that copper pillars allow help the technology to supersede solder bump technology, which reaches its lowest pitch at around 40 microns. Finer pitches allow for a higher I/O count, which increases performance. In this work, the assembly of ultrathin monolithic microwave integrated circuit (MMIC) gallium nitride (GaN) fine-pitch copper pillar flip chip assemblies on high-density interposers was successfully demonstrated. Using the 150-μm pitch copper pillar flip chip, the assembly processes for both organic printed circuit board (PCB) and silicon interposers were evaluated, with both an electroless nickel immersion gold (ENIG) and eutectic tin-lead solder pad finish evaluated. For the 2D/2.5D/3D assembly process development, a standard in-house pick and place tool was used, followed by mass solder reflow, finished with an underfill for reliability test. The interconnect robustness was determined by die pull strengths, a flux stamping investigation, and cross sections. Complete reliability and qualification test data on GaN copper pillar flip chip 2D assembly was completed, including 700 temperature cycles and unbiased highly accelerated temperature/humidity stress test (UHAST). Adding copper pillar technology to GaN MMIC dice, integrating GaN Cu pillar technology into 2.5D/3D packaging technology, and assessing GaN Cu pillar interconnect reliability at the interposer level are all unique aspects of this work.**

***Keywords*—2D, 2.5D, 3D, copper pillar, GaN, MMIC, reliability, temperature cycle, UHAST, COTS**

Introduction

Looking closer at the evolution of phased array radar architectures over the last few decades, it is obvious that the future will require denser packaging. The next generation of radar systems will require operating at wider frequency and bandwidths, capable of handling higher traffic, integrated elemental digital beamforming, lower power consumption, smaller footprint, lighter weight, lower cost, and higher reliability. By increasing the I/O count and switching from antiquated wire bonding to advanced packaging, the new radar systems will rise to meet all of the intense requirements. Because of the harsh environments that radars are exposed to, such as areas with high radiation and high-temperature fluctuations with zero tolerance for failure, the reliability of the packages is the key. For high-density advanced packaging, the interconnects are the critical failure points. Thus, the reliability of the interconnects is essential to understand.

In this work, assembly challenges in 2D/2.5D/3D ultrathin gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) fine-pitch copper pillar flip chip die were investigated. Reviews of previous work done by several researchers are listed in the references [1-6]. Wei-Wei (Xenia) Liu et al. provided a methodology to improve coplanarity by collocating oval and circular solder bumps. The paper reported that better coplanarity can be achieved by the proposed method to collocate different bump shapes. Numerous variable factors were reported, such as process control, unoptimized plating parameters, or bump shape, which were directly related to poor coplanarity. That paper aimed to provide a creative design rule, where active copper pillar bumps were collocated with dummy bumps, to solve the coplanarity mismatch issue [1-3]. Bong et al. presented novel and effective methodologies showing how a 500-DPPM (defective parts per million) copper pillar bump defects were detected, tracked, and fixed to ultimately improve the yield and lower DPPM [4]. Islam et al. addressed the risk factors for fine bump pitch flip chip assemblies, risk mitigation plans, comprehensive assembly and reliability data, and cost benchmarking. Several case studies with fine-pitch copper pillar bumps were considered in this study [5]. Fu et al. discussed the successful development of copper pillar bumps for the 7 nm technology [6].

In this work, ultrathin MMIC GaN fine-pitch copper pillar flip chip assemblies on high-density interposers were successfully demonstrated. Using a 150-μm pitch copper pillar flip chip, the assembly processes for both organic (printed circuit board [PCB]) and silicon interposers were evaluated, both with an electroless nickel immersion gold (ENIG) pad finish. For the 2D/2.5D/3D assembly process development, a standard in-house pick and place tool was used, followed by mass solder reflow, finished with an underfill for reliability. The interconnect robustness was determined by die pull strengths. Complete reliability and qualification test data on GaN copper pillar flip chip 2D assembly was completed, including 700

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temperature cycles and unbiased highly accelerated temperature/humidity stress test (UHAST) testing. This article was structured based on the following three sections. Section II showed the assembly process developments of the fine-pitch copper pillar 2.5D/3D assemblies using an 80-µm pitch test vehicle. Section III showed the underfilling process development for fine-pitch copper pillar, using a 150-µm pitch test vehicle. Section IV showed the reliability evaluation of ultrathin GaN MMIC copper pillar flip chip die on two different interposers, such as organic and silicon, using a 150-µm pitch test vehicle.

2D/2.5D/3D Copper Pillar Assembly Process Developments

For this part of the experiment, the assembly methods were investigated, to understand the best approaches for creating 2D/2.5D/3D assemblies. The process steps were developed specifically to evaluate the robustness of the copper pillar interconnects for 2D/2.5D/3D assemblies to satisfy the stringent reliability criteria of defense customers. In this study, the assembly parameters and variables were taken into account, including copper pillar pitch, interposer type, interposer pad finish, and bonding method, listed in Table I.

The key assembly inspection parameters that were used to develop the 2D/2.5D/3D assemblies are listed in Table II. For both the inspection and process check requirements, JEDEC and MIL standards were used.

Table I
Assembly Variables and Parameters

Assembly variables	
Pitch	80 µm/150 µm
Interposer types	Organic/silicon
Interposer pad finishes	ENIG/solder
Assembly level	2D 2.5D/3D
Bonding type	Thermo-compression (3D 80 ump) Mass reflow (2D 150 ump)

Table II
Key Assembly Process Parameters and Inspection Criteria

Defects to inspect	Test method
Die crack and chipping	Optical
Die/Interposer warpage	Shadow Moire
Pillar height coplanarity	Profilometer
SOP coplanarity	Profilometer
Paste nonuniformity	Optical inspection/SPI
Flux nonuniformity	Optical inspection
Placement misalignment	x-ray inspection
Reflow profile peak temp and TAL	Thermal profilers
Solder joint voids	x-ray/Cross section
Solder joint nonwet	x-ray/Cross section
Bonding strength	Die pull/Shear test
Flux residue	Die pull
Voids/Fillers separation	CSAM/Cross section
Bump wetting to UBM	Bump shear

SPI, solder paste inspection; TAL, time above liquidus.

A. Flux Dipping Nonuniformity

Before assembly, checking the coplanarity of copper pillars is essential to making sure all pillars make contact with the interposer. In this study, a flux dipping process was used for bonding copper pillar flip chip die on the interposers on 80 µm pitch copper pillar GaN parts. Warpage of the ultrathin MMIC die was observed, which affected the uniform flux printing process. A detailed flux printing and stamping study was performed, to optimize the flux printing process, as seen in Fig. 1. This was achieved by purposely contaminating the pick-and-place tip with flux and setting the nitrogen blow-off time to zero, effectively gluing the die to the tip. The purpose of this study was to see how the warpage of the ultrathin GaN die was affecting placement and flux parameters.

Fig. 2 shows flux missing on many corner pads after the flux stamping process was performed. The same process was repeated for full thick dice, but 100% of the pads had flux residue, as seen in Fig. 3. By comparing the flux patterns left on each interposer between 100-µm thin and full thick dice, it suggests that the 100-µm thin die was warped at the corners, in comparison with full thick dice, which were fairly flat.

The warpage of the dice is measured with a white-light profilometer. The flux stamping nonuniformity on the substrate coincides with the measured warpage data. When compared with full thick copper pillar dice, the 100-µm thin copper pillar dice reveal warpage. Due to the layer of copper pillars, the warpage data suggests that the 100-µm thin die becomes a smiley face or potato chip.

B. Die Pull Test and Failure Mechanisms

To measure the robustness of the copper pillar assembly process, initial die pull tests were carried out based on the MIL-STD-883J. In Fig. 4, a complete die pull failure map of the 80-µm pitch copper pillar solder joint is shown, with most failures being an intermetallic crack. A 3D rendering of failed

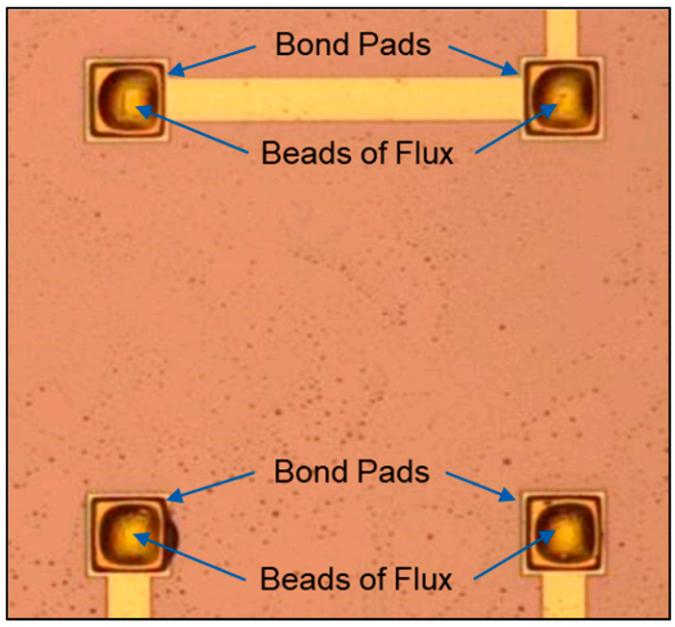

Fig. 1. Flux imprints created by copper pillars during "Stamping" process.

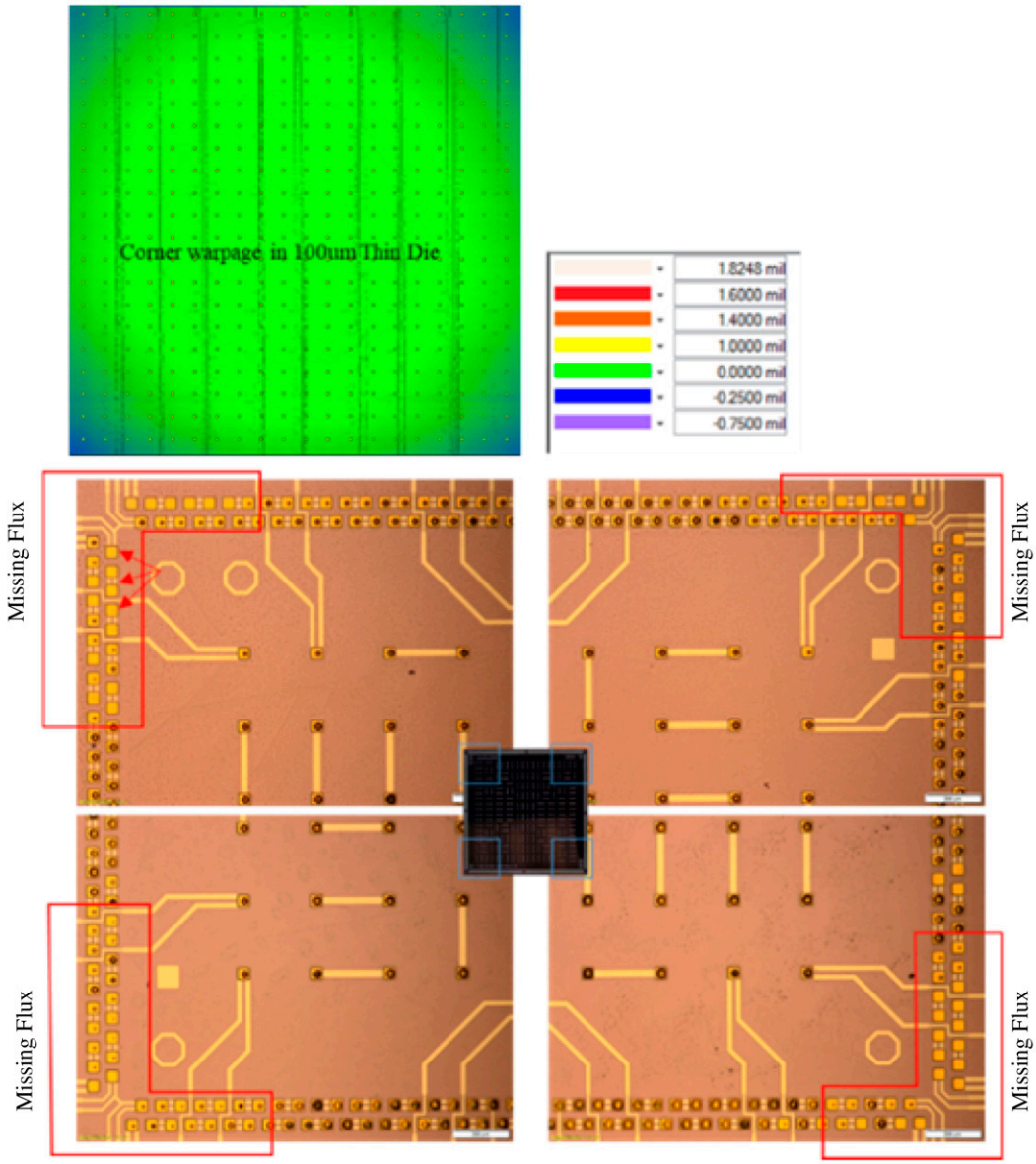

Fig. 2. Flux missing on many corner pads suggesting 100-μm thin copper pillar die are warped at the corners.

copper pillar joints is shown in Fig. 5. Between the pillars and solder interface, much of the copper pillar joint was opened up.

C. *Solder Compared with Electroless Nickel Immersion Gold Pads*

To further increase joint robustness, solder can be stencil printed onto pads. To explore this option, identical commercial off-the-shelf (COTS) parts were assembled and processed together, half with eutectic tin-lead solder applied to the pads, and half with the baseline ENIG pads. Based on the cross sections seen in Fig. 6, the solder applied to the pad increased the overall solder volume, which increased the strength, and therefore the reliability of the assembly. The standoff of the pillar to the interposer was also increased, due to the increase in solder volume. This will help increase the ability of the underfill to flow, as well as increasing the fatigue strength. However, with more solder volume, there is an increased risk for solder bridging, causing the package to short. This presents a challenge around 100 μm and below. The comparison of reliability data for ENIG and solder on pads assembly is shown in Tables III and IV.

To further investigate this, more assemblies and cross sections were created, as seen in Fig. 7 and Fig. 8. More solder and higher standoffs were still present, leading to the conclusion that this process was creating robust interconnections.

D. *2.5D/3D Pick and Place, Reflow, and Assembly*

To conclude the efforts to optimize the assembly process, the bonding type was explored, comparing thermo-compression bonding (TCB) to mass reflow. For the mass reflow process, the 80-μm flip chip dice were flux dipped, placed onto the silicon TSV (through silicon via) interposer, and run through a belt reflow oven, creating results seen in Fig. 9. For TCB,

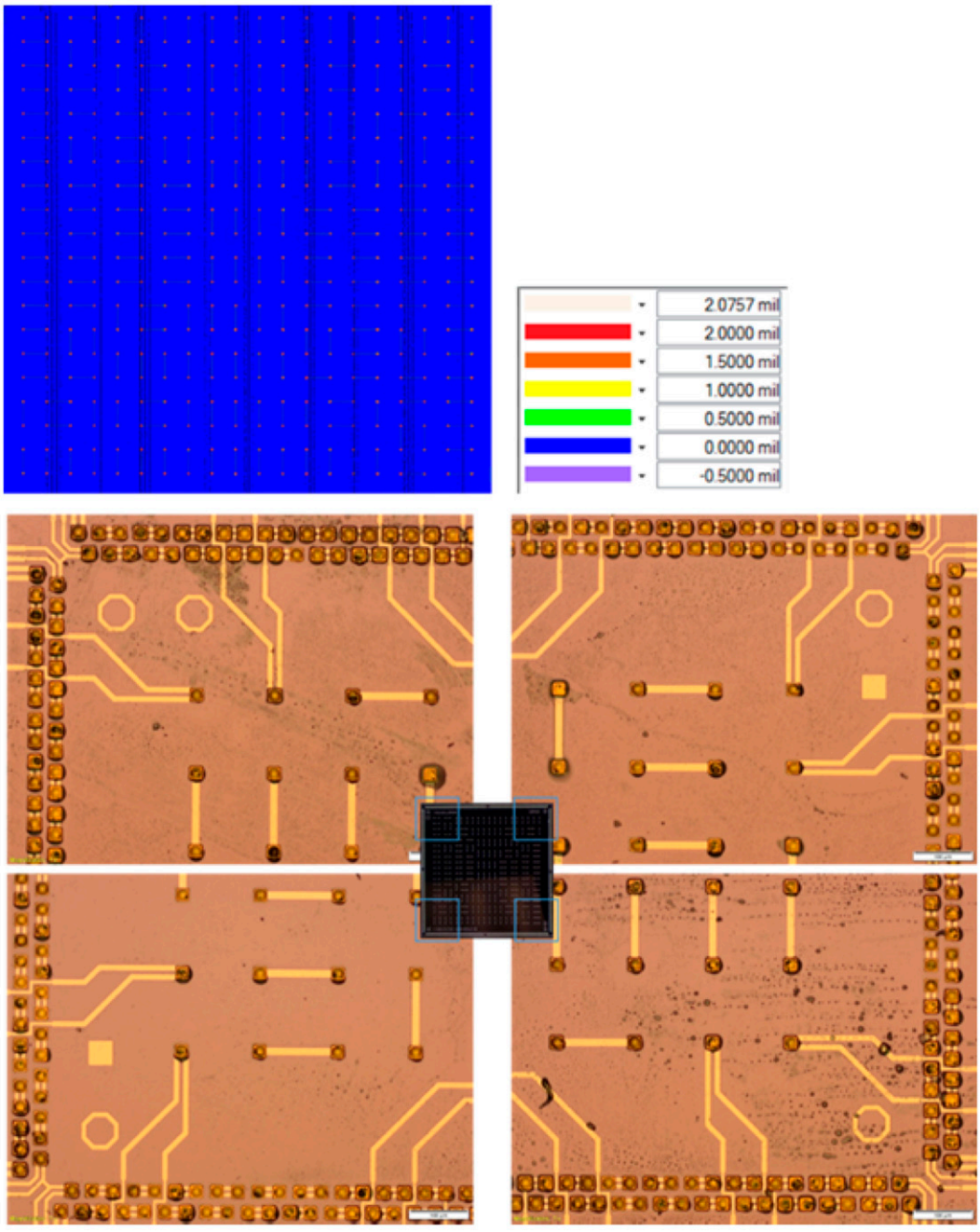

Fig. 3. All bond pads are successfully wetted with flux for full thickness copper pillar die.

force, temperature, and formic acid were used to reflow the solder caps in place, with results seen in Fig. 10. When assembling 3D stacks that included a 100-µm thin TSV die, the warpage of all three components was too much for the flux and solder caps to overcome, especially when utilizing the mass reflow option. Because of the number of opens observed in the mass reflow sample, TCB was the best avenue explored for 3D stacking. Though in both cases, robust copper pillar joints were created.

This conclusion differs from experiments with the 2D stacks, where the warpage of just two die was able to be overcome by the solder caps and flux alone. Because mass reflow is more manufacturable, this avenue was chosen for assembling the 2D components, which are described in sections III and IV of this article.

Fine-Pitch Copper Pillar Underfilling Process Developments

A. Underfill/Flux Compatibility Test

The interaction between the flux and the underfill is important for the long-term reliability of underfilled flip chip devices. After reflow, all fluxes leave residues behind, which is even

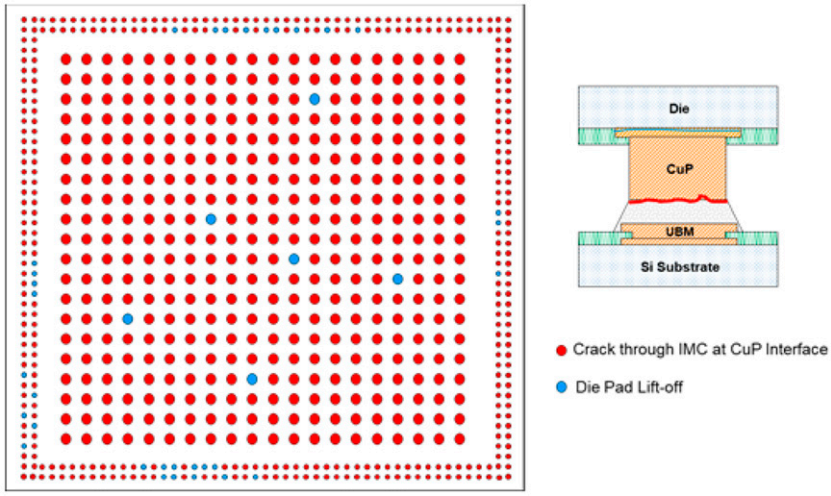

Fig. 4. Post reflow die pull crack maps for 80-µm pitch copper pillar joint.

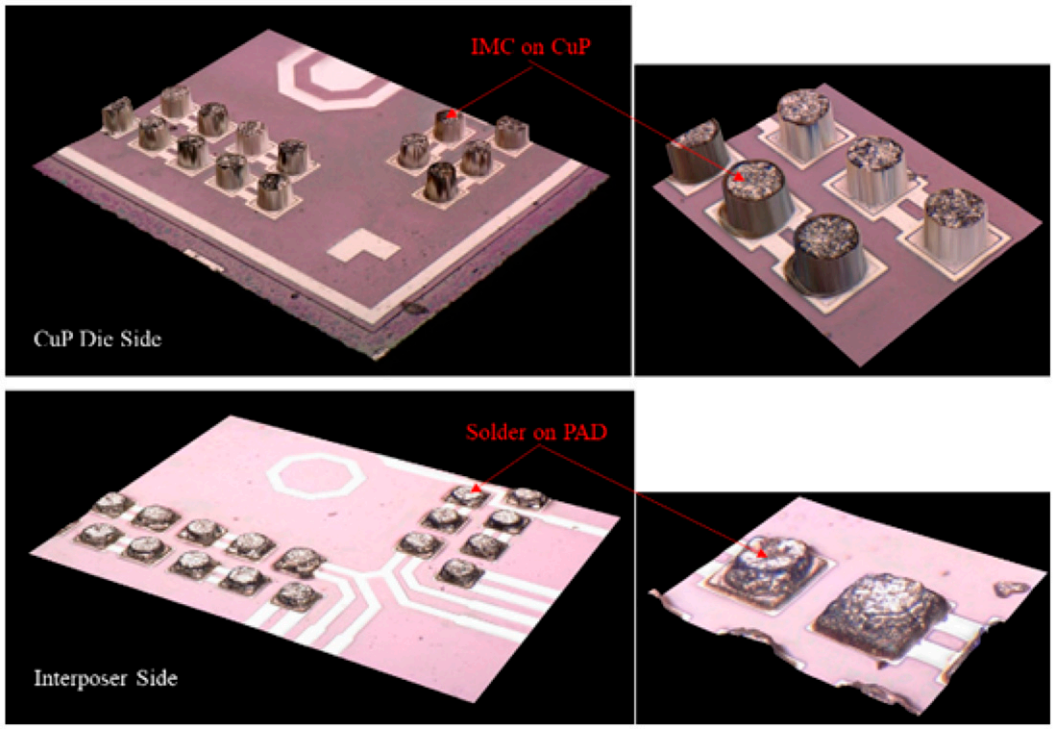

Fig. 5. Copper pillar joint failure interface after die pull test.

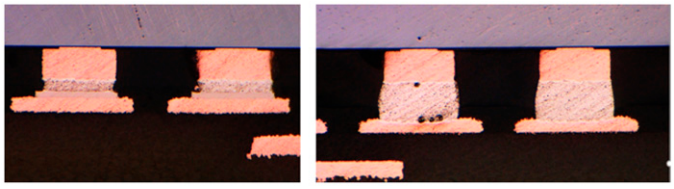

Fig. 6. Cross sections of ENIG pads (left) compared with solder on pad (right).

true for no-clean fluxes. When properly processed, no-clean or low-solid flux residues do not degrade electrical performance but will affect the adhesion and flow of the underfill. Particularly on larger die with small gap heights and pitch assemblies, flux residue is difficult to clean off. An elevated processing temperature is one of the main parameters that can change the characteristics of the flux residue after solder reflow. Thermo-mechanical structural reliability can be influenced by flux

Table III
Temperature Cycle Results

Cu pillar assembly DOE	Pad surface finish	Temp cycle life
Organic interposer	ENIG	T_{ENIG}
	Solder on pads	$>T_{ENIG}$
Silicon interposer	ENIG	$>T_{ENIG}$

Table IV
UHAST Results

Copper pillar assembly DOE	Pad surface finish	UHAST test results
Organic interposer	ENIG	All pass
	Solder	All pass
Silicon interposer	ENIG	All pass

residues in multiple ways. Thin films of flux residue could be present on the solder bump, substrate, or die and can greatly decrease interfacial adhesion. Once the underfilled unit is stressed by thermal shock, moisture, or other variables, the underfill begins delaminating from the surface. Fluxes can also affect reliability by physically impeding the flow of the underfill material. Flux residue builds up in gaps and can narrow the gap to a point where the underfill cannot flow properly, which

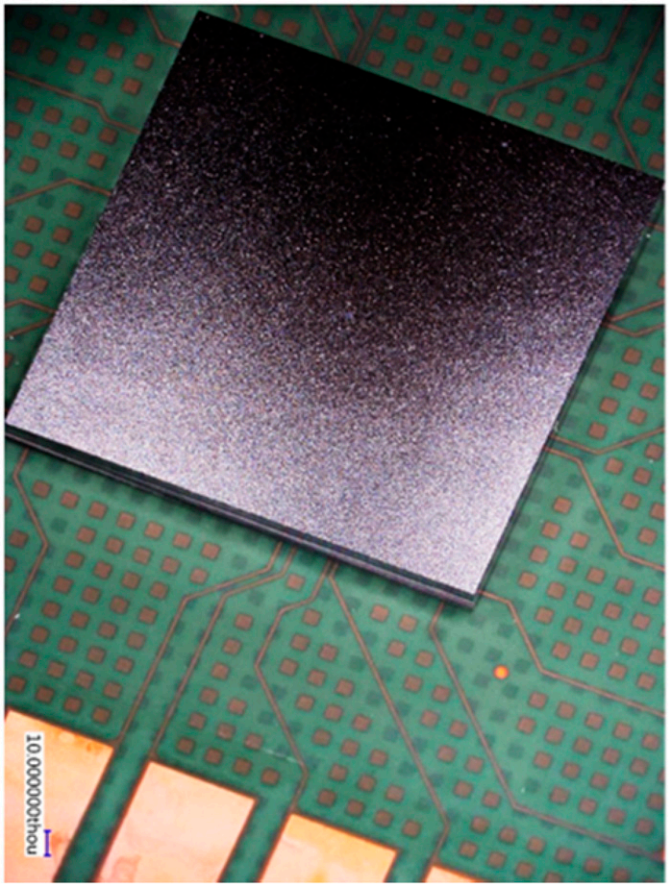

Fig. 7. Copper pillar assembly before cross sectional analysis.

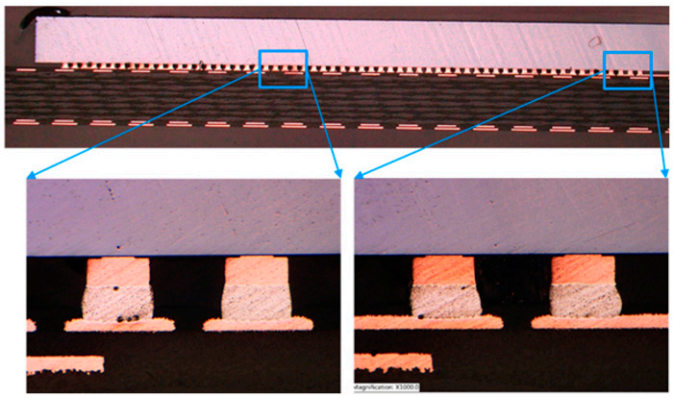

Fig. 8. Cross-sectional analysis of 150-μm pitch solder on pad package.

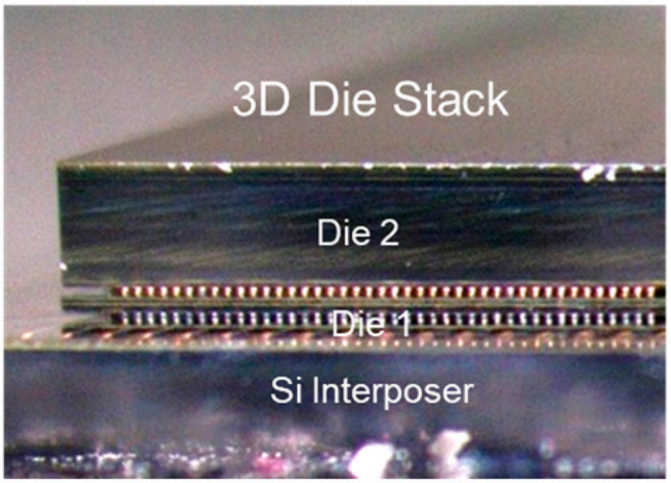

Fig. 9. 2.5D/3D Copper pillar assembly based on mass reflow.

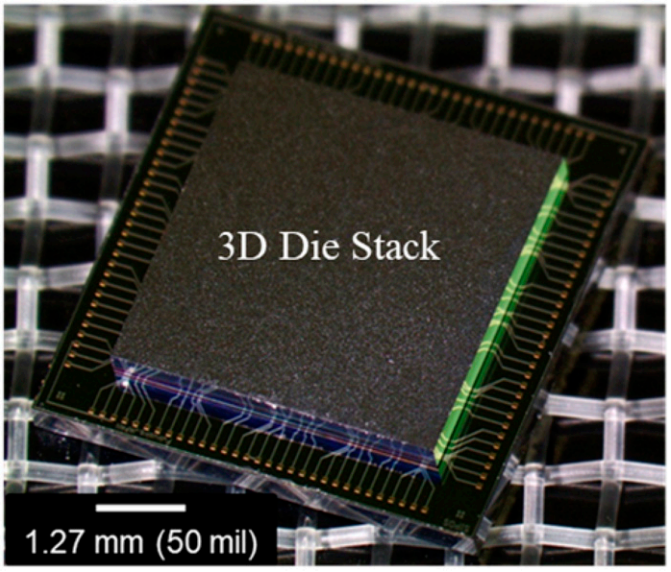

Fig. 10. 2.5D/3D Copper pillar assembly based on TCB.

encapsulates air, leaving a void, negatively affecting package reliability.

The first step to mitigating the risk of voiding was to determine which flux was compatible with each type of underfill. As mentioned earlier, utilizing flux and underfill that are compatible with each other is essential. For this experiment, three types of underfill and three types of flux were used. Underfill A and flux A are the baseline materials, with underfills B and C, and fluxes B and C being new materials. Each flux was dropped onto a bare glass substrate, with a drop of underfill on top of it. Each pairing was cured in an oven based on the underfill manufacturer's recommendations. Results are seen in Fig. 11, and were based on visual inspections. Although other flux-underfill pairings had pitting, or undesirable visual anomalies, underfill A-flux C and underfill B-flux C both showed the best results based on visual inspections. Because of these results, flux C is what was used when attaching the copper pillar die to the interposers for the underfill study, as shown in section III.B.

B. Underfill Design of Experiments Study

Since underfill will help to lessen the impacts of coefficient of thermal expansion (CTE) mismatch between the copper pillar and adjacent metals, deciding on an underfill will be key for the assembly's reliability, as it directly impacts interconnect robustness. Building upon the results of the flux-underfill capability study in section III.A, the underfill DOE (design of experiments) was ready to begin.

A DOE was set up to characterize the different factors affecting underfill, and to ultimately decide which underfill would be used on the GaN reliability test vehicles, used in section IV. The three factors that were varied were cleaning method (no clean, cleaning method A, and cleaning method B), part feature size (80-µm pitch copper pillar, 150-µm pitch copper pillar, or 150-µm solder ball), and an underfill material (underfill A or underfill B). Based on the results in Fig. 11 only flux C was utilized. The die and interposers used here were COTS parts with full area interconnects.

After the DOE was executed, C-SAM (C-mode scanning acoustic microscopy) images were taken to identify and detect voids in the underfill, to determine which combination of cleaning method, feature size, and underfill yielded the best results. In C-SAM images, light gray indicates a void in the underfill, whereas darker gray indicates coverage. Based on the C-SAM data in Fig. 12, underfill B worked best with the 150-µm pitch copper pillar parts, with no cleaning. However, for 80-µm pitch copper pillar parts, there is still more work to be done, which could potentially indicate that the selected underfill or cleaning method was not sufficient to clean the flux residue from the smaller gaps in the assembly.

One accidental outcome of this experiment was seeing how pressure curing both underfill A and underfill B seemed to yield less voids than a regular cure with no pressure, as seen in Fig. 13. As the sample size was not statistically significant, future experiments are planned to better understand the effect of pressure on both underfills, but initial results are very promising.

Ultrathin Monolithic Microwave Integrated Circuit Gallium Nitride Copper Pillar Assembly Qualifications

This section describes the culmination of this project, and overall point, which was to understand how the assembly process and selected materials affected overall package reliability.

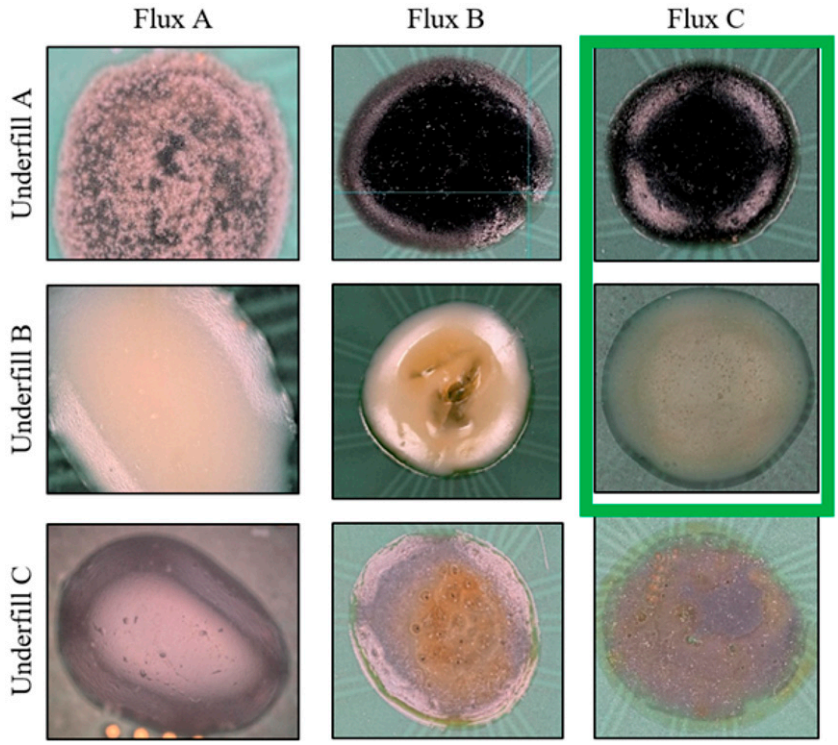

Fig. 11. Underfill flux capability study for Copper Pillar Flip Chip.

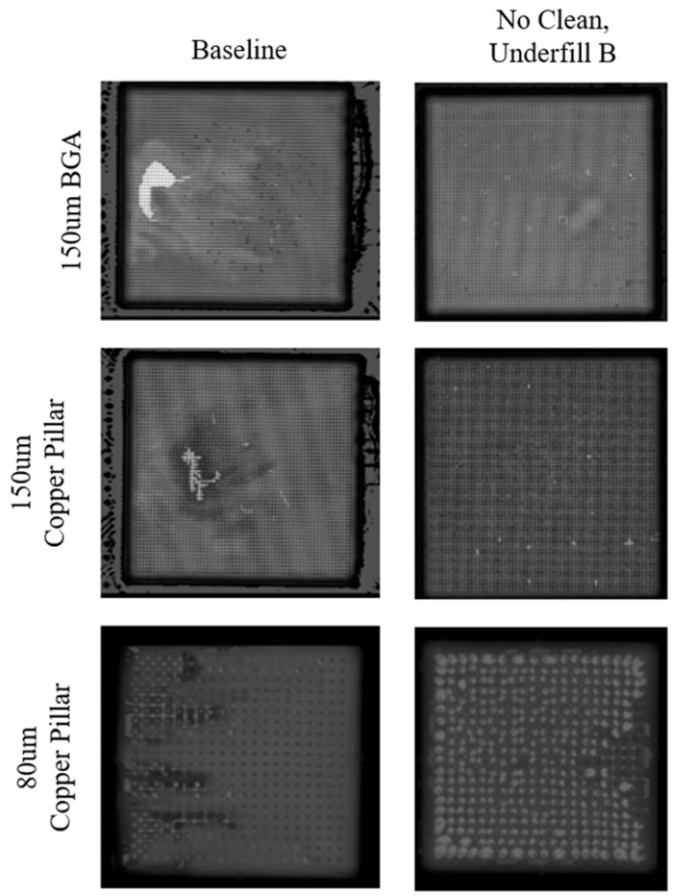

Fig. 12. Underfill DOE results.

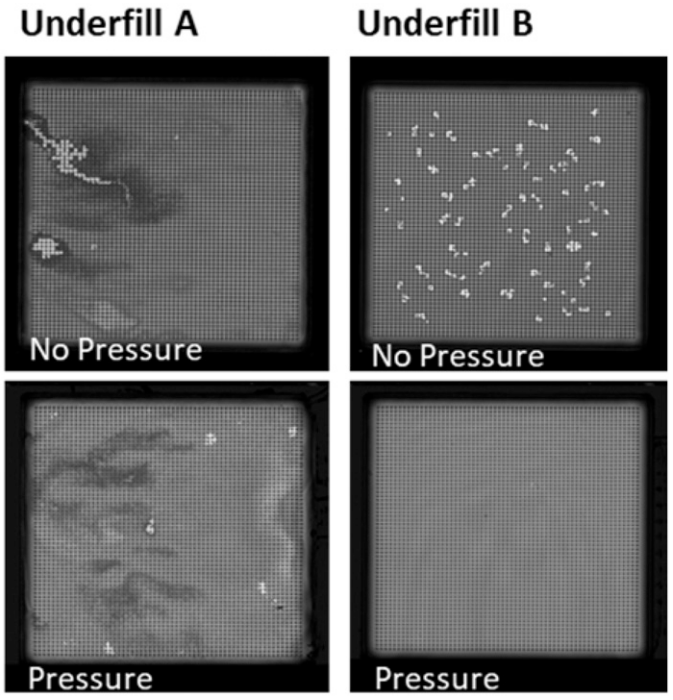

Fig. 13. Pressure curing of underfill shows less or no voids.

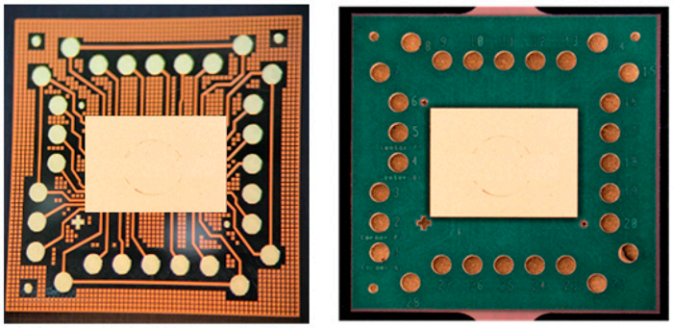

Fig. 14. MMIC GaN Copper pillar assembly on silicon and organic interposer.

To qualify the copper pillar MMIC GaN die assembly process, two different types of test vehicles were used, as seen in Fig. 14. Both assemblies used the same GaN die, which had a 150-µm pitch copper pillar with a pure tin solder cap. However, two different types of interposers were used, an organic and a silicon interposer, with ENIG pad finishes on both.

To further increase manufacturability, future iterations of this project were built using the die to panel level assemblies, as seen in Fig. 15. Twenty packages could be built and tested at a time, greatly reducing the amount of manufacturing time needed, when compared with 20 discrete packages.

Of note, one of the essential factors influencing the robustness of the assembly process is the copper pillar coplanarity. Incoming die was measured for coplanarity, and was found to be well within the requirement, which is less than ± 5 µm, allowing the experiment to move forward.

Now that the optimal assembly parameters and materials were identified, the reliability test vehicles were ready to be built. As seen in section III.B, once parts were underfilled, they were C-SAMed to analyze for underfill voiding. This way, any failures could be traced back to gaps in the underfill. Luckily, because of the rigorous underfill DOE completed in section III.B, which utilized components with a much denser copper pillar array, little to no voids were detected for all test vehicles, indicating that the selected process parameters were acceptable.

Once all parts were built, reliability testing commenced, in the form of temperature cycling and UHAST testing. The failure analysis of these parts are ongoing, including cross sections and x-rays, and will be reported in future work.

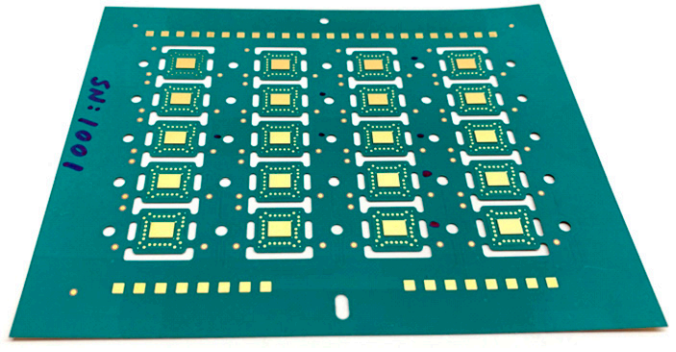

Fig. 15. Organic panel level assembly.

A. Temperature Cycling

Based on reliability document JEDS22-A104, condition B, parts were temperature cycled from −55°C to 125°C for 700 required cycles. Parts were removed from the chamber every 100 cycles for electrical measurements along the daisy chain. Using the organic interposer with ENIG pads as a baseline, the organic interposer samples with solder applied to the pads saw less fall out. The silicon interposer with the ENIG pads saw more fall out when compared with the organic interposer with ENIG pads. Summary seen below in **3.**

B. Unbiased Highly Accelerated Temperature/Humidity Stress Test

For UHAST, parts were again subjected to preconditioning, which consisted of three passes through a reflow oven, and a bakeout at 30°C/60% humidity for 192 h. UHAST was performed afterward at 130C/85% relative humidity (RH) for 96 h, based on JESD22-A110. None of the samples on either interposer failed UHAST testing, as seen in Table IV.

Summary and Conclusion

In this work, assembly of ultrathin MMIC GaN fine-pitch copper pillar flip chip assembly on high-density interposers was successfully demonstrated. Using a 150-µm pitch copper pillar flip chip, the assembly processes for both organic and silicon interposers were evaluated, both with an ENIG pad finish. For the 2D/2.5D assembly process development, a standard in-house pick and place tool was used, followed by mass solder reflow, finished with an underfill for reliability test. The interconnect robustness was determined by die pull strengths and cross sections. Complete reliability and qualification test data on GaN copper pillar flip chip 2D assemblies was completed, including 700 temperature cycles and UHAST testing. Based on reliability data, more failures occurred on the silicon assemblies than the organic assemblies, prompting an ongoing root cause investigation. Based on failure analysis data, modifications will be made to the assembly process and these qualifications tests will be repeated. In the future, full qualification data of solder on pad GaN copper pillar assemblies with failure analysis will be published.

Advanced packaging is a critical enabler for next-gen electronics. Fine-pitch interconnects and 2/2.5D/3D assembly are the keys for high-density packaging. Legacy ceramic, chip/wire packages are being phased out in favor of 2D flip chip and 2.5/3D advanced packaging. Priorities for aerospace and defense versus commercial, including truly heterogeneous integration—much more than just silicon, stable supply chain over long production durations (decades), as well as reliability, quality, security, and stability throughout the packaging ecosystem and lifecycle are all important.

References

[1] W.-W. Liu, "Bumping co-planarity collocation for different UBM size by geometry integration," Proceedings of the 52nd International Microelectronic and Packaging Society, IMAPS, Boston, MA, 2019.

[2] C.-S. Chen, C.-D. Suo, J.-M. Jao, K.-C. Yang, and F.-L. Chien, "Method of fabricating solder bumps with high co-planarity for flip-chip application," US Patent No. 6348401 B1, 2002.

[3] C.W. Ju, S.J. Kim, K.H. Pack, and H.T. Lee, "The effect of via size on fine pitch and high density solder bumps for wafer level packaging," Proceedings of the IEEE Electronic Components and Technology Conference, 2002.

[4] R.A. Bong, "Study to lower copper pillar flip-chip failure rate," Proceedings of the 52nd International Microelectronic and Packaging Society, IMAPS, Boston, MA, 2019.

[5] N.A. Islam, "Fine pitch copper pillar assembly challenges for advanced flip chip package," Proceedings of the International Wafer-Level Packaging Conference 2017, San Jose, CA, 2017.

[6] L.A. Fu, "Copper pillar bump development for 7nm Chip package interaction (CPI) technology," Proceedings of the 52nd International Microelectronic and Packaging Society, IMAPS, Boston, MA, 2019.