# $40~\mu m$ Ag/Au Flip-Chip Joints by Solid-State Bonding at $200^{\circ} C$

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Abstract—In this research, 40 µm silver/gold (Ag/Au) composite flip-chip interconnect joints between silicon (Si) chips and copper (Cu) substrates were demonstrated. The bonding was achieved by a solid-state process at a low temperature of 200°C for 5 min with the pressure applied at 250–400 psi (1.7–2.7 MPa), corresponding to 0.22-0.35 g of force per joint. To begin with, an array of 50  $\times$  50 30  $\mu$ m Ag/10  $\mu$ m Au columns with 40  $\mu$ m in diameter and 100 µm in pitch was fabricated by photolithographic and electroplating processes on silicon (Si) chips which were first coated with chromium (Cr) and Au films. The columns on the chip were then bonded to a Cu substrate by solid-state bonding. Cross-sectional scanning electron microscopy (SEM) images show that the exposed Ag/Au columns were well bonded to the Cu substrate. No joint breakage was observed despite the large coefficient of thermal expansion (CTE) mismatch between Si and Cu. A pull test was conducted. The breaking force and fracture strength are 6.5-7.3 kg and 2,940-3,310 psi (20.2-22.8 MPa), respectively. The breaking force is 2.5× of the criterion specified in MIL-STD-883E. Fracture modes were examined. Three modes were classified by fracture interfaces as Si-glue, Si/Cr/Au/Ag, and Au-Cu bonding interface. Of all joints evaluated, 27% of them break on the Au-Cu substrate bonding interface. Accordingly, the bonding interface is least likely to break among interfaces of the joint structure.

Keywords—Bonding, electronic packaging, flip-chip interconnect, flip-chip joints, gold, silver, solid-state bonding

# Introduction

Plip-chip interconnect is a configuration where the periphery of chip surface is fabricated with bumps that are bonded to the package substrate. It can achieve high input/output counts per periphery. Flip-chip joints have short interconnect distance, thus allowing low inductance and short signal delay [1]. Although wire bonding is still being used in about 70% of assembled packages [2], it is clear that flip-chip is the technology of choice for large-scale integrated circuits (ICs) that require high input/output (I/O) density and high operating frequency. As transistors on IC chips continue to shrink, the diameter of flip-chip joints has to scale down to cope with increased I/O density. According to the international technology road map for semiconductors (ITRS), the pitch

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in the flip-chip array for consumer and mobile products is projected to be 100  $\mu m$  by 2016 [2]. Thus, the joint diameter has to shrink to 50  $\mu m$ . There are two major challenges, the drastic increase in shear strain and the increase of electrical resistance of the joints.

At present, nearly all flip-chip joints in production are made of Tin (Sn)-based leaded or lead (Pb)-free solders [3-8]. The solder joints go through a molten state during the soldering process. The aspect ratio of height to diameter of the joint is thus constrained to about 0.7. As the joint diameter shrinks, the height is also reduced. However, the intermetallic compound (IMC) thickness does not scale with the joint height. As a result, the solder thickness of the joint decreases at a rate faster than the reduction of the joint height. Since there is very little IMC deformation compared to solder, the shear strain on the solder section of the joint increases at a rate faster than the rate of joint shrinkage. The shear strain is caused by CTE mismatch between the Si chip and the package substrate. As joints scale down, the electrical resistance of the joint increases. The resistance is given by  $R = 4\rho(h/\phi)/\phi$ , where  $\rho$  is the electrical resistivity of the joint material, h is the joint height, and  $\varphi$  is the joint diameter. For the same aspect ratio  $h/\varphi$ , R is inversely proportional to φ. To surmount these challenges, we looked into Ag as the joint material because it has the highest electrical conductivity and thermal conductivity among metals. The electrical resistivity of Sn-based Pb-free solders ranges from 0.12-0.14  $\mu\Omega$ m while the electrical resistivity of Ag is 0.0163  $\mu\Omega$ -m. By changing from Pb-free solders to Ag, the electrical resistance of a joint is reduced by a factor of 7.4-8.6 [9]. In a previous project, Si chips fabricated with  $50 \times 50$  Ag columns with 40  $\mu m$  in diameter and 100  $\mu m$ in pitch were bonded to Cu substrates using a solid-state process at 260°C with 680 psi pressure [10]. The force needed per joint is only 0.6 g (0.021 oz). No molten phase was involved and no IMC layer exists. Ag is also ductile, with a yield strength lower than that of Sn3.5Ag eutectic by a factor of 2.2 [11].

In this research, we extended the joint material from pure Ag to Ag/Au composite. For pure Ag joints, the bonding interface is Ag-Cu. Using Ag/Au columns, the bonding interface turns to Au-Cu. Since Au is very ductile and does not oxidize, Au-Cu bonding can be achieved at lower temperature and lower pressure compared with Ag-Cu bonding. In what follows, we report the experiment design and procedures of bonding flip-chip Ag/Au columns fabricated on

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Si chips to Cu substrates. Experimental results are presented and discussed. A short summary is then given.

## EXPERIMENT DESIGN AND PROCEDURES

Fig. 1 illustrates the process flow of fabricating Ag/Au flip-chip joints between Si chips and Cu substrates using solid-state bonding. Two-inch Si wafers are deposited with 30 nm Cr and 100 nm Au thin films by E-beam evaporation in high vacuum,  $1\times 10^{-5}$  torr. The Cr is adhesion layer and Au is seed layer for electroplating. Photoresist of 40  $\mu m$  in thickness is coated. The photoresist, KMPR $^{\text{(B)}}$ , is epoxy based and has high aspect ratio capability. Using photolithographic process, array of 50  $\times$  50 cavities 40  $\mu m$  in diameter and 100  $\mu m$  in pitch is produced on the photoresist. Oxygen (O2) plasma cleaning process is applied to remove photoresist residue on the bottom of the cavities.

Ag of 30  $\mu m$  in thickness is electroplated in the cavities, followed by 10  $\mu m$  Au. The Ag plating bath is a mild alkaline plating solution at pH of 10.5 containing potassium hydroxide (KOH) and sulfamic acid (H<sub>3</sub>NSO<sub>3</sub>). Au plating solution consists of sodium sulfite and sodium gold sulfite. The Ag plating is conducted with current density 13 mA/cm<sup>2</sup> at room temperature and Au plating with current density 2 mA/cm<sup>2</sup>

at 50°C. Current, voltage, temperature, and time are monitored closely during the plating processes. The photoresist is removed by its stripper at  $80^{\circ}$ C. After cleaning, 6 mm  $\times$  6 mm chips are diced from the 2-in wafers and ready for flipchip solid-state bonding experiments. The bonding substrate selected is 99.9% pure Cu with thickness of 0.88 mm. The Cu substrate is slightly polished to remove contamination and oxide layers. Cu is chosen to emulate the Cu electrodes and bond pads on package substrates.

To perform solid-state bonding, Si chip with Ag/Au flip-chip columns and Cu substrate are held together with a pressure of 1.7–2.7 MPa (250–400 psi) and heated to 200°C for 5 min. It is done in 0.1 torr vacuum to suppress oxidation [12]. Scanning electron microscopy (SEM) and energy-dispersive x-ray spectroscopy (EDX) are used to study the flip-chip joints of the bonded samples. A pull test is conducted to measure the strength of the flip-chip joints. The fracture modes are evaluated by SEM/EDX.

## EXPERIMENTAL RESULTS AND DISCUSSION

Photoresist with  $50 \times 50$  cavities of 40  $\mu m$  in diameter and 45  $\mu m$  in depth was produced on 6 mm  $\times$  6 mm regions of a Si wafer by photolithographic process. 30  $\mu m$ 

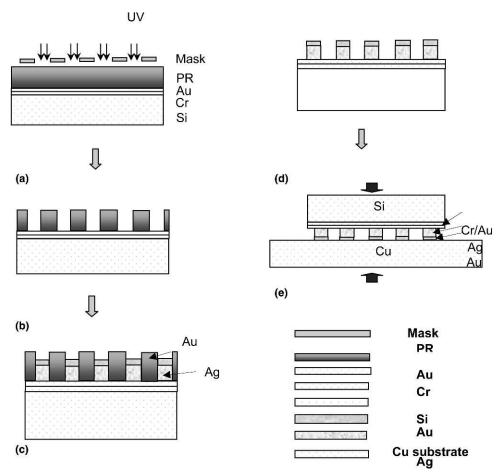


Fig. 1. Process flow of fabricating Ag/Au flip-chip columns on Si chip and bonding to Cu substrate: (a) photoresist coating and UV light exposure, (b) developing, (c) Ag plating followed by Au plating, (d) photoresist removal, and (e) solid-state bonding.

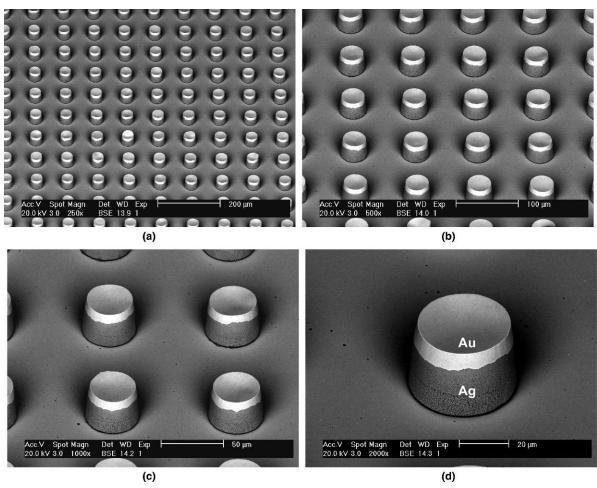


Fig. 2. BSE images at  $45^{\circ}$  view of Ag(30  $\mu$ m)/Au(10  $\mu$ m) columns with 40  $\mu$ m in diameter and 100  $\mu$ m in pitch on Si wafers coated with thin Cr and Au layers at (a)  $250\times$ , (b)  $500\times$ , (c)  $1000\times$ , and (d)  $2000\times$ .

tall Ag was plated in the cavities, followed by 10 µm Au. After stripping the photoresist, the wafer was diced into 6 mm  $\times$  6 mm chips, each having 50  $\times$  50 Ag/Au columns. Fig. 2 exhibits the backscattered electron (BSE) images of the Ag/Au columns with 40 μm in diameter and 100 μm in pitch on Si/Cr/Au at (a) 250×, (b) 500×, (c) 1000×, and (d) 2000×. The images show that the Au surface of the Ag/Au columns is a little concave but very smooth. The grain size of the Au layer is smaller than 30 nm. The sidewalls are straight but a little tapered, smooth, and well defined. The Si chip with Ag/Au columns were flipped over and bonded to a Cu substrate. The pressure applied is 1.7-2.7 MPa (250-400 psi). This corresponds to 0.22-0.35 g of force per joint. The solid-state bonding was carried out at 200°C for 5 min in 0.1 torr vacuum. The 5-min time is constrained by the equipment. In theory, bonding should occur in seconds.

The samples were cut along one complete row, polished, and examined under optical microscope and SEM. Fig. 3 discloses the BSE cross-sectional images of Ag/Au composite flip-chip joints bonded to the Cu substrate with a static pressure of 250 psi (1.7 MPa) at low magnification. The image shows that the Ag/Au columns are well bonded to Cu without any breakage or cracking. The joints sustain the significant

CTE mismatch between Si and Cu. Fig. 4 displays high magnification cross-sectional SEM images of a typical flip-chip joint. Fig. 4a shows the complete joint. It is seen that the Cu substrate was pushed down a little bit by the joint

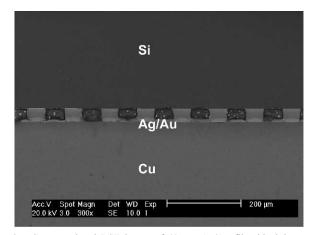


Fig. 3. Cross-sectional BSE image of 40  $\mu$ m Ag/Au flip-chip joints made between Si/Cr(30 nm)/Au(100 nm) and Cu substrate by solid-state bonding at 200°C with static pressure of 250 psi (0.22 g per joint).

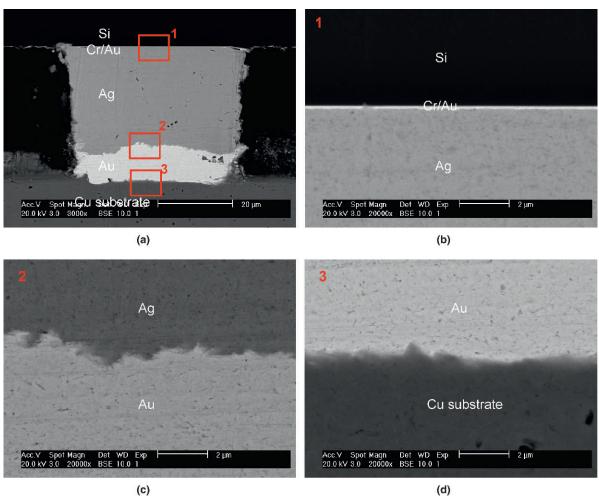


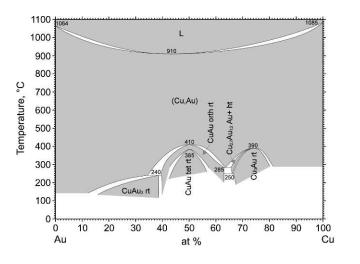
Fig. 4. Cross-sectional BSE images: (a) a typical Ag(30 μm)/Au(10 μm) joint bonded to Cu substrate, (b) Si/Cr/Au/Ag interface where the 100 nm Au layer is visible, (c) Ag/Au interface of the electroplated Ag/Au column, and (d) Au/Cu bonding interface.

because of the pressure applied. The Cu substrate was manufactured by a rolling and annealing process. It is soft, ductile, and easy to deform. The joint height was reduced from 40  $\mu m$  to 35  $\mu m$  due to compression. Fig. 4b shows the Si/Cr/Au/Ag interface where the 100 nm Au layer is highly visible. Fig. 4c displays the Ag/Au interface of an Ag/Au column, which is the electroplating interface. Fig. 4d shows the Au-Cu bonding interface produced by solid-state bonding. It is observed that both Au and Cu deform to achieve intimate contact. The force applied is only 0.22 g per joint.

Our fundamental theory of solid-state bonding is: when the spacing between A atoms and B atoms is brought within atomic distance so that they share electrons, bonding between material A and material B will occur. To share electrons, the A atoms and B atoms must be within atomic distance so that they see each other. However, seeing each other does not guarantee attraction and sharing electrons. That is why diffusion of the A and B atoms alone does not guarantee bonding. However, diffusion of materials A and B does not affect the bonding ability so far as the A atoms and B atoms continue to share electrons after diffusion. The ability of material A and material B to share electrons depends on their electronic configurations. The theory was seldom inves-

tigated and is beyond the scope of this paper. In this project, the ability of Au atoms and Cu atoms to share electrons is determined by the experimental bonding results.

The diffusion process may be part of the bonding mechanism, although it is not required for achieving bonding, as elaborated above. Fig. 5 displays the Au-Cu phase diagram [13]. It is seen that Au and Cu are completely miscible in the solid state. Au and Cu can form a substitutional solid solution. According to the Hume-Rothery rule [14-17], several conditions must be met for forming substitutional solid solutions. First, the atomic radii of solute and solvent atoms must differ no more than 15%. Second, the crystal structures of solute and solvent must match. Third, the solvent and solute should have the same valence. Last, the solute and solvent should have similar electronegativity. The radii of Au and Cu are 0.14 nm and 0.13 nm, respectively, differing by 11%. Au and Cu also have the same FCC structure, the same valence, and close electronegativity, that is, Au: 2.54 and Cu: 1.9. Therefore, Au and Cu are able to form a substitutional solid solution at the Au-Cu bonding interface without changing the crystal structure. The interdiffusion of Cu and Au in a Cu/Au film stack at 200°C was previously studied [18]. It was observed that the IMC



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Fig. 5. Au-Cu binary phase diagram [13].

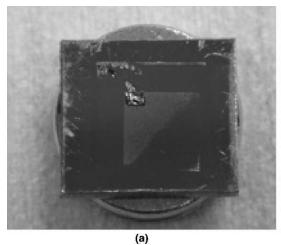
Cu<sub>3</sub>Au began to show up after 45 min of annealing. CuAu<sub>3</sub> was found only after 3 h of annealing. Based on this result, no IMC is expected to form at our bonding conditions of 200°C for 5 min. Our EDX data on the Au-Cu bond line do not detect any IMC formation. The diffusion of Au into Cu was studied by elastic scattering of protons and deuterons [19]. The activation energy (Q) and pre-exponential diffusivity ( $D_o$ ) were 45,750 cal/mol (1.98 eV) and 0.104 cm<sup>2</sup>/s, respectively. Using this data, the diffusion depth in our samples is calculated to be 1.5 × 10<sup>-3</sup> nm, smaller than the radii of Au and Cu atoms. This suggests that diffusion did not occur.

In order to study how surface conditions affect bonding results, Cu substrates with surfaces exposed to air for several days before bonding were used. The results show that none of the  $50 \times 50$  Ag/Au columns on the Si chip was bonded to the Cu substrate. The cause of bonding failure is Cu oxidation. It is clear that fresh and clean bonding surfaces are essential

for successful solid-state bonding. If A atoms and B atoms do not see each other along the bonding interface, they cannot share electrons and consequently bonding will not occur.

A pull test was performed on several bonded samples to evaluate joint strengths and fracture modes. In our pull test fixture, an aluminum pull bar was attached to the Si side of a bonded sample with super glue while the Cu substrate of the sample was fixed and clamped by two stainless steel holders on an optical table. In the testing process, the pull force was increased gradually and steadily, and did not stop until the sample broke. We then investigated the failure mechanism of these tested samples. The results of two representative samples, A and B, are reported. Figs. 6a and 6b are photos of the Cu side of the samples A and B, respectively. For sample A in Fig. 6a, a 0.8 mm × 1 mm piece of Si remains on the Cu substrate. However, a closer look reveals that 50% of the Ag/Au composite joints are still bonded on the Cu. For sample B in Fig. 6b, 80% of the Si chip remains bonded to the Cu substrate. The measured breaking force for samples A and B is 7.32 kg and 6.50 kg, respectively. The average strength for flip-chip joints is 22.8 MPa (3,310 psi) and 20.2 MPa (2,940 psi), respectively. The average strength is calculated by dividing the breaking force expressed in Newtons by the total number of joints (2,500) and the cross-sectional area of a joint. According to MIL-STD-883E, Method 2031.1, the failure criterion of the flip-chip pull-off test is 500 kg/in<sup>2</sup> [20]. This corresponds to a force of 2.5 kg for our samples. Thus, the breaking force of our samples is about  $2.5 \times$  of the military requirement. The breaking force, the fracture strength, and fracture modes are presented in Table I.

Fracture modes were further studied by SEM/EDX analysis. Three fracture modes were identified as follows. Mode I: breakage between evaporated Cr/Au and electroplated Ag/Au columns. Mode II: breakage at the bonding interface between Au and Cu substrate. Mode III: breakage on the glue-Si interface. These fracture modes are identified by fracture interfaces with SEM/EDX observations and classified by the fracture root causes. For clarity, a sketch was prepared to



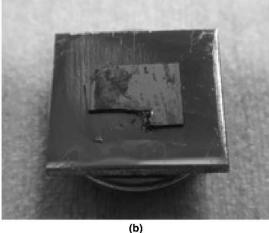


Fig. 6. Photos of samples after the Si chip was pulled off in pull test: (a) sample A, and (b) sample B. The sample consists of a 6 mm  $\times$  6 mm Si chip bonded to Cu substrate by  $50 \times 50$  Ag/Au composite joints using a solid-state bonding process at  $200^{\circ}$ C.

Table I
Fracture Forces, Fracture Strengths, and Fracture Modes of Samples Observed
After Pull Test

Samples	Breaking force (kg)	Fracture strength MPa (Psi)	Fracture modes
A	7.30	22.8 (3,310)	Mixed mode:  Mode I: 45%, breakage between evaporated Cr/Au and Ag/Au columns.  Mode II: 50%, breakage on the bonding interface between Au and Cu substrate.  Mode III: 5%, breakage on glue-Si interface Mixed mode: Mode I: 16% Mode II: 4% Mode III: 80%
В	6.50	20.2 (2,940)	

illustrate these fracture modes, as shown in Fig. 7. Figs. 8a-f are the BSE images of sample A after the pull test. Figs. 8a and 8b are low magnification images of the Cu substrate. Fifty percent of the flip-chip joints are still bonded on the Cu substrate. In this region, marked I, the Si chip broke off the joints at the interface between the Cr/Au and Ag/Au columns. This break belongs to fracture mode I. Figs. 8c and 8d exhibit the fracture interfaces on the Cu side and on the Si side, respectively. Fig. 8c shows four representative Ag/Au columns remaining on the Cu substrate. The majority of fracture interfaces are between the Au of the Cr/Au layer and the Ag section of the Ag/Au column, designated as mode Ia. This is the electroplating interface when Ag sections of Ag/Au columns were plated on the Si chip coated with Cr/Au. There are several circular Cr/Au regions remaining on the columns. For these regions, the fracture interface is between Cr of the

Cr/Au layer and Si, designated as mode Ib. Fig. 8d displays the broken-off marks of the four columns on the Si chip that was pulled off. Most of the marks are on Cr/Au except for several circular regions where Cr/Au was torn off and the underlying Si was seen. For mode I fracture, the bonding interface is stronger than the electroplating interface. On the region marked II in Fig. 8a, the flip-chip joints broke off the Cu substrate and stayed on the Si chip. This break belongs to fracture mode II. Fig. 8e shows the broke-off mark on the Cu side. Most fractures incurred on the bonding interface between electroplated Au and the Cu substrate. Some Au residue is observed, indicating fracture inside the Au section of the Ag/Au column. Fig. 8f is a top view image of a joint on the Si side, exhibiting annulus geometry. The outer ring is the top view projection of the sidewall of the Ag/Au column. The sidewall shows up like a ring because of its tapered profile. The center circular region is where the joint broke. Some mountain-like Cu trace is seen, suggesting fracture inside the Cu substrate. We wish to point out that Figs. 8e and 8f are not from the same joint. In reality, it is very difficult to find a match pair of broke-off mark on the Cu and a column on the Si chip. For sample B shown in Fig. 6(b), the superglue that bonded the pull bar to the sample broke during the test. Si piece of 2 mm × 4 mm stayed on the pull bar. 80% of the Si chip remains bonded on the Cu substrate, exhibiting mode III fracture. On this 2 mm × 4 mm Si piece, mode I and II fractures were observed, of which 80% is mode I and 20% is mode II.

Of interest to observe is that no flip-chip joints broke on the Ag/Au interface of the electroplated Ag/Au columns. The electroplating Ag/Au interface of Ag/Au columns is stronger than the Au/Ag interface between Cr/Au on Si and the Ag section of the Ag/Au columns. The percentages of mode I, mode II, and mode III fractures are 31%, 27%, and 42%, respectively. Mode II fracture, breakage on the

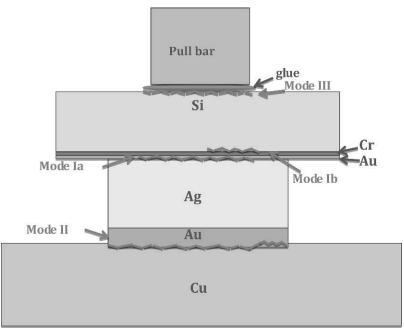


Fig. 7. Illustration of fracture modes.

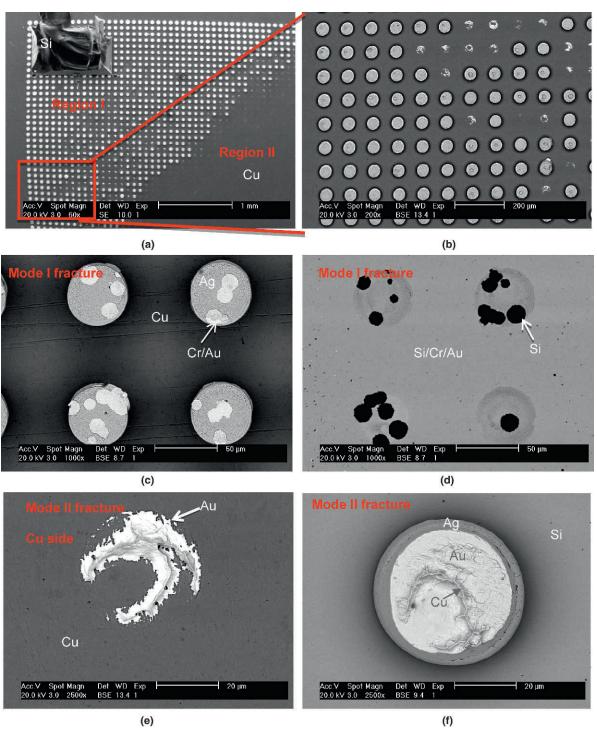


Fig. 8. BSE images of sample A shown in Fig. 6(a): (a) and (b) low magnification images on Cu side, (c) mode I fracture on Cu side, (d) mode I fracture Si side, (e) mode II fracture on Cu side, (f) mode II fracture on Si side. Mode I fracture: breakage between evaporated Cr/Au and Ag/Au column. Mode II fracture: breakage at the bonding interface between Au and Cu substrate.

solid-state bonding interface, has the lowest percentage, and thus is least likely to incur in pull test.

# SUMMARY

 $40~\mu m$  Ag/Au composite flip-chip joints were made between Si chips and Cu substrates using solid-state bonding at  $200^{\circ}C$ 

with a static pressure of 250–400 psi (1.7–2.7 MPa). Within a 6 mm  $\times$  6 mm Si chip, 50  $\times$  50 flip-chip joints bond and connect the chip to the Cu substrate. The pitch of the joints is 100  $\mu m$ . Each joint starts as a column consisting 30  $\mu m$  Ag section and 10  $\mu m$  Au section on the Si chip coated with Cr and Au. During bonding, the Au section of the column was bonded to the Cu substrate. The resulting joint height

is 5 µm less than the column height because of compression. Cross-sectional SEM images show that Ag/Au flip-chip joints were well bonded to the Cu substrate without voids or breakage. A pull test was performed. The breaking force and fracture strength are 6.5-7.3 kg and 20.2-22.8 MPa (2,940-3,310 psi), respectively. The breaking force is  $2.5\times$ the criterion in MIL-STD-883E. The temperature needed for this new process is only 200°C, which is 60°C lower than typical reflow temperature of Pb-free solders. The bonding force per joint has decreased to 0.22-0.35 g. Despite the large CTE mismatch between Si and Cu, no joint breakage was observed. No cracking or damage was observed on Si chips. There is no molten phase during the bonding process. Neither flux nor underfill was used. Compared with solder flip-chip joints, the immediate advantage of this new process is the reduction of electrical resistance of the joints of the same size by a factor of 7.

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