Journal of Microelectronics and Electronic Packaging (2015) **12**, 67-71

ISSN: 1551-4897

Enabling Manufacturable 3-D Technology and Ecosystems Using a 28-nm FPGA With Stacked Silicon Interconnect Technology

Woon-Seong Kwon,[1,*] Myongseob Kim,[1] Jonathan Chang,[1] Suresh Ramalingam,[1] Liam Madden,[1] Genie Tsai,[2] Stephen Tseng,[2] J.Y. Lai,[2] Terren Lu,[2] and Steve Chiu[2]

***Abstract*—Technology challenges and solutions in the development and manufacturing of stacked silicon interconnect (SSI) technology have been investigated with the established foundry and outsourced semiconductor assembly and test ecosystem. Key enabling technologies, such as through-silicon-via processing, interposer backside manufacturing yield enhancement, new stacking technology, interposer warpage control, and microbump processes and joining, which are the building blocks for SSI technology, were developed. Xilinx's 28-nm field programmable gate array with an SSI technology platform was used to develop and optimize the seamless integration of the processes, structures, and parameters, as well as to evaluate their yield, reliability, and device performance.**

***Keywords*—Interposer, stacked silicon interconnect technology, manufacturing yield, warpage, microjoining**

Introduction

Both through-silicon via (TSV) and stacked die technologies have been gaining traction due to performance and manufacturing issues associated with transistor scaling. 3-D die stacking architecture with TSV offers a unique combination of low power and high bandwidth per watt without increasing the scaling cost significantly. For Xilinx, due to the repetitive and unique structures of its field programmable gate arrays (FPGAs), stacked silicon interconnect (SSI) technology is a perfect fit to provide a high-performance solution to build large, homogeneous logic devices with very high logic cell count, as well as heterogeneous logic die integration [1].

To realize the superior manufacturability and cost-effectiveness of SSI technology, the full fabrication sequence requires seamless integration and optimization from perspectives of both TSV/back-end-of-line (BEoL) metal stacks in foundry wafer processing and mid-end/back-end processes in outsourced semiconductor assembly and test (OSAT) wafer/die processing. The entire flow must be optimized to deliver the greatest performance (yield, reliability) for the highest productivity (cost).

Line yield and defect density control are two of the most closely guarded secrets in the manufacturing of SSI technology. Many efforts have been made to enhance line yield in various aspects of particulate control, wafer-edge yield engineering, any process nonuniformities enhancement, surface treatment/modification, and so on. Critical processes were identified and countermeasures implemented to improve overall yield and quality performance.

Another manufacturing challenge is the need for high yielding and highly reliable microjoining metallurgy and bonding technology. In standard copper pillar microbump structure, there is a limited supply of Sn atoms coming from solder capping material. This could cause voiding and cracking symptoms in microjoints, affecting long-term reliability. Moreover, intermetallic compound (IMC) occupies a major volume fraction of the solder joint during the assembly process or after long-term storage at high temperatures [2, 3]. To solve these technical limitations, a copper heavy-doping approach to SnAg solder was invented to prevent the undesirable void formation and intermetallic reaction that can lead to voiding or cracking on the top and bottom interfaces.

In the current Xilinx SSI configuration, four separate 28-nm FPGA slices were connected to each other through a 65-nm, passive TSV silicon interposer. The 28-nm FPGAs dies having more than 50,000 microbumps are stitched together through the silicon interposer to provide device-scale interconnect hierarchy. Having more than 200,000 microbumps and a very large FPGA/interposer die size results in any particulate contamination or defect control having an ever-increasing impact on microjoining yields. One part of yield loss in microjoining can be attributed to random defects, which involve contamination by fall-on particles, stubborn temporary glue, organics, and any other undesirable contaminants that result from mid-end and back-end processing in OSAT. The other main contributors to yield loss are systematic defects, which include design margin (bump coplanarity in isolated and dense area) and process variation (warpage and carrier glue). The innovative reconfigurable (chip-on-wafer [CoW]) technology based on chip-on-chip (CoC) stacking, using releasable self-adhesive layers, were developed and implemented to overcome such manufacturing limitations and roadblocks. Moreover, this

The manuscript was received on November 12, 2014; revision received on February 4, 2015; accepted on February 4, 2015

The original version of this paper was presented at the IMAPS 46th International Symposium on Microelectronics (IMAPS 2013), September 30-October 3, 2013, Orlando, Florida.

[1]Xilinx Inc, 2100 Logic Drive, San Jose, California

[2]Siliconware Precision Industries Co Ltd, No.153, Sec. 3, Chung-Shan Rd, Tantzu, Taichung 42756, Taiwan, China

*Corresponding author; email: woon-seong.kwon@xilinx.com

doi:10.4071/imaps.453

technology enables the wafer-scale cleaning technology and automated optical inspection (AOI) for robust defect control and further yield improvement.

In this paper, technical challenges and solutions in the manufacturing of SSI technology have been investigated with the established foundry and OSAT ecosystem.

Package Description

The high-performance FPGA die is a four-slice, 28-nm chip mounted on a 100-μm thick silicon interposer, 25 mm × 31 mm, with hundreds of thousands of microbumps at a 45-μm pitch. The TSV interposer is assembled on a 45 mm × 45 mm organic package with 180-μm pitch C4 bumps. The package is monitored through multiple chains consisting of microbumps, C4 bumps, and TSV to check interconnect integrity and reliability testing. Fig. 1 shows the cross-sectional pictures with key physical features of this SSI package.

Key Enabling Technologies

A. Interposer OSAT Manufacturing Yield Enhancement

Quite a few factors can cause considerable yield loss in foundry TSV manufacturing and OSAT mid-end processes, factors that include the different definition of critical killer defects from existing fabrication/OSAT integration, glue residues/contamination at bevel and edge areas due to plasma inhomogeneity toward the wafer edge, wafer bow due to film stress, nonuniformities in etch profiles and post-chemical mechanical polishing (CMP) film thickness, and plasma- or handling-induced mechanical damage at the thin wafer edge. Considerable efforts have been made to enhance line yield and interposer die yield in various aspects of particulate control, wafer-edge yield engineering, any process nonuniformities enhancement, surface treatment/modification, thin-wafer handling damage, and so on. From a process integration perspective, statistical process control, which is extremely useful in process control and optimization, is also applied for yield improvement in mid-end-of-line (MEoL) modules. This part of our study presents the MEoL yield improvement effort that utilizes an engineering collaboration dedicated to improving line yield and die yield. Several case studies are presented to illustrate the efforts and substantial yield enhancement outcome.

The front of a TSV interposer wafer was temporarily glued with to a carrier wafer. Bonding-glue total-thickness variation, edge bead amount, glue coverage for trimmed bevel, and bonding void were optimized for securing line yield and improving downstream process integration. TSV interposer wafers were ground with successively finer-grade abrasives (Z1/Z2/Z3) to make them thinner, enabling them to have a certain amount of silicon over-burden on top of the TSV copper bottom. The postgrind surface property of Si is critical for particulate control during subsequent process steps. That is, the hydrophobic Si surface tends to attract water droplets that contain organic materials. When the water droplet is removed from the hydrophobic surface during the wafer drying process, the water marks remain and organic residues form. This watermark defect is invisible right after the grinding step and becomes visible after the reactive-ion etching (RIE) step. This is a crucial defect mode for subsequent RIE etchback and final known-good-die (KGD) electrical testing. It is necessary to remove the watermark and contaminants from the ground Si surface.

As described in Fig. 2, both Si CMP optimization and postgrind surface clean could result in a defect-free surface. Controlling the wettability of the grind surface and post-CMP cleaning method played an important role in the removal of particles and water marks from the Si surface. In other words, changing the grind surface from a hydrophobic to hydrophilic surface made it less likely that particles adhered during subsequent steps.

During the MEoL manufacturing process, several defects (e.g., carrier wafer damages and contamination) caused by temporary glue particulate, dry etching, film deposition, and wafer handling were likely to occur at the wafer edge. These edge defects and particles are easily transferred to the polished Si surface during subsequent process steps (e.g., RIE or CVD or wafer transport steps). Fig. 3 depicts the representative defect images after the RIE etchback step. Foreign material showing a carbon peak (Fig. 3a) could come from a postetch defect from either edge glue particulate or an environmental random defect. An etching byproduct showing sulfide and fluorine peaks (Fig. 3b) is the in-process particle from the etching process. A hard-mask defect showing carbon and silicon peaks (Fig. 3c) could be originated from a pre-etch defect that acted

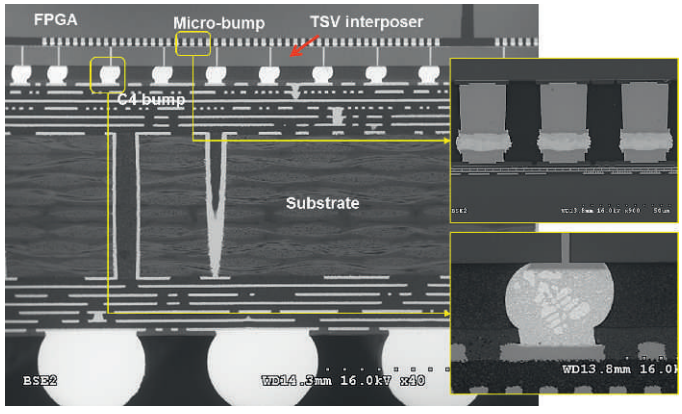


Fig. 1. Cross-sectional image showing the physical features of the Xilinx SSI technology device (Courtesy of Xilinx, United Microelectronics Corporation [UMC], Siliconware [SPIL]).

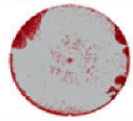
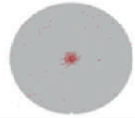
Method	CMP 1 +CLN1	CMP 2 +CLN1	CMP 2 +CLN2
Surface	Hydrophobic	Hydrophilic	Hydrophilic
Defect map			
Defects	Watermark, chemical residue (a)	Watermark (b)	No defect (100%yield) (b)

Fig. 2. Defect maps: (a) before grind-surface optimization and (b) after grind-surface optimization with polishing and cleaning steps.

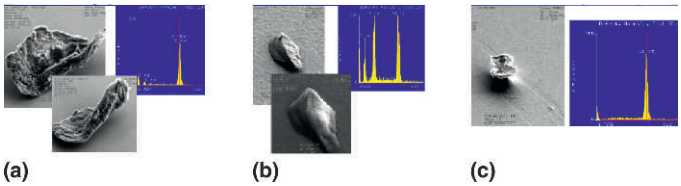


Fig. 3. Defect maps: (a) foreign material, (b) SF6 byproduct, and (c) hard-mask defect due to preexisting particles.

as a Si hard mask. Thus, the wafer edge or bevel area was a primary source of yield-lowering defects. Therefore, the cleanness at the wafer edge (top and bevel) is crucial for yield enhancement.

In this development, the effectiveness of a special wafer-edge-bevel cleaning (wet plus dry) technique was investigated as a method to reduce defect sources from the wafer edge during RIE and CVD steps. To see the impact of bevel cleaning in a single RIE etch step, different bevel cleaning methods prior to the RIE etchback step were evaluated. As described in Fig. 4, the result showed a clear positive effect of bevel cleaning on defect count and die yield. Even minor fall-on particles, shown in Fig. 4c, could be scrubbed away in the next wafer cleaning step, which further continued to achieve defect-free in-line yield.

Plasma etches yield the localized etch rate difference on dissimilar material (Si and SiO_2) interfaces, due to etch radical charging on the oxide surface that causes either footing or notching. It becomes worse with over-recessed TSV tip height (or pillar height), which is more likely to occur at the wafer edge. Fig. 5a displays the worst-case electrical failure scenario, due to an Si footing defect, particularly for the wafer edge.

To enhance TSV tip-height uniformity after the RIE step, the gradient Si etch rate across the wafer was applied to compensate for the nonuniform thickness of incoming wafers, due to carrier bond and lapping steps. Fig. 5b presents FIB/SEM images of the TSV revelation tip with optimized RIE etchback, showing that TSV tip-height variation across the wafer center to edge was evidently uniform and there was little oxide liner loss on top of the exposed TSV tip.

With the aforementioned gradient Si etching technique and localized charge-reduction effort, the TSV tip-height uniformity and Si footing size were substantially improved and final KGD yield was close to 100%, as shown in Fig. 5c.

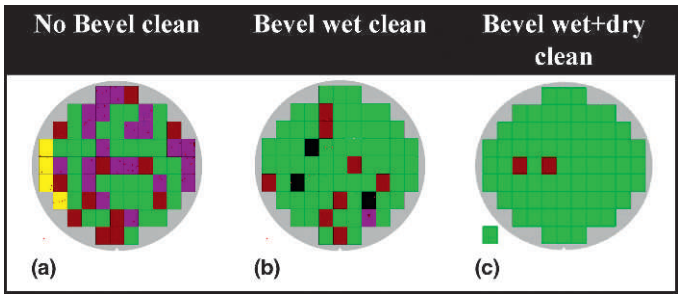


Fig. 4. Representative interposer die AOI yield map after RIE etchback step (a) without bevel engineering effort, (b) with bevel wet cleaning, and (c) with bevel wet plus dry cleaning.

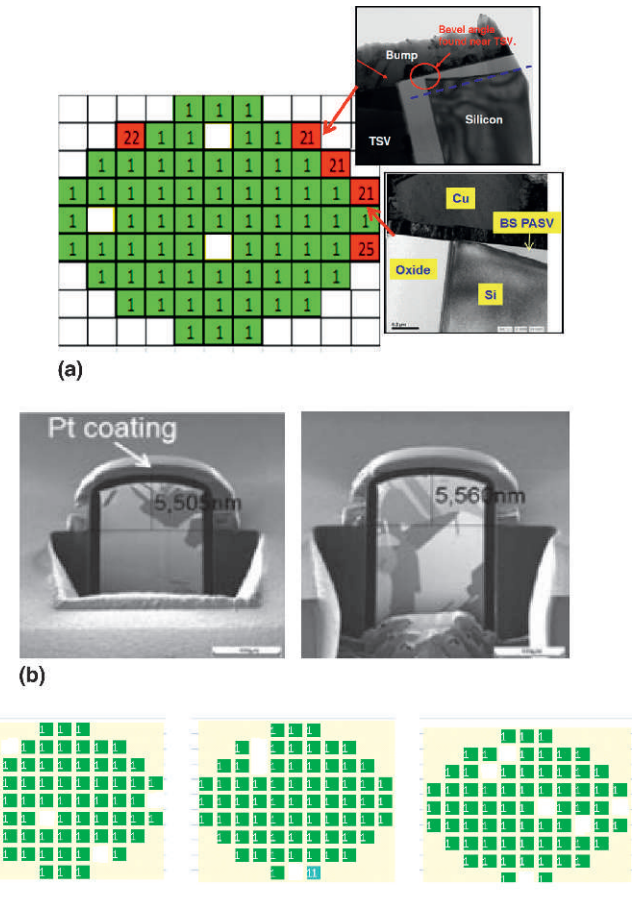


Fig. 5. (a) Interposer KGD failed die (Bin 21/22/25) and its FIB/TEM images of a failed die of a nonoptimized etch process, (b) FIB/SEM images of TSV revelation structure at the wafer edge after RIE etchback, (c) nominal KGD E-test map results using optimized processes (no such bin failed die) (Courtesy of Xilinx, UMC, SPIL).

B. New, Reconfigurable CoW Technology for a Warpage-Immune Stacking Process

During the microjoining process, an interposer die is likely to be susceptible to high-reflow-temperature warpage, and such interposer die warpage leads to inconsistent microjoint formation between a die and an interposer. Several factors could impact the extent of interposer die warpage, including the thickness of the interposer, frontside interconnect copper-metal density, the TSV feature, processing temperature, and asymmetric stresses balance coming from different dielectric stacks on the front and back sides. Unless stresses are balanced, the warpage of a thin, large interposer can be significant and cause die-handling or microjoining issues in bonding. Stresses can be balanced by optimizing film stresses on both sides of the interposer wafer.

Engineering efforts to control the stress balance of both frontside SiN passivation dielectrics and backside isolation dielectrics were made to have minimal warpage at both room temperature and reflow temperature. Fig. 6 shows one of the improvement efforts from an interposer warpage perspective. As shown in Fig. 6, room temperature warpage was substantially improved by about 45%. However, since the frontside

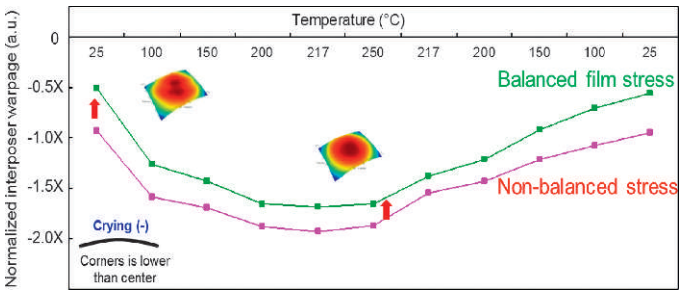


Fig. 6. Normalized warpage change comparison for nonbalanced stress and balanced stress tuning on frontside and backside.

multilayer and high-density interconnect copper metal (65-nm Cu process) influences the entire temperature-dependent global warpage behavior of interposer, it is challenging to meet the warpage requirement for room temperature (die handling) and reflow peak temperature (microjoining), which enable the standard mass reflow joining process for both CoC and chip-on-substrate. Moreover, making the warpage backward by tuning the film stress could give rise to adverse effects on integration.

Meanwhile, the TSV interposer attached directly to an organic substrate is known to suffer from substrate-reflow warpage issues, due to inherent substrate warpage and composite CTE mismatch of the Si/substrate. CoC stacking also has a limitation with regard to the thin-die handling and warpage control in the process of top-die stacking on it. The innovative, reconfigurable CoW technology using a releasable, self-adhesive layer was developed to eliminate inherent interposer warpage, enabling extremely high yields and productivity. Moreover, due to both a large number of microbumps (more than 200,000) and a very large FPGA/interposer die size, any particulate contamination or in-line defect control had an ever-increasing impact on microjoining yields, whether from a random defect or a systematic defect. From a defect-control perspective, this new method also enables the wafer-scale cleaning technology and AOI inspection for robust defect control and yield improvement. Unlike the standard CoW stacking approach, this reconfigurable CoW has no dissimilar die-size constraint of mother/daughter die and scribe lane design limit.

The reconfigurable CoW technology using a releasable, self-adhesive layer includes the following process modules: (a) Si cavity wafer preparation for the interposer bottom C4 pocket; (b) releasable, self-adhesive layer deposition onto the entire surface; (c) interposer die reconfiguration using pick and place, and tacking; (d) wafer-scale clean and interposer AOI inspection; (e) multiple top-die stacking on reconfigured interposers; and (f) mechanical decarrier and cleaning.

Fig. 7a illustrates the reconfigurable CoW bonding-process sequence. Si cavities are etched onto a silicon wafer to fit the interposer bottom C4 bump. Then the dielectric liner oxide is conformed to the entire silicon surface for better film wettability. After that, the release layer is deposited at a thickness of 1-2 μm. The choice of the intermediate release layer depends not only on its adhering properties, which have to be compatible with the reflow process, but also on its capability of decarrier upon application of a simple mechanical peel-off. Candidate release polymers have been developed according

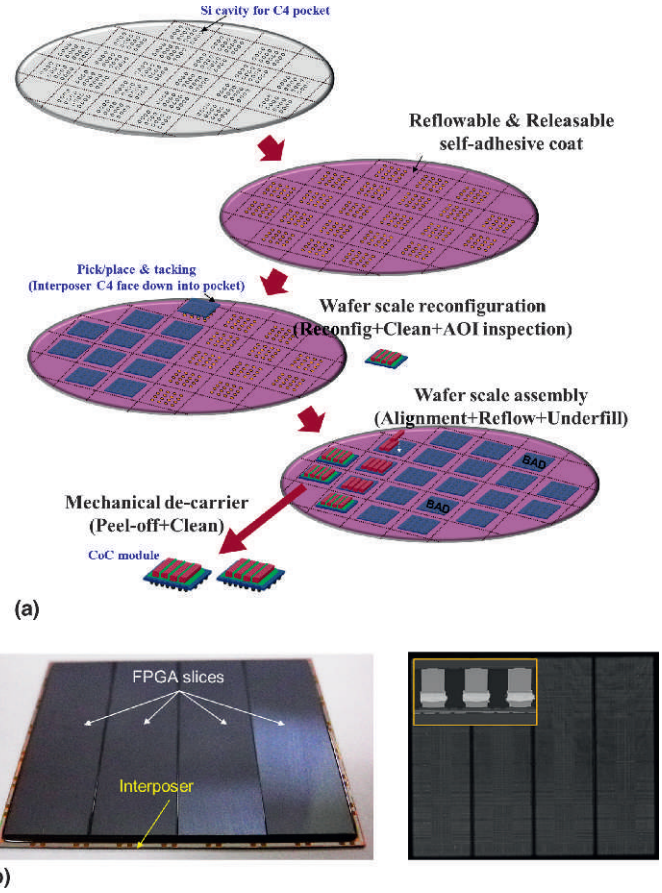


Fig. 7. Innovative, reconfigurable CoW technology. (a) Reconfigurable CoW bonding-process sequence and (b) oblique view of final chip-on-interposer module.

to the criteria, and a die pick-and-place procedure has been defined and optimized for each of them. The idea of the interposer pick-and-place procedure is to attach, at low temperature, the interposer die to the deposit-release glue layer only, in a fast and reliable operation, leading to a high-throughput process. At this step, interposer warpage becomes almost flat, through the thin, self-adhesive, release layer, and retains the flatness even during high reflow peak temperature (reflowable properties). Top FPGA slices are then sequentially stacked on the reconfigured interposer units with mass reflow and underfilling processes. Then the reconfigured and stacked wafer is flipped onto the blue-tape film frame and all individual stacked modules are mechanically detached from the base wafer. Fig. 7b shows four FPGA dice mounted on an interposer die using the process seen in Fig. 7a. All the microjoint results revealed quite uniform joint quality and stand-off height across the 25 mm × 31 mm interposer area.

The subsequent flip-chip BGA process with this CoC stack module was exactly the same as the standard flip-chip ball grid array assembly process in production (i.e., flip-chip mount, underfill, heat spreader attach, and BGA ball mount).

C. New Microbump Scheme for High-Temperature Reliability

Another manufacturing challenge is the need for highly reliable microjoining metallurgy and bonding technology.

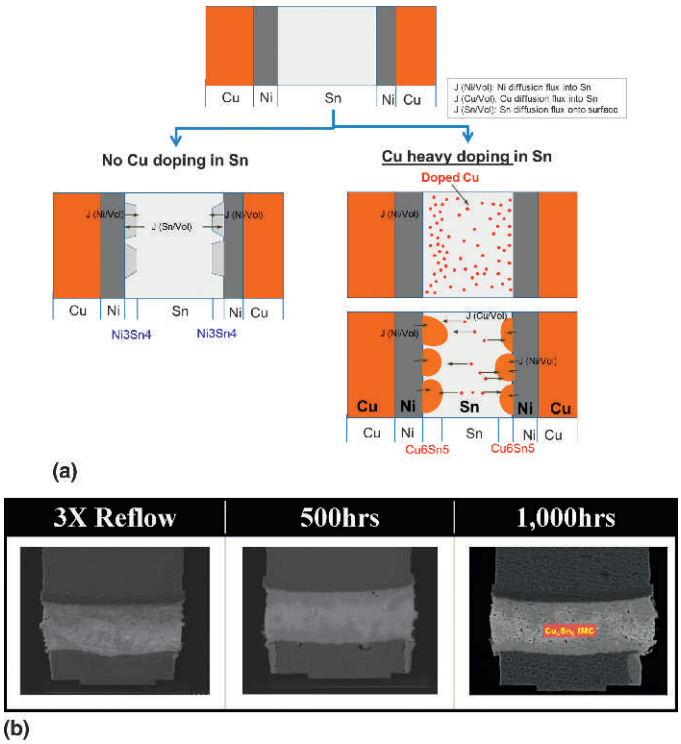


Fig. 8. (a) A schematic model of the possible fluxes due to interdiffusion without and with heavy doped Cu element in solder (not to scale). (b) Cross-sectional images after high-temperature storage test at 150°C.

In copper pillar microbump structure, there is a limited amount of Sn and dual consumption of the limited Sn atoms for intermetallic formation from top and bottom UBM pads. There are adverse effects of this in terms of long-term reliability with respect to voiding symptoms in microjoints. Furthermore, it is known to have net volume shrinkage when IMCs form during the reaction between Sn and a UBM metal. The theoretical shrinkage values can be calculated given the molar volumes of IMCs and those of the pure elements [4-6]. As calculated in the literature, the microjoint height has to shrink by 11.3% in the case of Ni_3Sn_4, and by 5.0% and 4.3% in the cases of Cu_6Sn_5 and Cu_3Sn.

Due to both limited Sn volume in microbumps and volume shrinkage due to fast Sn intermetallic (Ni-Sn and Cu-Sn) formation, volumetric voiding or cracking defects used to be the primary concern for long-term aging reliability tests. To solve this technical limitation, a copper heavy-doping approach into SnAg solder was invented to minimize the undesirable void formation and intermetallic reaction that could lead to voiding or cracking on both the top and bottom interfaces. Copper doping in the solder system can be accomplished by either ternary SnAgCu plating or thin seed-copper plating on top of Ni barrier layer. Thermodynamically, there is a competing reaction between Ni-Sn and Cu-Sn intermetallic formation, depending on the copper concentration in solder [7-9].That is, when the copper volume exceeds the critical content in the solder, Ni_3Sn_4 phase formation is suppressed and Cu_6Sn_5 phase starts to form even on the Ni metal surface, with copper atoms migrating to form Cu-Sn intermetallic on Ni in Fig 8. This is because Cu-Sn reaction has lower Gibbs free energy than Ni-Sn reaction when the copper concentration in the solder is above the critical limit. This Cu-Sn layer formed on top of the Ni barrier acts as a diffusion reaction barrier for subsequent Ni-Sn IMC formation and sidewall solder wetting. This is why the microjoint is intact even after aging at 150°C for 1,000 h, which is almost same as T0 structure.

Conclusions

There are multiple manufacturing and technical challenges to enable seamless integration and optimization of SSI technology manufacturing for multiple die stacking on TSV interposers. It is demonstrated with Xilinx's 28-nm FPGA SSI technology platform that optimized manufacturing processes and new technology development are crucial to achieve high yield, robust reliability, and high device performance for 3-D technology integration. We have successfully integrated manufacturing technology into a foundry plus OSAT platform that is a major step toward production-worthy technology. In addition to the optimization of manufacturing processes, innovative technologies have been developed with foundry and OSAT collaboration and implemented to address assembly-related issues for further improvement of yield and reliability.

Acknowledgments

The authors would like to thank United Microelectronics Corporation's TSV integration team for valuable contributions and data on this development.

References

[1] K. Saban, "Xilinx stacked silicon interconnect technology delivers breakthrough FPGA capacity, bandwidth, and power efficiency," Xilinx WP 380, Vol. 1.2, December 11, 2012.

[2] H.Y. Chuang, J.J. Yu, M.S. Kuo, H.M. Tong, and C.R. Kao, "Elimination of voids in reactions between Ni and Sn: A novel effect of silver," *Scripta Materialia*, Vol. 66, pp. 171-174, 2012.

[3] J.F. Li, P.A. Agyakwa, and C.M. Johnson, "Interfacial reaction in Cu/Sn/Cu system during the transient liquid phase soldering process," *Acta Materialia*, Vol. 59, pp. 1198-1211, 2011.

[4] J.F. Shackelford and W. Alexander, *CRC Materials Science and Engineering Handbook*, 3rd ed. New York: CRC Press, 2001.

[5] H.P.R. Frederikse, R.J. Fields, and A. Feldman, "Thermal and electrical properties of copper–tin and nickel–tin intermetallics," *Journal of Applied Physics*, Vol. 72, pp. 2879-2882, 1992.

[6] H.Y. Chuang, T.L. Yang, M.S. Kuo, Y.J. Chen, J.J. Yu, C.C. Li, and C. Robert Kao, "Critical concerns in soldering reactions arising from space confinement in 3-D IC packages," IEEE Transactions of Device and Material Reliability, Vol. 12, pp. 233–240, 2012.

[7] J.Y. Kim, Y.C. Sohn, and J. Yu, "Effect of Cu content on the mechanical reliability of Ni/Sn-3.5Ag system," *Journal of Materials Research*, Vol. 22, pp. 770-776, 2007.

[8] M.O. Alam, Y.C. Chan, K.N. Tu, "Effect of 0.5 wt % Cu in Sn-3.5%Ag solder on the interfacial reaction with Au/Ni metallization," *Chemistry of Materials*, Vol. 15, pp. 4340-4342, 2003.

[9] T. Laurila, V. Vuorinen, and M. Paulasto-Krockel, "Impurity and alloying effects on interfacial reaction layers in Pb-free soldering," *Materials Science and Engineering: R: Reports*, Vol. 68, pp. 1-38, 2010.