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Use of Wafer Applied Underfill for 3D Stacking

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***Abstract*—A key element for improving 3D IC stacking and packaging reliability is the choice of the right underfill (UF) material. The underfill is a specialized adhesive whose main purpose is locking together the top and bottom dice; it must fill the gap between bumps and between dice, while reducing the differential movement that would occur during thermal cycling. Traditional underfill processes are based on local dispensing after solder bump reflow (i.e., capillary dispensing), or before flip chip operation with no need of reflow (no flow underfill, NUF). In case of 3D stacking, such processes present some limitations: the need for a dispensing area (die size increase); material flow (spacing between dice), and cost (low throughput). After an introduction on typical underfill applications such as die-to-package and die-to-die assembly, we report the work done to assess the properties of several wafer applied underfill (WAUF) materials and their integration in 3D stacking. These materials were initially applied on silicon wafers in order to assess the minimum achievable thickness and material uniformity. The wafers were coated with different methods: spin coating and film lamination. After this initial assessment, the most promising materials were used for 3D stacking. The test vehicle used has Cu/Sn microbumps with a pitch of 40 μm. The quality of the materials is judged by electrical test, SAM (surface acoustic microscope), and X-SEM (scanning electron microscope).**

***Keywords*—3D Integration, multi-die stacking, wafer applied underfill**

Introduction

Although significant results have been achieved, 3D-IC integration still presents uncertainties that are delaying high volume production. One of these concerns is the reliability of 3D stacking and packaging.

A key element for 3D stacking and packaging reliability is the choice of underfill (UF) to integrate in the assembly processing: die stacking and final packaging. During thermocycling or normal working conditions, the solder joints die-to-package or die-to-die (3D-IC) are affected by fatigue and local stress that can generate failures (e.g., cracks, delamination, see Fig. 1). The main scope of UF is to mitigate the effects of this stress and protect the chip from moisture entrapment and other contaminants (refer to Fig. 2), which can compromise chip performance in the subsequent steps [1]. The requirements for underfill are different as they depend on the target assembly process: die-to-package or die-to-die. In both cases, the choice of the right material is not straightforward.

In the case of the die-to-package assembly, the UF will have to mitigate the differences among the package substrate (typically an organic laminate), the solder bumps (typically ∼100 μm sizes), the silicon die, and the package overmolding. In the case of the die-to-die assembly, the underfill has to mitigate the difference between two silicon dice and microbumps (typically ∼10 μm sizes).

In the following paragraphs we give more details on the die-to-package and die-to-die assembly approaches. Later, we focus on wafer applied UF (WAUF) for die-to-die and die-to-wafer assembly.

A. Underfill in Die-to-Package Assembly (Flip Chip BGA)

Underfill materials and processing are key elements in flip chip ball grid array (BGA) packages. In a flip chip BGA (see Fig. 3) the die is assembled onto a multilayer organic substrate, which is finally soldered onto a printed circuit board (PCB) by solder balls.

In the case of a four-metal-layers substrate, the stack-up typically consists of a thick BT (bismaleimide-triazine, resin based), usually identified as laminate core and coated with copper (inner copper layers).

The inner layers are enclosed by new dielectric layers (i.e., pre-preg, preimpregnated composite fibers) which is then followed by a new copper lamination. The external copper layers are finally protected by coating a liquid photoimageable (LPI) solder resist (typically epoxy or epoxy-acrylate). The solder resist is than selectively etched to allow connections of die-to-substrate (i.e., FC pads) and substrate-to-board (i.e., solder ball pads).

To avoid pad oxidation and/or improve solderability, FC pads and solder ball pads can have different metal finishing (Ni, Au, NiAu, etc.) or organic solderability preservatives (OSP) coating. The different properties of all these materials heavily affect the thermomechanical loads applied to the solder joints.

In a standard working environment, the flip chip BGA package is exposed to several thermocycles (e.g., −40°C/+125°C for reliability check). This creates material deformation and fatigue damage such as cracks and/or delamination as shown in Fig. 1. This type of failure can be limited if the materials used have similar properties. The coefficient of thermal expansion (CTE) and Young's modulus (E) are two main parameters to consider when defining a BGA package. On the other hand, for adhesives like UF, another important parameter that needs to be taken into account is the T_g (glass transition temperature). The T_g of an adhesive indicates the temperature at which the adhesive changes from being a glassy solid to a rubbery material, and usually this transition means a significant increase in the CTE value. The CTE value below T_g is defined as α_1 and

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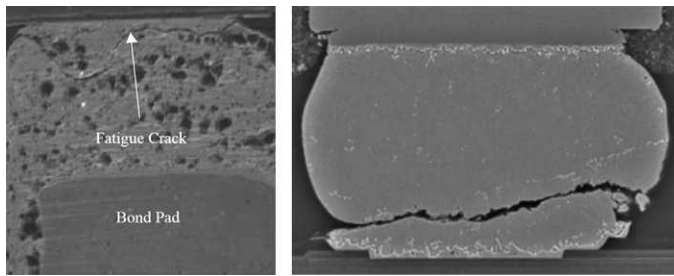

Fig. 1. Example of solder fatigue cracks.

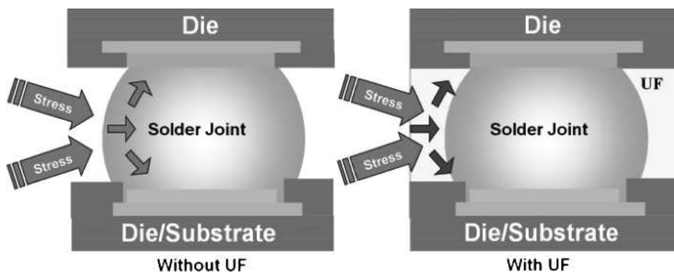

Fig. 2. Underfill mitigates the stress on the solder joint.

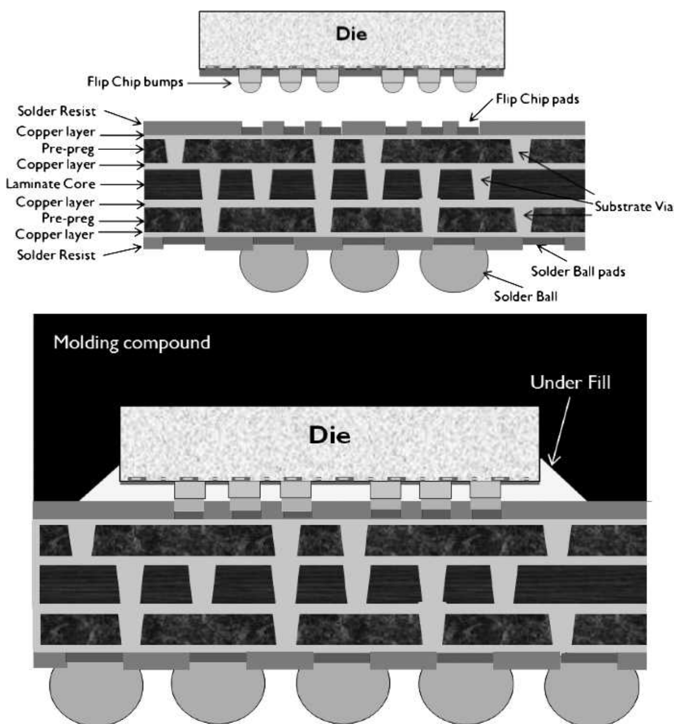

Fig. 3. Typical stack-up for flip chip BGA.

the CTE value above T_g is defined as α_2. High CTE values of UF, especially α_2, would cause high shear strain in the thermal shock condition, induced by the CTE mismatch. This is the reason why most UFs are formulated to have a T_g value well above the use temperature.

Table I illustrates the Young's modulus and the CTE values for typical materials in an FC BGA package.

In a flip chip package, the UF is used to fill the gap between the die and the substrate (refer to Figs. 2 and 3). The application

Table I
Young's Modulus and CTE for Typical FC BGA Package Materials

Material	E (GPa)	CTE (ppm/°C)
Aluminum	70	23
Copper	117	17
Diamond	940	1
Nickel	200	13
Silicon carbide	450	2.77
Silicon	169	3
Gold	80	14
Solder bump (Pb90Sn10)	27.3	24.5
Solder bump (Sn3.5Ag)	30	21.5
CuSn IMC	110	23
Polyimide	8.3	15
Silicon nitride	250	3.2
Epoxy	15	55
Molding compound-1	17	18
FR-4 substrate	17	3
BT substrate	15	27
Ceramic substrate	85.3	14

of UF reduces the thermal expansion mismatch between the silicon die and the organic substrate and protects the solder bumps [1]. UF is normally applied at one or more sides of the die by filling the die-to-package gap under capillary action (capillary UF). The quality of the filling process is dependent on parameters such as die size, bump pitch, gap height, UF viscosity, flow time, surface tension, wettability of substrate solder mask, die passivation layer, and bump material [2, 3]. The best combination of all these parameters is the key factor for successful flip chip package. The use of capillary UF is time-consuming as it requires enough time for the capillary action and an additional curing step (see Fig. 4). These two aspects are not negligible and negatively affect the assembly throughput.

Furthermore, apart from the processing time, another concern that is related to capillary UF is the area required for dispensing. To ensure a complete gap filling in an acceptable time, enough dispensing area should be available on the landing substrate. This is not always the case for components requiring high system integration and, together with timing requirements, represent a key disadvantage of capillary UF.

To circumvent these issues, two approaches are currently being considered: vacuum UF and no flow UF (NUF).

The first approach (vacuum UF) is mainly an extension of capillary UF (see Fig. 5) by enhancing material flow with gas pressure [4] This approach is at the moment still in a concept phase and far from becoming a standard for volume production. It offers advantages in terms of good gap filling (e.g., no air bubbles trapped), but still presents concerns in terms of throughput and required equipment upgrade.

The second approach, based on NUF, is more widely used. In this approach, the material is dispensed on the landing substrate before die stacking. In this case, the flip chip operation has the double function of die-substrate bonding and curing the UF [5]. This approach fits standard flip chip operations and, even if the UF is not fully cured during stacking (typically ~90% of material is cured), complete curing is obtained by assembly steps such as post molding cure. This approach presents concerns such as that the material needs to be transparent to see alignment marks during FC operation, dispense timing

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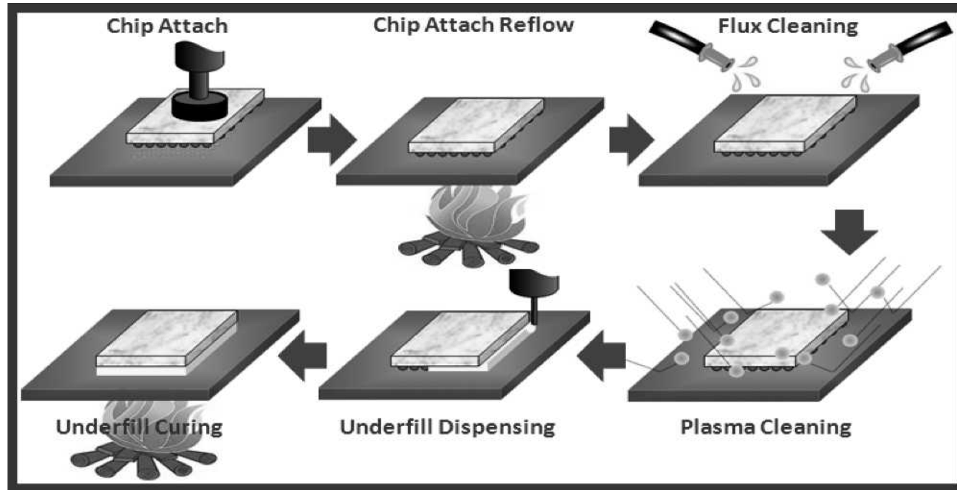

Fig. 4. Assembly process in case of capillary UF.

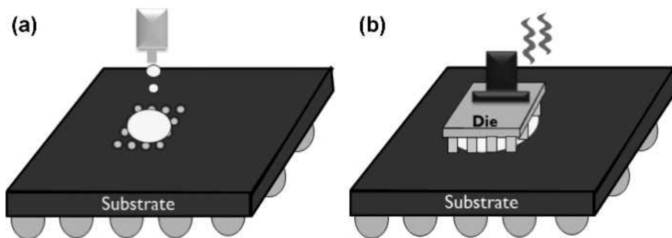

Fig. 5. Assembly process in case of NUF: (a) UF dispensing; (b) Die flip chip (typically thermo-compression bonding).

(still done for each single die), UF/filler entrapment between bumps, and voids and other defects related to material flow (see Fig. 6). Problems such as transparency and filler entrapment can be solved by using filler-less or nano-filled materials, but both options have disadvantages for reliability and cost.

B. Underfill in Die-to-Die Assembly

The main goal for 3D-IC integration is to increase device density by using high density vertical connections, that is, 3D stacking. The processes needed for 3D integration start from the formation of through-silicon-vias (TSVs) and move along wafer thinning, backside processing, microbumping, and stacking including UF [6, 7]. The UF used in this die-to-die assembly enhances the bonding between dice and prevents entrapment of moisture and other contaminants. In 3D stacking, the main challenges for UF are the narrow gaps between dice (~10 μm) and fine microbump pitches (~20 μm). The final package in which 3D stacks will be encapsulated will depend on the final application, and considering that mobile applications are the main driver for 3D integration, the BGA package is the typical option (see Fig. 7).

Considering the challenges of die-to-die assembly in 3D integration, the use of capillary UF is not an immediate choice. This is mainly due to the following reasons: (a) narrow gap and the fine bump pitch, which require extremely low viscosity materials and/or process development (e.g., vacuum supported underfill [4]); (b) need for dedicated dispensing area, which limits the possibility of stacking dice with the same size.

Better choice is considered to be the use of NUF. In case of NUF, apart from the same concerns present for die-to-package assembly (material transparency, dispense timing, UF/filler entrapment, voids, etc.) another issue is related to the volume control required to avoid UF overflows on the die backside. The UF overflow can contaminate backside pads. Excess UF can also be thicker than microbumps and prevent die-to-die stacking (see Figs. 8 and 9). Avoiding backside overflow is a fundamental requirement for multidie stacking where dispense volume control is critical.

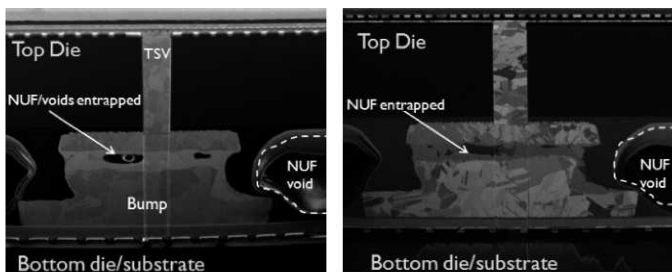

Fig. 6. Defects seen in the case of assemblies using NUF material.

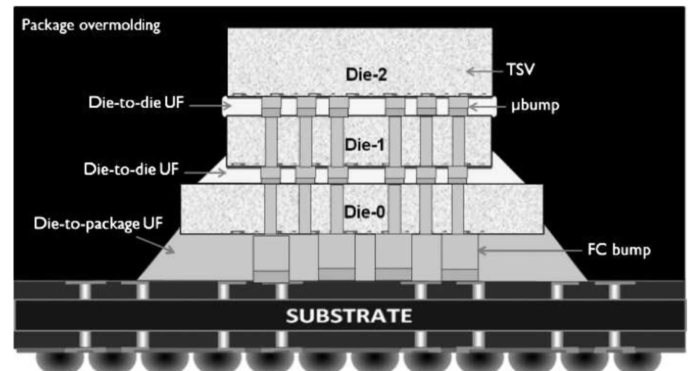

Fig. 7. Typical stack-up in the case of BGA package with multi-die stack.

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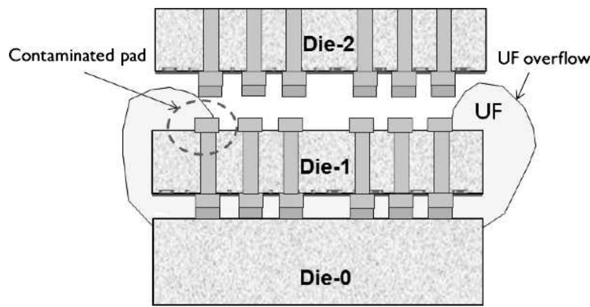

Fig. 8. UF flowing to die backside contaminating backside pad/bump.

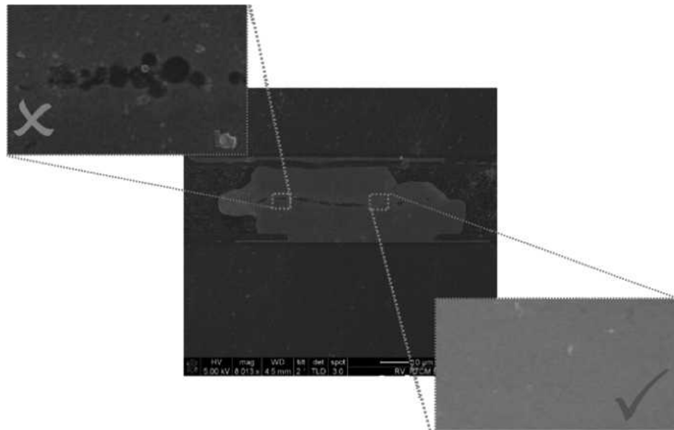

Fig. 9. Example of UF filler entrapment between bumps of stacked dice. Top left picture indicates areas with entrapped filler, while the bottom right picture shows area filler-free.

C. WAUF and 3D Integration

Local dispensable UF, like capillary UF and NUF have both a fundamental limit that is related to the timing for dispensing: for both kinds of UF the dispense is done locally for each die/stack with negative effects on throughput. WAUF is therefore a valuable candidate to increase UF processing throughput. WAUF can be put in two main categories: spin coatable WAUF (UF is applied on wafer by spin coating) and film WAUF (UF is laminated on the wafer, preferably by vacuum lamination). Typical process flows for both materials are depicted in Fig. 10.

These two categories of materials can be compared in terms of material properties (refer to Table II) but also in terms of processing. From a processing point of view, both categories of UF present advantages and disadvantages. Table III presents an initial comparison between the two categories.

Another way to compare these materials is to identify the possible advantages and disadvantages that they will bring to 3D stacking flow.

To achieve 3D stacking, there are three main approaches that are currently pursued: die-to-die (D2D), die-to-wafer (D2W), and wafer-to-wafer (W2W). In this work, we consider only the first two approaches.

The D2D approach also has two alternatives: (a) die-to-package followed by sequential die-to-die stacking (typical approach used by packaging houses) and (b) die-to-die stacking to make die-cube followed by die-cube-to-package stacking (i.e., a typical approach that could be used by a device manufacturer). The D2W approach also has two variations: (a) Die-to-wafer with individual bonding (each die is individually bonded on the landing wafer) and (b) die-to-wafer with collective bonding (dice are firstly placed on the landing wafer and then collectively bonded).

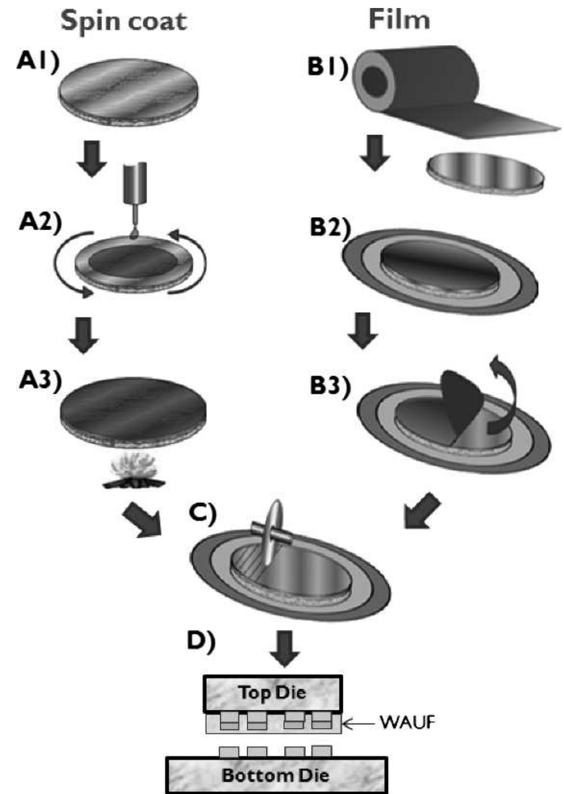

Fig. 10. Process flows for spin coat or film wafer applied underfill. Left-side process: spin coat flow. (A1) Incoming bumped wafer (200 mm diameter). (A2) Spin coating using manual spinner. (A3) B-stage (curing) on hot plate. (C) Dicing of coated wafer. (D) Die-to-die assembly. Right-side process: film lamination flow. (B1) Vacuum lamination on bumped wafer. (B2) Wafer mounting on dicing frame. (B3) Removal of UF protective film. (C) Dicing of laminated wafer. (D) Die-to-die assembly.

Table II
Material Properties for Some Evaluated Materials

Material	E (GPa)	T_g (°C)	CTE (ppm/°C) α_1	CTE (ppm/°C) α_2
Capillary_UF1	9.0	100	26	90
Capillary_UF2	2.9	125	40	125
Capillary_UF3	2.0	110	50	160
NUF_1	2.6	81	75	190
NUF_2	5.8	87	31	64
NUF_3	8.6	87	30	71
NUF_4	3.4	152	56	172
F-WLUF_1	8.4	110	31	116
F-WLUF_6	6.8	118	47	147
F-WLUF_7	3.8	128	35	148
F-WLUF_3	5.6	109	43	89
L-WLUF_4	8.5	93	32	165
L-WLUF_5	2.8	117	78	210
L-WLUF_2	1.7	74	49	284
Molding compound-1	23.5	125	0.9	3.4
Molding compound-2	18	180	13	38

Notes: F-WLUF indicates film wafer level UF, L-WLUF indicates spin coatable UF. Molding compounds are included as reference.

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Table III
Comparison for Processing Spin Coat WAUF vs. Film WAUF

Spin Coat WAUF	
Pros	Cons
Freshness: material defrosted just before use Earlier to use: spinner more common and less expensive than vacuum laminator	Material waste disposal: drainage system required Need low viscosity materials for uniform coating and low thickness Limited pot life (∼days) B-stage step is critical
Film WAUF	
Pros	Cons
Longer pot life (∼weeks) Not strongly dependent on bump distribution, thanks to vacuum lamination No B-stage required: fewer process steps Easy material waste disposal	Need vacuum laminator Need protective film to avoid contamination

In case of D2D stacking, the WAUF is applied at the wafer level prior to dicing and stacking (see Fig. 11).

In the case of D2W, there are multiple options: WAUF applied before die-to-wafer bonding (after dicing, same as in the case of die-to-die), WAUF applied on landing wafer during die-to-wafer bonding, or a combination of both options (see Fig. 12). The option of having the WAUF applied before die-to-wafer offers more advantages in terms of process manufacturability: UF coating/lamination can be done in batches (all wafers processed before dicing); or final dicing can be done using the alignment marks of the landing wafers (these marks are less visible in the case where WAUF is present on the wafer). A more complete comparison is given in Table IV.

D. Evaluation Procedure for WAUF

WAUF materials have been evaluated in three subsequent phases: (a) pre-screening and material selection; (b) requirements assessment; and (c) assembly test.

In the prescreening phase, before starting any evaluation, the material vendors have been requested to propose materials that could fulfill (at least partially) the following requirements:

- Able to reach uniform material thickness (<30 μm, 10 μm target).
- Able to fill gap for small bump pitch (≤40 μm).

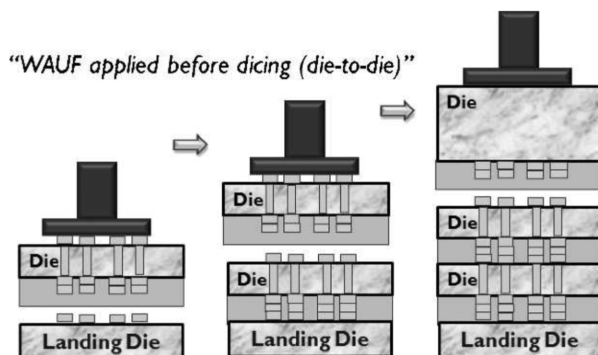

Fig. 11. Die-to-die stacking using WAUF.

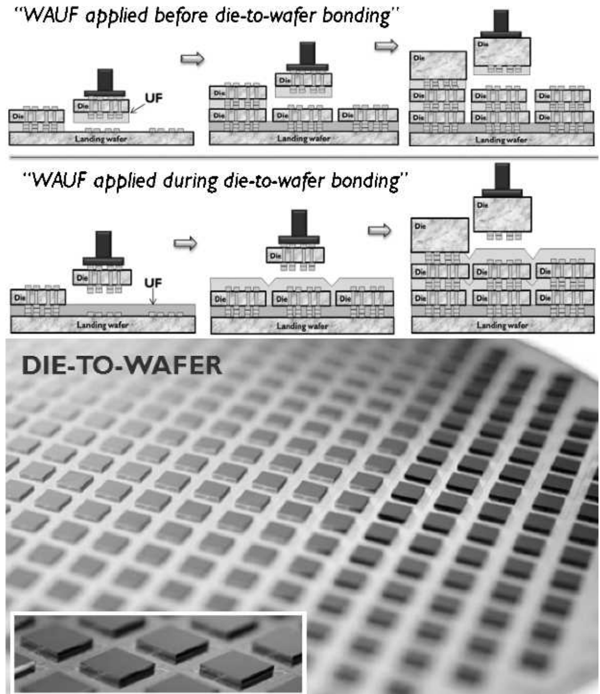

Fig. 12. Die-to-wafer stacking process by using WAUF.

Table IV
Comparison for Processing WAUF Before D2W Bonding or During D2W Bonding

WAUF before D2W stacking	
Pros	Cons
Wafer can be processed in batches then go to dicing Spacing between stacks is free from UF material (marks on landing wafer are visible) Fits both stacking approaches: D2D and D2W Easier to integrate: wafer is not transferred to other equipments for UF coating/lamination	Special trays required to carry dice with UF (UF can stack die in the tray) Dicing can contaminate UF (particles) Lamination of thin wafers can be complex (need of carrier? Or covering when on dicing frame?)
WAUF during D2W stacking	
Pros	Cons
Gap between stacks is filled while stacking: free wafer reconstruction No particle contamination due to dicing	Application after die stacking can induce topography between stacks UF material will cover marks on landing wafer UF covering after die stacks will require transfer to new equipment coater/laminator

- High transparency to allow die alignment based on control marks.
- Good tackiness at ambient temperature.
- Low curing temperature.
- Process capability up to 250°C.

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After this initial screening, mainly based on material datasheets and the supplier's suggestions/experience, the selected materials are moved to the requirements assessment phase.

Requirements Assessment and Test Vehicles

The scope of this phase is to assess whether the materials proposed by suppliers are in line with the requirements. The wafers used in this phase are initially dummy silicon wafers (200 mm wafer diameter) and are later device wafers.

The device wafers consist of two different test vehicles that are later stacked on top of each other using die-to-die assembly.

The two test vehicles are named: PTCM (packaging test chip, version M) and PTCN (packaging test chip, version N). They are processed using 130 nm CMOS technology with two metal layers BEOL (back end of line). The microbumps are placed in a periphery array configuration with a 40 μm bump pitch.

The stack PTCM + PTCN (refer to Fig. 13) is electrically characterized by measuring the resistance of the daisy chain (DC) structures. These structures are accessible on the bottom die (larger than the top die).

The design parameters of test vehicles are summarized in Table V. The target requirements for this phase are the following:

- Thickness range achievable.
- Thickness uniformity.
- Absence of defects.
- Transparency.
- Process ease.
- Reworkability.

A. Thickness Range Achievable

Material is coated on 200 mm wafers and then thickness is measured. Target is to get a minimum thickness in the range of 10 μm and exclude materials that are far from this value (>30 μm).

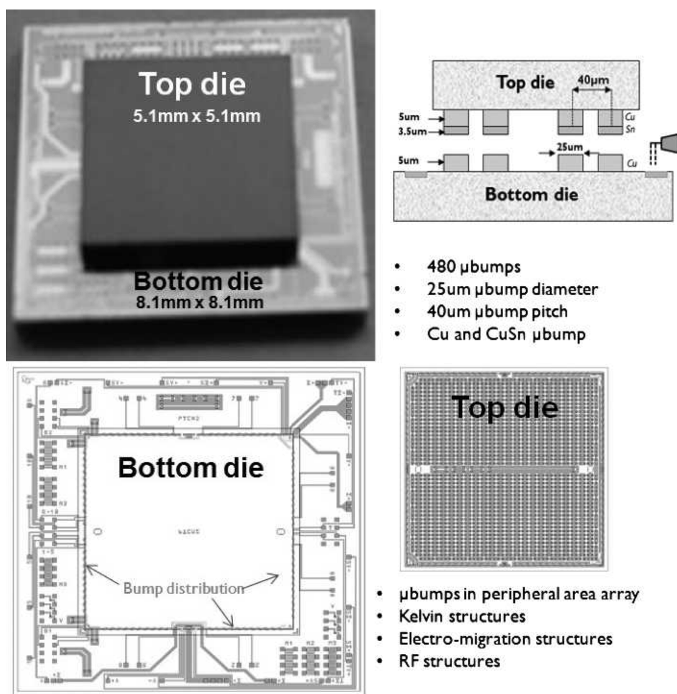

Fig. 13. Layout and characteristics of used test vehicle.

Table V
Design Parameters of Used Test Vehicles

	PTCM (Top die)	PTCN (Bottom die)
Die size	5.1 mm × 5.1 mm	8.1 mm × 8.1 mm
Microump pitch	40 μm	40 μm
Microbump diameter	25 μm	25 μm
Microbump metallurgy	Cu/Sn	Cu
Microbump thickness	5 μm/3.5 μm	5 μm
Number of microbumps	480	480

B. Thickness Uniformity

After coating, the material uniformity is measured by Ellipsometer. Target is to get material uniformly distributed on the wafer with a max TTV (Total Thickness Variation) below 2 μm.

C. Absence of Defects

Coated material should not present any visible defects: voids, cracks, residues, etc.

D. Transparency

Coated material should be transparent to allow bonding alignment based on pattern recognition (alignment marks).

E. Process Ease

The judgment is based on the complexity to prepare the material, repeatability of the process, storage requirement, shelf life, frost-defrost, tool cleaning, and drainage.

F. Rework-ability

The judgment is based on the possibility of removing the coated material to allow rework in case of misprocess.

Requirement Assessment Results

A total of nine suppliers were contacted in this phase and only three of them were able to provide materials (other materials were proposed later, but the evaluation results are not reported in this paper).

The selected suppliers provided a total of five materials, named, respectively: A1, A2, and A3 (spin coatable types), and B1 and B5 (film types).

The first spin coatable (A1) material was immediately discarded after the spin coating exercise. Material A2 could be slightly optimized but was still not in line with the requirements; even the highest rotation speed (3000 rpm) could not confer uniform material coating on the wafers (see Fig. 14).

More promising where the remaining three materials, the spin coatable material (A3) and the two films (B1, B2).

Material A3 was initially processed to identify the best spinning conditions on full thickness (725 μm) wafers. These conditions were then confirmed/assessed in the following cases: (a) Full thickness blanket wafer; (b) Thinned (25 μm) blanket wafer on carrier; (c) Full thickness top-die bumped wafers.

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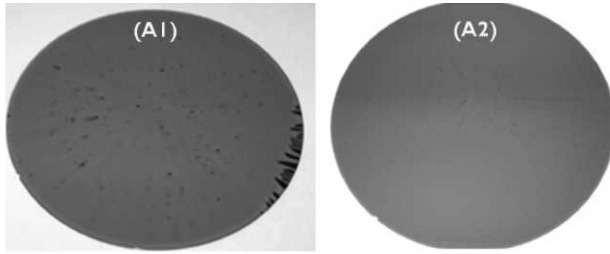

Fig. 14. Aspect of materials A1 and A2 after spin coating at 3,000 rpm.

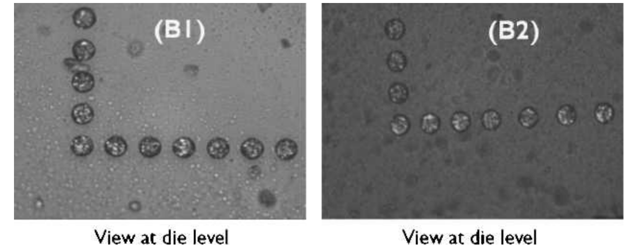

Fig. 16. Aspect of material B1 and B2 after spin lamination on top-die bumped wafers and dicing (die level).

The results of this evaluation are shown in Table VI and Fig. 15, and they are in line with the most important requirements: 15 μm thickness (±2 μm), high transparency, and absence of defects.

While all the process steps for the spin coatable materials were performed at IMEC facilities, the two film materials were laminated at the supplier site. This was due to the requirement for a vacuum lamination system, which is not at available at IMEC.

The two film materials where also laminated, in this case on the top-die wafers.

The thickness measurements showed good alignment with the requirements (15 μm ±2 μm) but the transparency of the materials was inferior to material A3; we also observed more particles than in the case of the A3 material (see Fig. 16).

The transparency of the material is in general related to the filler content (percentage and size) and the base chemistry; these properties are reported in Table VII for all evaluated materials.

Regarding the higher number of particles observed on the film types, this may be due to the tackiness of the materials: film materials were tackier than the spin coatable materials, therefore trapping more particles during dicing.

Even if materials B1 and B2 were both opaque and did not allow alignment marks to be seen, the bumps were still visible, so that the assembly could be performed by using manual bump-to-bump alignment.

Table VI
Thickness Measurements with WAUF Material A3

Spinning speed (rpm)	Wafer type	Ellipsometer (avg) (μm)	△ (Max − min) (μm)
2,500	Blanket full thickness	16.49	0.14
2,500	Blanket thinned on carrier	16.41	0.27
3,000	Blanket full thickness	13.72	0.28
3,000	Blanket full thickness	15.42	1.3

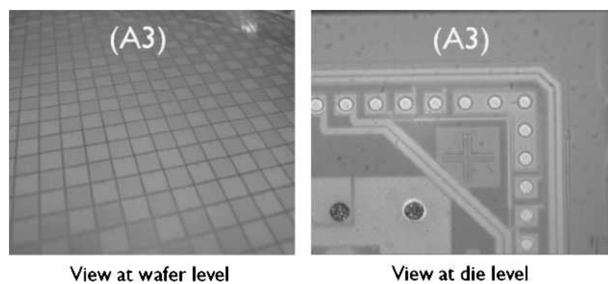

Fig. 15. Aspect of material A3 after spin coating on top-die bumped wafer and dicing (die level).

Assembly Test

After the previous phase, the materials A3, B1, and B2 were moved to the next phase, the assembly test.

The assembly flow used to stack the two test vehicles is shown in Fig. 10.

The three materials were assessed based on the following criteria:

- Dicing
- Tackiness
- Electrical test
- SAM
- X-SEM

A. Dicing

After removal of the protective film (see Fig. 17), the wafers covered with WAUF material are placed on a dicing frame and later diced. The requirements are:

- No smearing due to dicing.
- No delamination.
- No particles trapped in the material during dicing.
- No material degradation due to blade/water interaction.

B. Tackiness

The dice are placed on a landing wafer heated to 80°C at the lowest pressure. The requirements are:

- Dice stay in place (no movement) after wafer population for ~1 hr.
- Dice stay in place (no movement) if wafer is transferred from one tool to another tool (2 m distance).

C. Electrical Test

After dicing, the dice with WAUF are bonded on the bottom dice using the die-to-die assembly process.

The bonding yield is defined by the number of functional daisy chain connections, which is also the main parameter to assess the materials in this phase (refer also to Fig. 13).

D. XSEM and SAM

After bonding, the stacked dice are analyzed by SAM (surface acoustical scanning) to check eventual material

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Table VII
Material Properties in Terms of Filler Content and Optical Clarity

Material	A1	A2	A3	B1	B2
Base chemistry	Epoxy	Epoxy	Epoxy	Hybrid	Epoxy
Filler %	50/60	40/50	20/30	20	40
Filler size	μm (10 μm max)	μm (5 μm max)	nm (∼50 nm)	nm (∼50 nm)	nm + μm
Flux agent	Yes	Yes	Yes	Yes	Yes
Optical clarity	Translucent	Translucent	Transparent	Transparent	Transparent/translucent

Fig. 17. Removal of protective film from wafer with WAUF and placement of dicing tape.

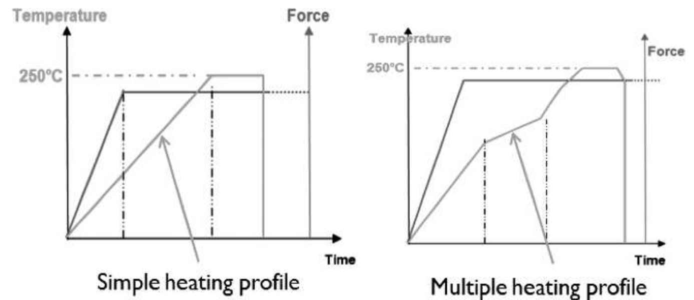

Fig. 18. Examples of simple/multiple heating profiles used for assembly test.

delamination and cross-sectioned to check failures and micro-bump interconnection.

E. Assembly Test Results

The first two criteria for the assembly test (dicing and tackiness) were performed by optical inspection after each step with following results:

- No UF delamination or smearing.
- No dirtying of the blade observed.
- Some particles trapped in UF (mainly in the case of materials B1 and B2, the film samples).
- No deterioration of UF material.
- Tackiness test passed by all materials (dice stay in place for at least 2 days).

For what the electrical test, the stacks were assembled using different bonding profiles where the following parameters were considered:

- Simple/multiple heating profiles.
- Higher/lower bonding pressure.
- Shorter/longer bonding time.

For each bonding profile we assembled 10 stacks. An example of heating profiles is given in Fig. 18, while in Table VIII and Table IX the achieved electrical yield is reported in the cases of all bonding profiles (see samples Pr_1 through Pr_10).

From Table VIII and Table IX, it appears evident that only two materials gave electrical yielding stacks: material A3 (spin coatable) and material B2 (film).

It is also evident that the bonding profile can sensibly affect the final electrical yield, and therefore can be further optimized for yield improvement.

Summarizing the previous assessments, the electrical results, data coming from SAM images (see Fig. 19), and cross sections (see Fig. 20), we have deduced the following indications for justifying the failure/success of the 3D stacks:

Table VIII
Summary Table Indicating Electrical Yield for Defined Bonding Conditions in Function of Pressure and Heating Profiles

	Simple Heating Profile				Multiple Heating Profile			Multiple Heating Profile		
Material	Pr_1	Pr_2	Pr_3	Pr_4	Pr_5	Pr_6	Pr_7	Pr_8	Pr_9	Pr_10
A2	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
A3	NO	NO	NO	NO	YES (40%)	YES (40%)	YES (50%)	NO	NO	YES (20%)
B1	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
B2	NO	NO	NO	NO	YES (50%)	NO	NO	YES (30%)	YES (20%)	NO

Pressure

- Material A2 is too opaque and thick so dice cannot be properly aligned during bonding and the material is not squeezed out to allow connection. It is believed that required improvements to achieve an acceptable yielding percentage (>80%) are out of range for this material: material A2 is not considered for further development.
- Material A3 has the required uniform thickness and it is transparent, these factors allow proper material squeezing and good bonding alignment. It is believed that further material improvements can grant an acceptable yielding percentage (>80%): material A3 is considered for further development.
- Material B1 needs further optimization in the base chemistry to allow good intermetallic formation. Even if opaque, good alignment is achieved but this is not enough to grant an electrical yield. It is believed that improvements will not be sufficient to grant an acceptable yielding percentage (>80%): material B1 is not considered for further development.
- Material B2 is slightly opaque, but good alignment is achievable. The thickness of the material is also fine and

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Table IX
Summary Table of Electrical Yield Results Based on Bonding Profiles

Bonding profile	Material/electrical yield (%)			
	A1	A3	B1	B2
Pr_1	0	0	0	0
Pr_2	0	0	0	0
Pr_3	0	0	0	0
Pr_4	0	0	0	0
Pr_5	0	40	0	50
Pr_6	0	40	0	0
Pr_7	0	50	0	0
Pr_8	0	0	0	30
Pr_9	0	0	0	20
Pr_10	0	20	0	0

Note: 10 stacks done for each profile: total 100 stacks.

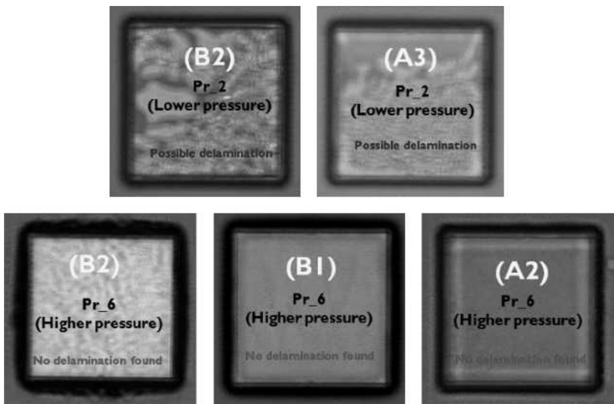

Fig. 19. SAM inspections of stacks bonded with different materials and bonding profiles.

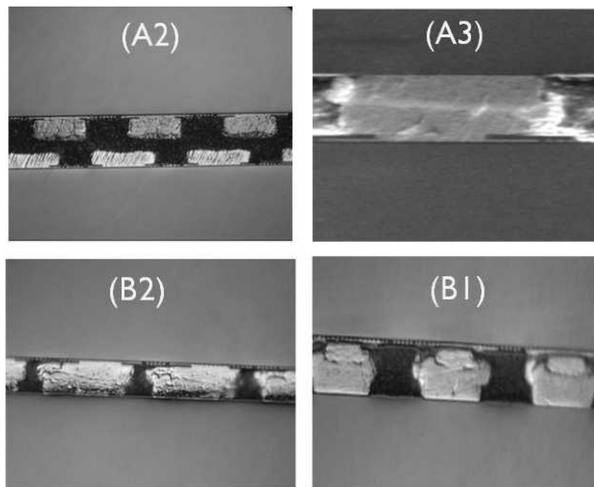

Fig. 20. Cross section of stacks with different materials.

the base chemistry allows some electrical yielding stacks. It is believed that further material improvements can grant an acceptable yielding percentage (>80%): material B2 is considered for further development.

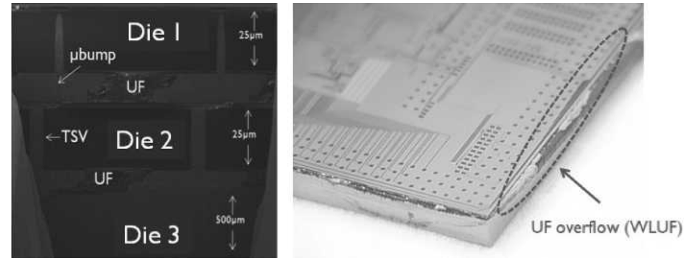

Fig. 21. Cross section and optical image of 3D stacking using WAUF in case of 3-dice level stacking.

Conclusions

WAUFs offer advantages when compared to standard capillary or local dispensable materials: high process throughput, in line with multi-die stacking processing (also in case of same dice size) and process scalability for small microbump pitch (≤40 μm).

In this work we reported on the evaluation of five WAUF materials (three spin coatable and two films). The evaluation was performed on blanket wafers and functional devices with 40 μm bump pitch in peripheral area array configuration. Among the evaluated materials, only two showed good electrical yielding on the selected test vehicles.

The achieved electrical yield can easily be improved by modifying the bonding profiles. The results obtained with this evaluation are very encouraging for future use of WAUF materials in 3D-IC integration flows.

New activities are now ongoing at IMEC to investigate/develop new WAUF materials that could be used for 3D multiple dice stacking (see Fig. 21).

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