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Quantitative Assessment of the Effects of Strain on Future III-V Digital Applications

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Abstract—**In this paper the strain effects on the performance and reliability of future digital III-V device are discussed. Strain is incorporated in the device during fabrication, packaging, and operation. A high amount of strain can introduce defects and cracks in the epilayer. The band structure of the active device region is also altered due to strain. These strain induced changes determine performance, reliability, and lifetime of the device. Therefore, it is necessary to consider strain effects while designing a device for a particular application. Here, compressive-strain-induced changes are used as design parameters and their impact on the logic performance of the device is studied. It is interpreted that the design significantly decreases the gate leakage current and improves the subthreshold slope.**

Keywords—**Gauge factor, logic, reliability, strain**

Introduction

Recently III-V semiconductor devices for More Moore applications have been developed using advanced growth techniques and have shown promising performance for high speed and low power applications [1]. In most of the cases, these flexible growth techniques incorporate a substantial amount of strain in the device active layer. Thermal strain due to mismatched thermal expansion coefficients, lattice mismatch strain, and other process induced strain are intentionally or unintentionally incorporated in the device during fabrication. Also, strain is transmitted to the active region during device packaging [2]. Chip bending experiments have shown that device performance is highly affected by external geometric bending strain [3]. Strain is also induced in the device during its applications as the device has to perform in a nonsteady environment. For instance, strain can be induced in the system when the device is mounted on a heat sink during thermal cycling operations [4]. A high amount of strain can increase defect density and can increase the risk of semiconductor device failure or decrease the device lifetime. It is also shown that strain alters the band structure of the semiconductor and the material shows modified electronic properties. The transformed electronic properties change the basic current-voltage characteristics of the operating device. Therefore, it is necessary for the device to undergo a thorough strain reliability test and device failure analysis before it is put into commercial use.

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In order to design a device for III-V digital applications, strain effects need to be well understood beforehand. Strain properties can then be used as design parameters to optimize the digital performance of the device.

In this work, we provide a systematic study of compressive strain on the performance of heterojunction field effect transistors (HFET) that have been widely used as a model for next generation III-V digital devices. The compressive-strain-induced changes are used as design parameters and this strain is incorporated in the $In_{0.53}Ga_{0.47}As$ channel using strain transfer virtual substrate (STVS) technology. The thermal strain and external strain are also incorporated into the design equation for realistic analysis. Considering all these effects, an ideal value of 0.8% compressive strain is used for analysis. The impact of strain-induced shift in bandgap and mobility on impact ionization gate current and drive current was analyzed. Also, the gauge factor of the device is extracted, which is used for design consideration. It is interpreted that accurate strain induced design can allow optimization of future logic devices and improve reliability.

Design Parameters of Strained and Lattice Matched Heterojunction Devices

A general design for a digital device begins with the evaluation of material properties like bandgap and mobility and the device dimensions which suit the device performance. For an unstrained InGaAs ($In_{0.53}Ga_{0.47}As$ lattice matched to $Al_{0.42}In_{0.58}As$), these properties are readily available in the literature and can also be obtained using interpolation methods [5]. The mobility and bandgap of the unstrained channel are determined from the following set of equations:

$$\mu_0(x) = 30682 - 71341x + 88556x^2 - 57327x^3 + 17311x^4 \quad (1)$$

$$E_g(x) = 0.36 + 0.63x + 0.43x^2 \quad (2)$$

The band structure is developed for the unstrained heterojunction device by carefully fitting the bandgap and mobility as the simulation parameters.

Theoretical and experimental results predict that the incorporation of strain alters the band structure of the semiconductor and the material shows modified electronic properties [6]. Therefore, it is necessary to evaluate the parameters of strained InGaAs and then use them as simulation parameters. Also, the device dimensions are designed such that the strain contained in

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the layer does not produce misfit dislocations. Once the band structure and other material properties of the strained layer are known, the device characteristics can be obtained by solving Schrodinger's equation self-consistently with Poisson's equation in the simulator.

In the device under test (DUT), a portion of the strain is transferred to the channel using a strain transfer virtual substrate (STVS) of AlInAs buffer layer [7, 8]. The AlInAs epitaxial composition is varied in both the STVS and barrier layer for a uniform transition from the lattice matched channel to the compressively strained channel. For the growth of the InGaAs layer with a lattice constant a_{InGaAs} on an STVS of lattice constant a_{STVS}, the biaxial strain $(\varepsilon_{\mathrm{P}})$ and uniaxial strain developed on the InGaAs channel are given, respectively, by

$$\varepsilon_{\mathrm{P}} = \left(\frac{a_{\mathrm{STVS}} - a_{\mathrm{InGaAs}}}{a_{\mathrm{InGaAs}}}\right)$$
$$\varepsilon_{\perp} = -\frac{2c_{12}}{c_{11}}\varepsilon_{\mathrm{P}} \tag{3}$$

A very important reliability issue is the defects in strained devices during heteroepitaxial growth. Strain relaxation is a major cause of the misfit dislocations, which degrades device performance. There is a particular thickness of the channel for which the strain is comfortably accommodated in the layer and no misfit dislocations are produced. This is the critical thickness of the channel. It is also of technological interest to model the critical thickness considering the effects of strain. Therefore, we utilize the critical thickness model of Cammarata and Sieradzki that shows that the critical thickness for compressive strain is higher than that of tensile strain [9, 10]. The critical layer thickness is determined by the equation below and depicted in Fig. 1.

$$h_c = \frac{b(1-\vartheta\cos^2\alpha)\left[\ln\left(\frac{h_c}{b}\right)+1\right]}{8\pi|\varepsilon_{\mathrm{P}}|(1+\vartheta)\cos\lambda} + \frac{\gamma(1-\vartheta)}{|\varepsilon_{\mathrm{P}}|2G(1+\vartheta)} \tag{4}$$

Here ϑ is Poisson's ratio, b is the magnitude of the Burgers vector, G is the shear modulus, and it is assumed that $\cos\alpha = \cos\lambda = 0.5$. The surface energy γ is obtained by linear interpolation of commonly accepted surface energy values of InAs and GaAs. In our device the thickness of the channel is designed at a thickness below the critical thickness and assumed that no dislocations are present at this thickness.

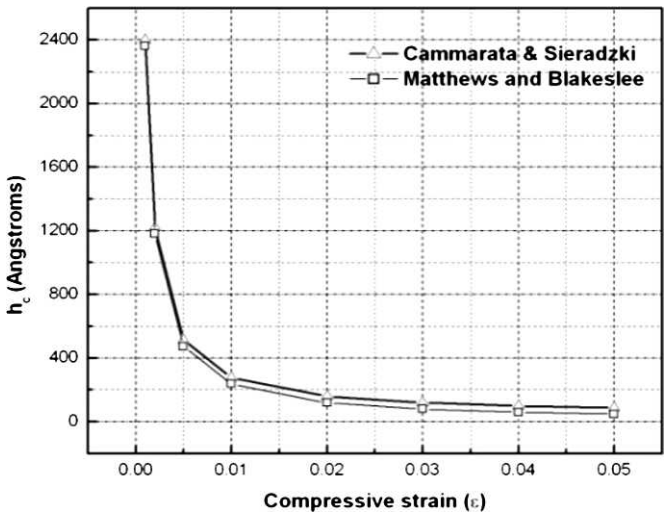

Fig. 1. Critical thickness of a $Al_xIn_{1-x}As/In_{0.53}Ga_{0.47}As/\ Al_xIn_{1-x}As$ quantum well according to the theory of Cammarata and Sieradzki.

While the strain incorporated by the STVS is the dominant factor, in order to have a realistic design, the effects of thermal induced strain and package induced strain are incorporated in the design equation of the strain. The thermal cycles during device fabrication and operation also result in a temperature dependence of the built-in strain. Mechanical stress applied to the device using chip bending experiments can be utilized to study the effect of strain on device performance during packaging tests. Therefore, the total strain on the device can be approximated as the superposition of all the strain components and can be given as:

$$\varepsilon_{\mathrm{P}} = \frac{a_{\mathrm{STVS}} - a_{\mathrm{InGaAs}}}{a_{\mathrm{InGaAs}}} + \int_{T_g}^{T_r} (\alpha_{\mathrm{InGaAs}} - \alpha_{\mathrm{STVS}})dT + \varepsilon_{\mathrm{ext}} \tag{5}$$

Here α is the thermal expansion coefficient which is dependent on temperature and $\varepsilon_{\mathrm{ext}}$ is the geometric bending strain due to packaging and device operation and includes strain components that are not incorporated in the two parts [11]. The limits of integration provide the operation/fabrication temperatures in Kelvin. If α is considered to be temperature independent, then the thermal strain contribution can be interpolated as $0.84 \times 10^{-6}\ \Delta T$, which is tensile in nature. For a growth temperature of 853K, the tensile strain is 0.046%.

Since our focus is the effect of strain on device performance, the combined influence of the three strain components is considered to be compressive. Therefore, we use an ideal value of 0.8% compressive strain for analysis of band structure, gate leakage, and device drive current changes.

The compressive strain lowers the symmetry of the crystal lattice of the semiconductor device, and the bandgap and transport properties are modified. The band gap of the strained semiconductor is obtained by using the formulation of a strained *k.p* framework. This method provides the physics behind the strain and its influence on the band structure of the materials.

The energy correction in the conduction band induced by the strain can be described by the equation [12]:

$$\Delta E_{\mathrm{con}} = 2a' \frac{c_{11} - c_{12}}{c_{11}}\varepsilon_{\mathrm{P}} \tag{6}$$

Here a' is the hydrostatic deformation potential for the conduction band. The energy corrections in the heavy and light hole valence bands are

$$\Delta E_{\mathrm{h}} = \left[2a\frac{c_{11} - c_{12}}{c_{11}} + b\frac{c_{11} + 2c_{12}}{c_{11}}\right]\varepsilon_{\mathrm{P}} \tag{7}$$

$$\Delta E_{\mathrm{l}} = \left[2a\frac{c_{11} - c_{12}}{c_{11}} - b\frac{c_{11} + 2c_{12}}{c_{11}}\right]\varepsilon_{\mathrm{P}} \tag{8}$$

Here a and b are the hydrostatic deformation potential and shear deformation potential for the valence band, respectively. The shift in the bandgap due to compressive strain of 0.8% is

0.0470 eV. The bandgap shift corresponding to compressive strain is shown in Fig. 2.

The parameters that have been used in the calculation for band gap shift are obtained by a linear interpolation of InAs and GaAs as listed in Table I.

The mobility of the electrons is obtained from the model given by Kopf et al. The electron mobility decreases monotonically as a function of biaxial strain in the channel as shown in Fig. 3. The mobility of the charge carrier is modeled as:

$$\mu_{avg} = (\mu_P^2 \mu_\perp)^{1/3} \tag{9}$$

The mobility and bandgap are fitted in the simulator as the material properties of the channel.

The gauge factor of HEMTs is of particular importance for strain induced performance enhancement and reliability studies [13]. The GF determines the sensitivity of the device with respect to the applied strain. This strain factor is therefore a source of information that can be used by engineers while working with strain technology. The gauge factor of the device is given as:

$$GF = \frac{\Delta R}{R\varepsilon_P} \tag{10}$$

Here R is the calculated resistance in the lattice-matched condition and ΔR is the change caused by the compressive strain.

Although the gauge factor utilizes the piezoelectric induced change in 2DEG concentration, here the variation is considered due to the strain induced bandgap shift along with bandgap variation due to the use of a different epitaxial composition barrier that alters the electron concentration in the channel. Further, for the <001> growth direction, there are no piezoelectric contributions [14]. The calculated gauge factor of the strained device is −20.

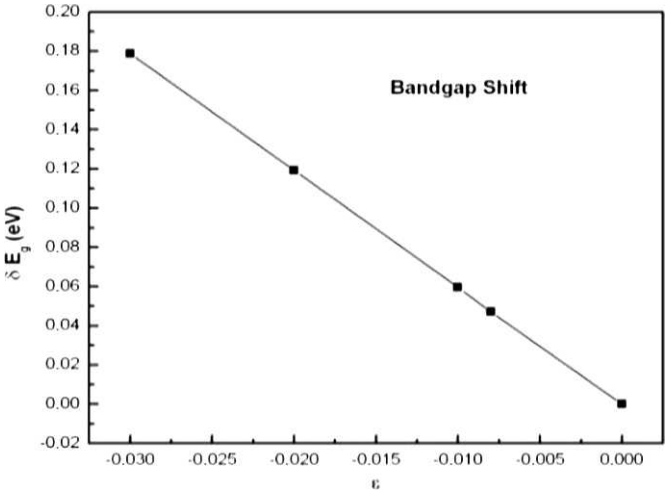

Fig. 2. Bandgap shift profile in $In_{0.53}Ga_{0.47}As$ due to compressive strain.

Table I
Parameters Used for Band Shift Calculations

Parameter	Symbol	InAs	GaAs
Elastic stiffness constant	C_{11}	8.3	11.8
Elastic stiffness constant	C_{12}	4.5	5.4
Hydrostatic deformation potential for conduction band	a'	4.1	6.8
Hydrostatic deformation potential for valence band	a	2.5	2.7
Shear deformation potential for valence band	b	−1.8	−1.7

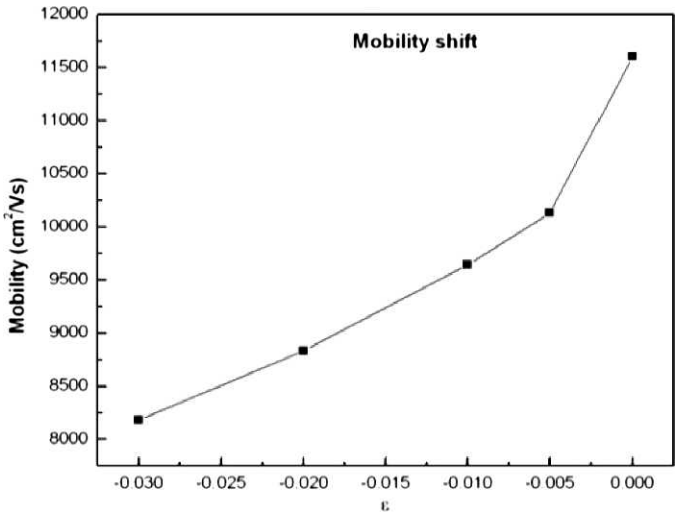

Fig. 3. Mobility shift profile in $In_{0.53}Ga_{0.47}As$ due to compressive strain.

Device Simulator and Structure

Drift-diffusion 2D physical simulations were carried out using the commercially available ATLAS/BLAZE module from SILVACO [15]. The HEMT structures are simulated using a two-dimensional finite-element grid representation and fine meshing was used in the channel and gate region for simulation accuracy. The device physics are obtained from Maxwell's laws and from the current continuity, Poisson, and carrier transport equations. Since these equations form a set of coupled differential equations, the solution of the Schrodinger-Poisson equations are performed by Newton's method. The simulations take impact ionization into account through the generation rate term by activating Selberherr's model. To achieve a realistic gate leakage, the Schottky thermionic emission model is incorporated, which accounts for nonideal effects on the barrier height, such as the image-force-induced barrier-lowering mechanisms. The image-force-induced barrier lowering affects the barrier height, and therefore modulates the gate current. The model parameters were programmed with DECKBUILD and the device parameters and graphics were extracted from data files using TONYPLOT.

The DUT is an HFET [16] that consists of $In_{0.53}Ga_{0.47}As$ active region sandwiched between two AlInAs layers. The epitaxial composition of AlInAs layers in the device is varied to obtain a transition from lattice matched to biaxial compressive strained device structure. The ohmic regions are highly doped at 6×10^{18} cm^{-3}. The 25 nm AlInAs barrier layer is double delta doped to provide the necessary 2DEG charge density. Designs with delta doping of 2×10^{18} cm^{-3} in the barrier are considered to have no parasitic conduction in the barrier. The channel is separated from the doped Schottky barrier by a 2.4 nm spacer layer to prevent scattering due to dopant atoms. The recess layers are passivated with Si_3N_4 and

interface charges are used as per experimental standards. It may be noted that the dimensions and epitaxial compositions of cap layers and channel are kept the same for both the lattice matched (LM) and compressively strained (S) devices considered in the simulation.

Fig. 4 shows the schematic view of the band structure of lattice matched and 0.8% compressively strained heterojunction device. The schematic reveals the increase of bandgap due to compressive strain.

Results and Discussion

In order to investigate the reliability and design of the device, the drain characteristics of the DUT at defined gate voltages are extracted. Fig. 5 shows the shift in the drain characteristics on the application of compressive strain. The reduced drain current is attributed to the decrease in the electron mobility and increased phonon scattering rate due to compressive strain. Note that the carrier confinement in the strained channel is less than that of the lattice matched device due to the use of STVS. The carrier confinement is calculated as $\Delta E_c = 0.64\Delta E_g$. Also, the change in peak linear transconductance g_m induced by compressive strain shows that the design of the device with $\varepsilon < 0$ has a reduction effect in the drain characteristics (Fig. 6).

However, when benchmarked against strained Si technology, strained digital III-V still yields higher mobility.

The strain induced threshold voltage shift is clear in the transfer characteristic curve of the devices in Fig. 7. The threshold voltage shift is due to the change in bandgap, which is determined by the net shift of both the conduction band and the valence band. Also, the threshold voltage shift is related to the changed bandgap of the barrier layer.

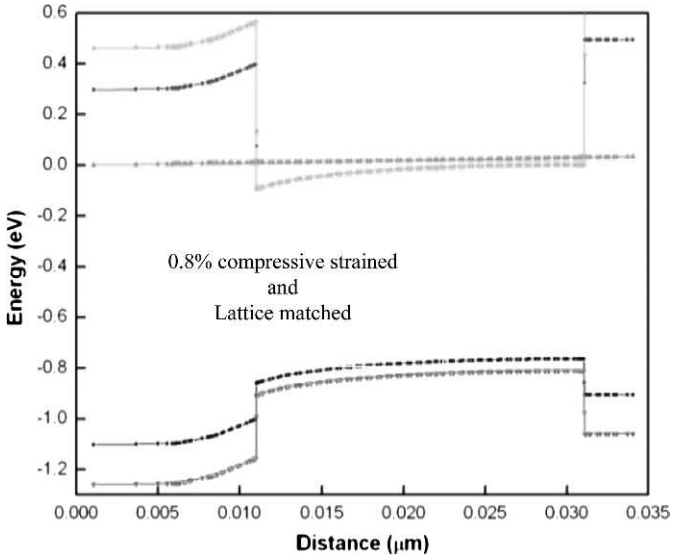

Fig. 4. Band structure in lattice matched and 0.8% compressive strained $Al_xIn_{1-x}As/In_{0.53}Ga_{0.47}As/Al_xIn_{1-x}As$ heterojunction based HEMT.

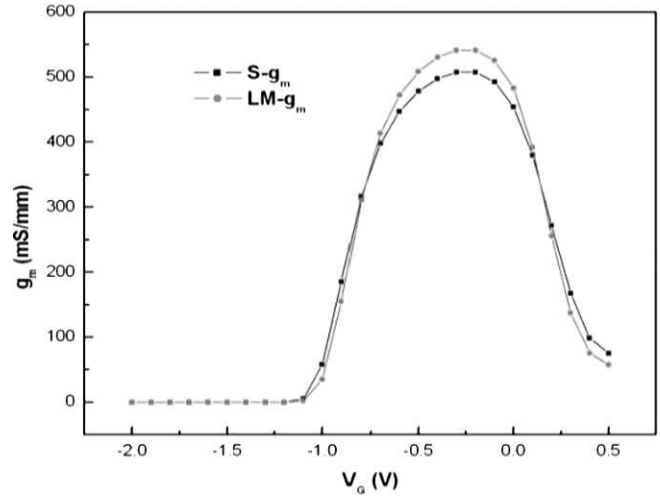

Fig. 6. Comparison of transconductance between strained (S) and lattice-matched (LM) HEMT.

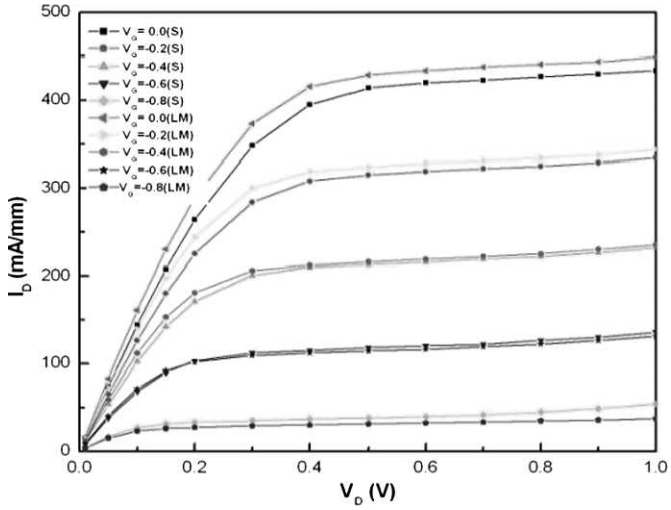

Fig. 5. Drive current reduction of strained device compared with lattice-matched device.

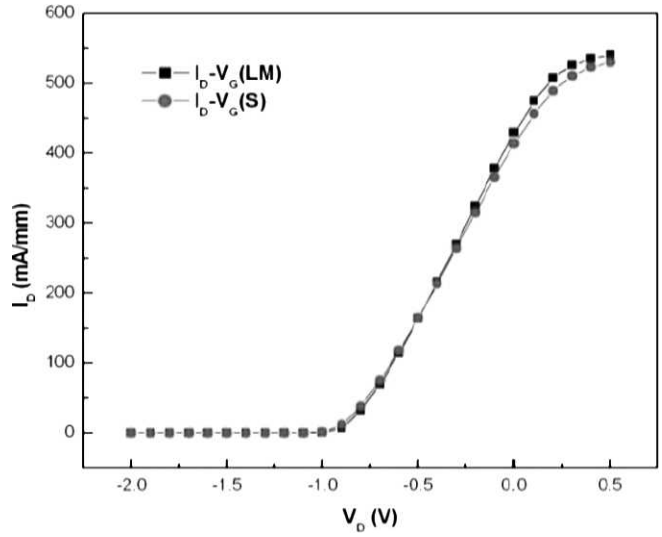

Fig. 7. Transfer characteristics of the investigated LM and S heterojunction devices.

In order to investigate the effect of compressive strain on logic performance, the logic figure of merits needs to be analyzed. Fig. 8 shows a typical curve of drain current versus gate voltage (V_G) in logarithmic scale for the strained and lattice matched device at a drain bias of 0.5 V. It allows measurement of many logic determinants such as subthreshold slope, I_{OFF}, I_{ON}, and threshold voltage (V_T). The subthreshold slope for the compressively strained device (88 mV/dec) comes closer to the theoretical limit of 60 mV/dec with respect to the lattice matched device (104 mV/dec). Also, there is not much change in the ON current. The lower value of the strain induced subthreshold slope shows that the strained device exhibits a faster transition between the OFF and ON current states.

In order to have a quantitative digital analysis, the leakage current must be included with the OFF state current. The origin of the leakage current is impact ionization in regions of high electric field where carriers multiply. The impact ionization rate is much higher in the lattice matched device than the strained device. As impact ionization is dependent on the bandgap of the device, which changes with applied strain, the device becomes unreliable. Therefore, the device needs to undergo design iterations to optimize the energy gap for low leakage digital applications. This can be achieved by tuning the strain to more negative values which increases the bandgap and electron effective mass.

One of the most important manifestations of impact ionization is the bell shaped characteristics of the gate leakage current. Fig. 9 shows the commonly obtained bell shaped gate leakage characteristics at V_D = 0.5 V. The plot reveals the decrease of gate leakage current for the strained device due to increased band gap.

The plot of the maximum gate leakage current in Fig. 10 for the strained and lattice matched device also shows significant reduction in gate current.

The overall effect of gate leakage reduction is the improvement in the I_{ON}/I_{leak} figure of merit of the device. Here I_{leak} is defined as the average of the OFF state current and the gate leakage current [17].

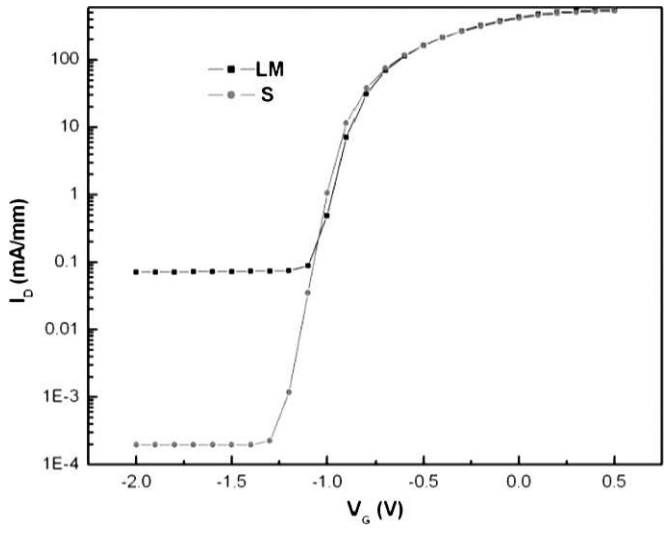

Fig. 8. Subthreshold characteristics of LM and S devices.

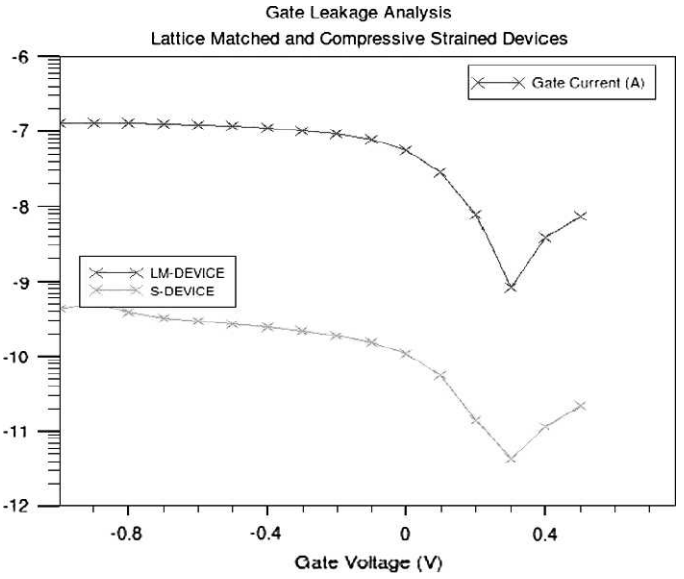

Fig. 9. Impact ionization gate current characteristics of LM and S devices.

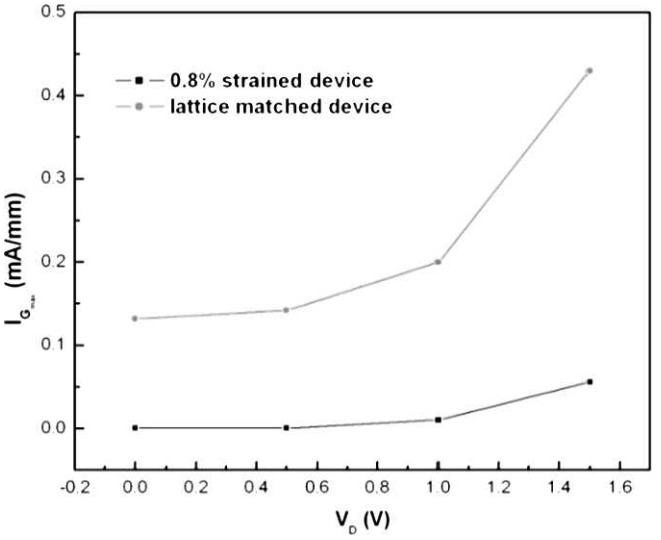

Fig. 10. Maximum gate current at different drain bias.

The simulation results of logic parameters are summarized in Table II.

The ON, OFF states and I_{ON}/I_{leak} ratio are highly relevant parameters of a digital device and show marked changes with strain. The device parameter variation as a result of strain plays a role in determining the overall reliability. Therefore, it is necessary to design the device taking strain into consideration, such that the effects of strain can be tuned for better performance and long-term reliability.

Table II
Summary of Extracted Parameters

Device type	V_T [V]	I_{ON}/I_{leak}	S [mV/dec]	V_{CC} [V]
LM	−0.80	1.24×10^3	104	0.5
S	−0.82	3.45×10^5	88	0.5

Conclusion

The effect of strain on the reliability of device performance is discussed in this work. Reliability issues occur as strain changes the semiconductor band structure and also produce defects. Since strain is unavoidable, it can be used as a design parameter for the device. This has been discussed using compressive strain which reduces the gate leakage current and the device can be used for low leakage applications. The strained device also shows improved subthreshold slope. Due to reduced electron mobility, the drive current is smaller than that of a lattice matched device. However, the overall digital performance of the device is improved.

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