Journal of Microelectronics and Electronic Packaging (2010) **7**, 125-130

ISSN: 1551-4897

Fabrication and Electrical Evaluation of Via Last Polymer Liner TSVs

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Abstract—**Imec is developing two TSV flavors for Si thicknesses of 50 and 100 μm for various wafer level packaging (WLP) applications where thin dice are stacked and electrically connected to each other through post CMOS processed TSVs and microbumps. As a differentiator, these TSV technologies use spin-on dielectric polymers as the insulating liner. A three-mask process sequence is implemented for fabrication of both TSV types; however, the TSV shape, the process flow, and the Si thickness are different for each one of them. All processes employed in the fabrication of the TSVs are performed at low temperature (<200°C) for post CMOS compatibility. For both TSV types, electrically yielding TSV connected daisy chains are measured on the fabricated wafers and the reliability of the TSVs while undergoing thermal cycle tests is analyzed.**

Keywords—**Through silicon via (TSV), 3D integration, wafer level packaging (WLP), polymer liner**

Introduction

The semiconductor industry has been urged to develop more innovative advanced packaging technologies due to ever-increasing demand for new and more advanced electronic products, with smaller form factor, superior functionality, and higher performance, while reducing the cost. 3D packaging, using through silicon via (TSV), and stacking through microbumps is probably the most promising concept that can successfully address the limitations of today's packaging technologies. 3D interconnect technologies can be realized at different levels of the interconnect hierarchy, allowing 3D stacks between wafers and die to produce multilevel systems integrating diverse CMOS and emerging technologies such as MEMS and III-V.

The TSV technologies described in this paper relate to bond pad level 3D integration using wafer level packaging techniques, 3D WLP [1]. Two 3D WLP TSV flavors with polymer insulating liners are described in this paper. Both are based on the thinning first, via last approach, where the 3D interconnects are implemented on the backside of the thinned device wafers. Key aspects of the TSV processes are firstly the fabrication of the TSV from the backside of the wafer and contacting to the bottom metal layer (Metal 1) of the back-end-of-line (BEOL) interconnect stack. The TSV approaches are therefore independent of the specific structure and materials used in the BEOL interconnect stack. The second key characteristic is the use of a thick polymer layer as a TSV liner, which is different from most traditional approaches that use thin CVD silicon oxide or nitride. Thick polymer liners significantly reduce TSV coupling capacitance, and hence improve the general electrical performance. Thick polymer isolation also absorbs some of the stress induced by the coefficient of thermal expansion (CTE) mismatch between the Cu in the via and the Si wafer.

This paper discusses the fabrication of the two 3D WLP TSV types, the electrical results of the TSV connected daisy chains, and the reliability of these TSVs while undergoing thermal cycle tests. A three-mask process sequence is implemented to fabricate the TSVs while the TSVs differ in shape and process sequence as a function of Si thickness. Independent of the chosen approach, the device wafers are mounted face down on a carrier using a temporary glue layer and thinned by grinding. For the TSV developed using 100 μm thick Si, a traditional TSV process is used where a chamfered cavity is etched in Si from the wafer backside with a bottom diameter of 70 μm and a top diameter of 100 μm to achieve a minimum target pitch of 160 μm. As the insulating liner, a special photo-sensitive spin-on dielectric is conformally coated in this chamfered TSV cavity. At the via bottom, a contact hole with 30 μm diameter is realized using the photolithography properties of the dielectric liner. A negative resist is used to define the pattern for metal deposition. Conformal electrochemically deposited (ECD) Cu is used to form the electrical connection between the wafer front and back. For the TSV developed using 50 μm thick Si, a different process sequence is used enabling a higher aspect ratio (AR) TSV where 5 μm wide ring trenches are etched through the Si and subsequently filled with a spin-on polymer dielectric. Center Si block is then dry etched and interconnects are realized by the bottom-up ECD Cu fill to form the TSV for target dimensions of 60 μm pitch and 35 μm TSV diameter. The advantages of this TSV using 50 μm thick Si are: (i) its scalability to smaller diameters or thicker substrates; and (ii) possibility to simultaneously plate tin (Sn) microbump on top of the Cu plug for immediate stacking on a landing die without the need for redistribution lines. Fig. 1 shows the schematic and the FIB cross-section pictures of the two fabricated polymer 3D WLP via last TSVs that are developed at imec. All processes employed in the fabrication of the TSVs are performed at low temperature (<200°C) for post CMOS compatibility.

Manuscript received August 2010 and accepted October 2010
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doi:10.4071/imaps.272

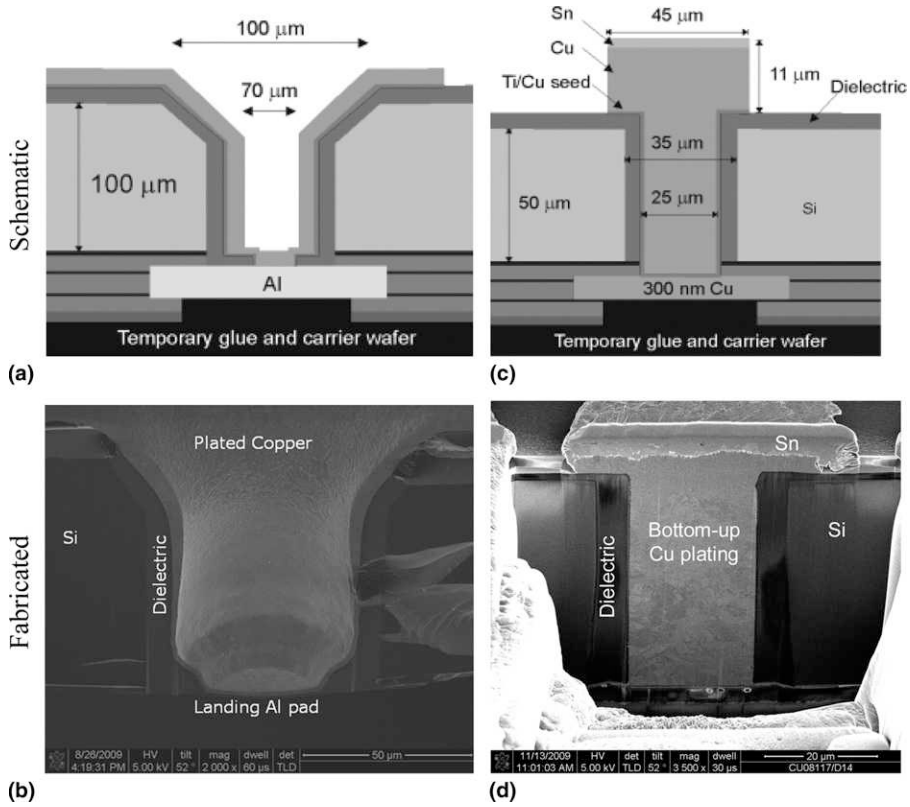

Fig. 1. Schematic and FIB cross section pictures of the two fabricated via last polymer liner TSVs for 3D WLP applications developed at Imec: (a, b) in 100 μm thick Si with conformal ECD Cu; and (c, d) in 50 μm thick Si with bottom-up filled ECD Cu.

A. Fabrication

1) TSV in 100 μm Thick Si with Conformal Polymer and ECD Cu

Fig. 2 shows the schematic process flow of the 100 μm TSV approach. The process flow has been performed at imec in clean-room facilities using 200 mm diameter Si wafers with a front side build up of 200 nm silicon oxide as premetal dielectric (PMD) and 1 μm patterned Al as the Metal 1 landing pad on the wafer front simulating a device wafer. The wafers are bonded face down on a carrier using a temporary glue material using the EV520 wafer level bonding tool by applying temperature and pressure in a controlled environment. Afterward, the wafers are thinned down to a Si thickness of 100 μm by mechanical grinding using the Disco DFG8560 tool with a total thickness variation (TTV) over a wafer of below 2 μm using both coarse and fine grinding to achieve high throughput and surface quality. The wafer stack is then cleaned to remove particles; and the surface damage after grinding is removed by wet and dry etch steps [Fig. 2(a)].

In order to pattern TSV cavity mask, 15 μm thick photoresist is spun and patterned on the ground wafer surface. The front to backside alignment strategy that can be applied at this point is determined by the type of carrier and the alignment tool capability. One can use CTE matched glass, for example, Pyrex, to do front to backside alignment. Since the device wafer is glued face down on a glass carrier, the alignment can be done looking through the glass to the front side of the wafer. This, however, is not a readily available feature in a standard contact mask aligner and, in our case, we used this special feature which was available in the IQ aligner from EVG. Glass, however, is not compatible with the high-end Si process environment due to its fragile, nonconductive, and (Na) contaminating nature. Therefore, it would be more fab friendly to use a Si carrier, which may mean that the aligner should have IR capability that is also an extra feature in most contact aligners. Still another alignment strategy would be to use the Si carrier and after thinning by grinding down to the required thickness, large cavities can be etched through the thinned Si up to the PMD layer on the position of the front side alignment marks. Then these opened marks can be used to align the TSV cavity litho to the front side structures by using the standard front side alignment procedure.

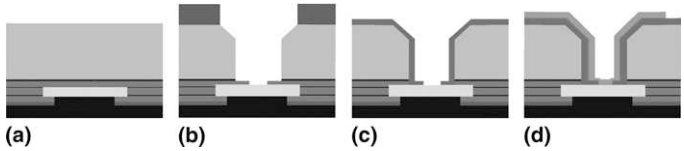

Fig. 2. Schematic process flow of the TSV in 100 μm thick Si with conformal ECD Cu: (a) device wafer is bonded face down on a carrier using temporary glue material and thinned down to 100 μm Si thickness, (b) chamfered TSV cavity is etched using photoresist as the mask, (c) photosensitive spin-on polymer dielectric is deposited as an insulating liner and patterned at the via bottom, and (d) Cu is conformally electroplated using a negative photoresist as the mask.

Once the TSV cavity litho is aligned from the wafer front to back using one of the procedures explained above, the TSV cavity is etched. In this 100 μm TSV approach, a traditional

TSV process is implemented with a modified TSV shape, which differentiates this process. This so-called chamfered shape is beneficial for the deposition of the spin-on dielectric layer in the subsequent step and it is done in two consecutive dry etch steps. First, the sloped cavity is formed using a photoresist mask with an isotropic silicon etching recipe adjusted to provide 60° sidewall and it consists of SF_6, C_4F_8, and O_2 gases. Second, straight vertical etching is done using the Bosch process-based anisotropic deep RIE (DRIE) recipe in the Adixen AMS 100SE tool. The final etching step is further optimized to avoid notching, a phenomenon that occurs when landing on a metal or a dielectric layer [Fig. 2(b)], which results in a negative corner at the via bottom, and hence imposes problems for the continuity of the subsequent layer deposition [2]. Fig. 3 shows this chamfered TSV cavity developed on blanket Si wafers where the via bottom diameter is 70 μm and the via top diameter is 100 μm with a target depth and minimum pitch of 100 μm and 160 μm, respectively.

In order to contact the Al Metal 1 pad on the wafer front, the silicon oxide PMD layer at the via bottom is dry etched. Then the photoresist is dry stripped, which also cleans the Si surface thoroughly and removes any Teflon-like polymer residues formed during the Si cavity and silicon oxide PMD etch sequence. As the dielectric liner, a special photosensitive spin-on polymer is conformally coated on the wafer. Initial process optimization showed that surface conditioning is a key parameter to have a conformal coating of this polymer on the sidewalls of the TSV cavity; and the coating quality is independent of the TSV pitch. At the via bottom, a contact hole with approximately 30 μm diameter is realized by photo patterning and an ultrasound assisted development step [Fig. 2(c)]. The limitation in scaling the diameter of this TSV type comes from the dielectric liner process. The cavity bottom should be large enough: (i) to have a uniform polymer layer at the via bottom, and (ii) to make a decent large gap litho (proximity ≈ TSV depth). Hence, the scalability of this TSV to smaller dimensions is limited. Fig. 4 shows this special photosensitive spin-on polymer litho development on blanket Si wafers where conformal coverage of the polymer and successful patterning of 30 μm diameter opening at the via bottom is seen. In the next step, a relatively thick Ti/Cu seed layer, of thickness 70 nm and 500 nm, respectively, is formed by PVD. Seed layer continuity, which is crucial for the subsequent conformal Cu electroplating step, is typically an issue for high AR TSVs. By multiple SEM cross-section measurements, the continuity of the seed layer is verified and reported, as shown in Fig. 5.

Next, conformal ECD Cu is used as TSV metallization using thick negative plating photoresist as the mask layer. Negative photoresist is preferred since only exposure on the wafer surface is required, and not in the TSV cavity, which would introduce nonuniform exposure of the photoresist due to resist thickness variation and the large proximity [3]. The electroplating is done in two steps. First, a low current density is applied to have a gradual deposition to enhance the Cu seed layer on the sidewalls. Second, a higher current density is used to do the bulk of the Cu interconnect and the routing lines. After the plating, the photoresist is removed and the seed layer is wet etched to complete TSV processing. Fig. 1(a) shows the schematic and Fig. 1(b) shows the FIB cross section of the fabricated TSV for 100 μm thick Si. Further processing using additional masks may consist of applying a second layer of the

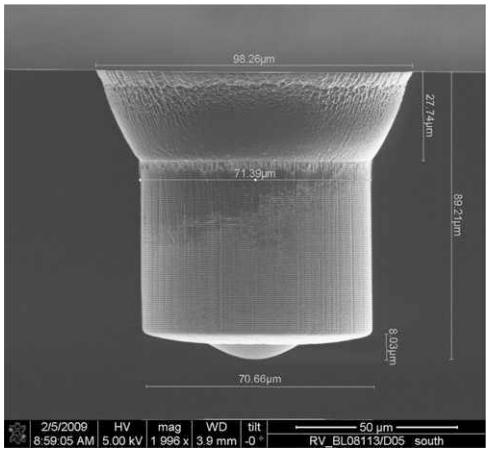

Fig. 3. Chamfered TSV cavity developed on blanket Si wafers: via bottom diameter is 70 μm and via top diameter is 100 μm.

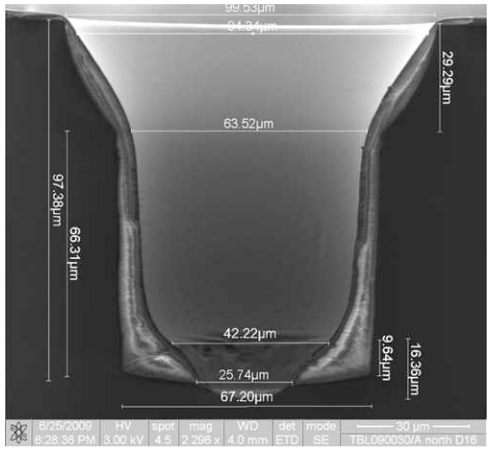

Fig. 4. Photosensitive spin-on polymer development on blanket Si wafers: conformal coating and patterning at the via bottom.

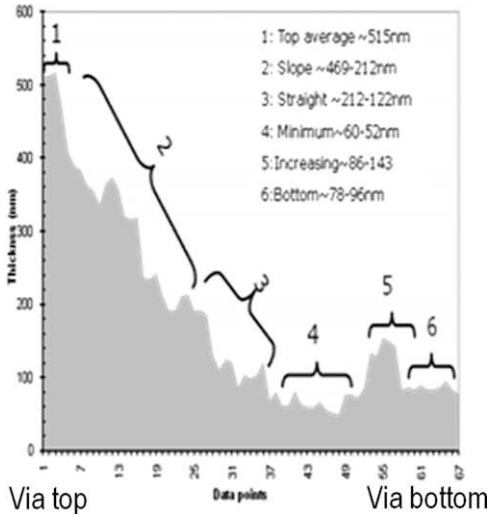

Fig. 5. Continuity of the Ti/Cu seed layer, which is required for conformal Cu plating, is verified by multiple SEM cross sections.

same spin-on dielectric layer as the passivation layer, and processing of flip chip bumps or UBM pads, making this process similar to WLP flip chip and CSP technologies.

2) TSV in 50 μm Thick Si with Bottom up Filled ECD Cu [4]

Knowing the scaling limitation of the 100 μm TSV, a different process sequence is used for the 50 μm approach that enables a higher AR TSV. Fig. 6 shows the schematic process flow of the 50 μm TSV approach. First, 5 μm wide ring shaped trenches are patterned on the wafer backside and etched through the Si substrate up to the PMD layer using a Bosch process-based DRIE recipe in the Adixen AMS 100SE tool [Fig. 6(a)]. The trenches are then filled with a spin-on polymer dielectric material [Fig. 6(b)]. Several polymers from different suppliers have been screened for filling of the ring trenches having an AR of 10 [5]. Experiments show that a low viscosity material performs better in achieving a void free filling of the ring isolation trenches. Throughout the TSV process, two viscosity versions of the same polymer material are used. First, the low viscosity version is used to fill the ring trenches, and then the polymer on the surface is etched back to expose Si. Second the higher viscosity version is used to cover the Si backside and patterned to open the central Si cores of the ring-shaped TSV structures. Here, the dielectric liner is used as a negative-tone hard mask to expose the TSV Si core and allow for Si core etching using a second Si DRIE sequence [Fig. 6(c)]. The PMD stack, which is exposed at the via bottom, is then wet etched in dilute HF to contact the Metal 1 layer of the BEOL stack. Here, the Metal 1 layer was a Cu layer instead of Al, and hence compatible with HF; and we chose the wet etch method mainly due to difficulties experienced in dry etching dielectric layers at the bottom of a 50 μm deep 25 μm diameter TSV cavity (e.g., extremely reduced etch rate).

In the next step, the Ti/Cu seed layer is deposited by PVD on the AR 2:1 TSV core surface. The target dimension of this TSV is currently limited by the PVD deposition step due to tool capabilities. The tool used for PVD seed layer deposition has an aspect ratio limitation of 2.3:1. Other tools can be used to scale this TSV structure to higher AR. In other words, the process sequence is applicable to smaller TSV diameters and/or thicker substrates, and hence is scalable. Another way to enhance the AR of the TSV is to apply a seed repair step between seed deposition and plating. We have investigated seed repair using electroless Nickel (e-less Ni) plating as a solution to increase the AR of the conformal seed layer. Experiments have shown that repair of the as-sputtered seed is possible for AR 3.3 (i.e., the TSV inner diameter, or Cu plug, of 15 μm). Fig. 7 shows two examples of the different conditions that are used during the development of the e-less Ni seed repair procedure on a blanket Si wafer with 15 μm diameter 50 μm deep TSV cavities. In Fig. 7(a), a 2 min HCl dip is followed by a 2 min activation of the Cu surface with $PdCl_2$ solution and a 30 s e-less Ni plating; nucleation sites at the via bottom are visible, but conformal seed repair could not be achieved. While in Fig. 7(b) HCl dip is not performed so that the limited Cu sites at the via bottom are not etched away and a longer, 450 s, of e-less Ni plating is performed resulting in conformal seed repair.

Next, a thick negative plating resist mask layer is applied before the bottom-up ECD Cu process, allowing the simultaneous formation of the Cu filled TSV and the Cu/Sn microbump on top for immediate stacking on a landing die [6]. After stripping the electroplating photoresist, the metallic seed layer is removed by wet etch [Fig. 6(d)]. Fig. 1(c) shows the schematic and Fig. 1(d) shows the FIB cross section of the fabricated TSV that uses spin-on polymer and bottom-up Cu fill in 50 μm thick Si wafer. Fig. 8 shows the FIB cross section detail of the TSV in 50 μm thick Si where e-less Ni seed repair is implemented.

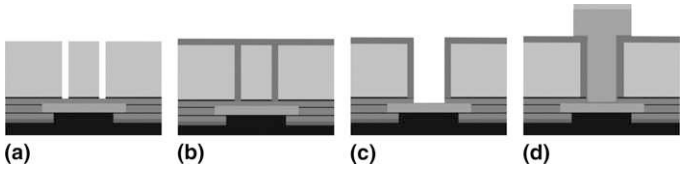

Fig. 6. Schematic process flow of the TSV in 50 μm thick Si with bottom-up filled ECD Cu: (a) 5 μm wide ring trenches are etched on the wafer backside, (b) trenches are filled with the spin-on polymer dielectric material, (c) Si core is etched using the dielectric polymer as hard mask, and (d) TSV core is filled by bottom-up ECD Cu and the Cu/Sn microbump is formed on top.

Results

The test vehicle used to develop the TSV technologies includes TSV daisy chains of various lengths connecting a

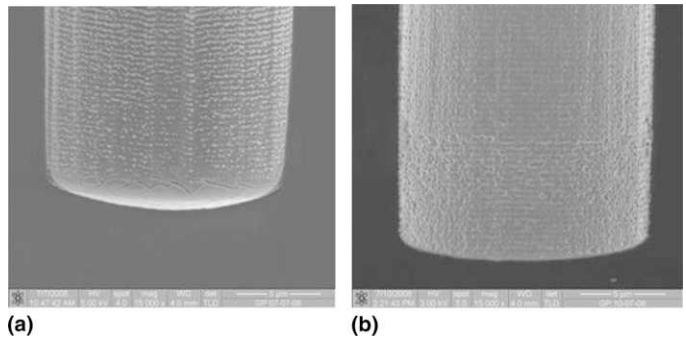

Fig. 7. Two different conditions for seed repair: (a) 2 min HCl dip followed by 2 min activation of Cu surface with $PdCl_2$ solution and 30 s e-less Ni plating; nucleation sites at the via bottom are visible but not conformal; (b) no HCl dip and 450 s e-less Ni plating, conformal seed repair is achieved.

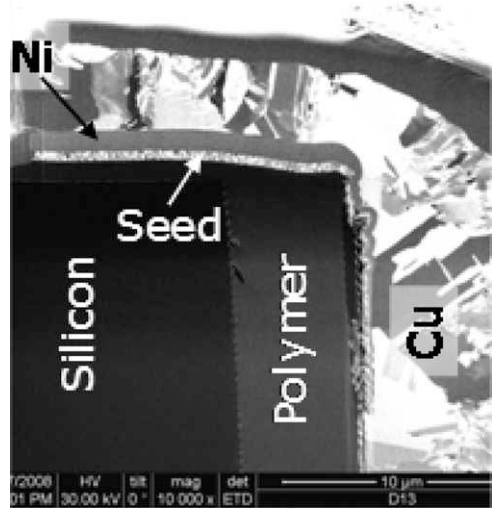

Fig. 8. FIB cross section detail of the TSV in 50 μm thick Si where e-less Ni seed repair is applied.

different number of TSVs to determine the TSV yield and the resistivity. For both TSV approaches, the yield is estimated by measuring DC continuity of daisy chains on fabricated TSV wafers. For the 100 µm thick chamfered TSV approach, TSVs with different pitches ranging from 160-400 µm are measured. Fig. 9 shows the daisy chain element resistance (one TSV resistance including the routing lines) measured for different pitches. The electrical measurements show that up to 90% electrical yield is achieved on the TSV wafers depending on the daisy chain pitch. Single TSV resistance excluding the routing lines is measured through Kelvin structures and is found to be ~4-20 mΩ (Fig. 14). Electrically yielding dice are further subjected to up to 1000 thermal cycles from –40 to +125°C, and the results show limited yield loss (Fig. 10).

For the 50 µm TSV approach, different length daisy chains with only 60 µm TSV pitch were designed and measured. Up to 95% electrical yield is achieved on the fabricated wafers [7]. For this type of TSV, since the Sn bump is directly plated on the TSV, the wafers are further diced after TSV processing and flip chip bonded to a landing die by transient liquid phase (TLP) bonding through Cu/Sn microbumps as shown in Fig. 11 [6]. Fig. 12 shows the daisy chain element resistance obtained from the measurements of daisy chains composed of 15 and 32 TSVs in series. The single TSV resistance is measured to be 10-15 mΩ on bonded stacks through Kelvin structures (Fig. 14). Since Kelvin structures are measured after 3D stacking, the TSV resistance shown in Fig. 14 includes the Cu/Sn intermetallic connection for this TSV. Thermal cycling of TSV dice was also done, and after 1000 thermal cycles, no electrical failure was observed, that is, both the daisy chain resistance and the leakage current between the interlaced chains remained unchanged (Fig. 13).

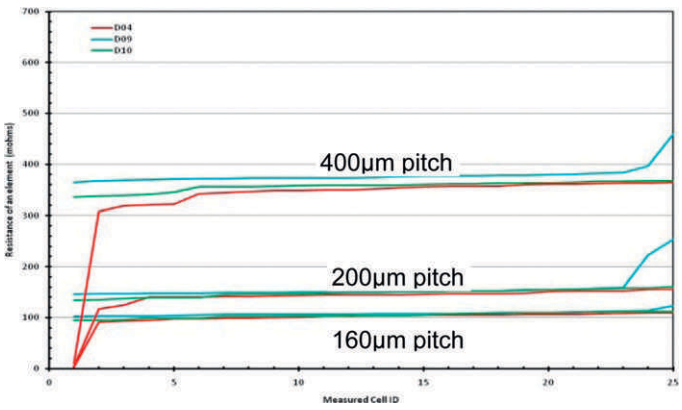

Fig. 9. Daisy chain element resistance (one TSV resistance including the routing lines) measured for different pitches on 100 µm TSV wafer.

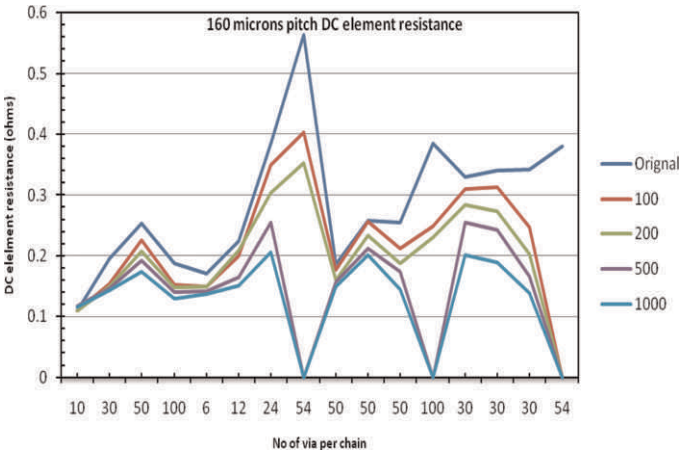

Fig. 10. Electrically yielding dice on 100 µm TSV wafer are subjected to up to 1000 thermal cycling from –40 to +125°C and the results show limited yield loss.

Conclusion

Two types of 3D WLP TSVs using spin-on applied dielectric polymers as liner isolation in 50 or 100 µm thick Si wafers are fabricated based on thinning first, via last approach, where 3D interconnects are implemented on the backside of thinned

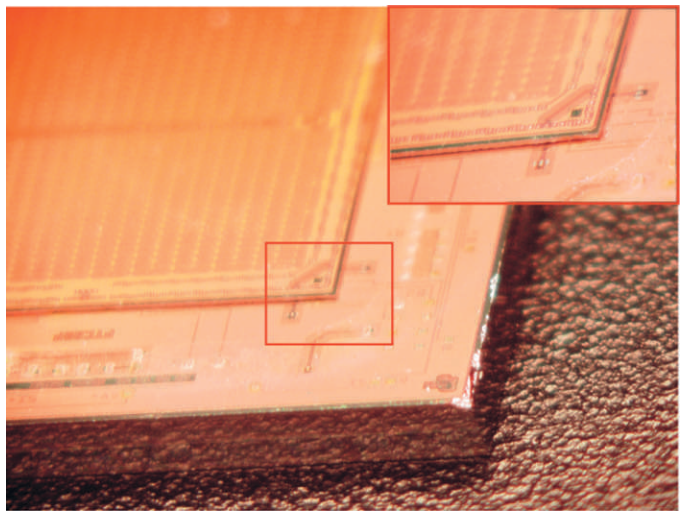

Fig. 11. 3D image of the bonded stack for 50 µm TSV using spin-on polymer liner and bottom-up Cu fill. Inset shows the bonded 50 µm thin TSV die.

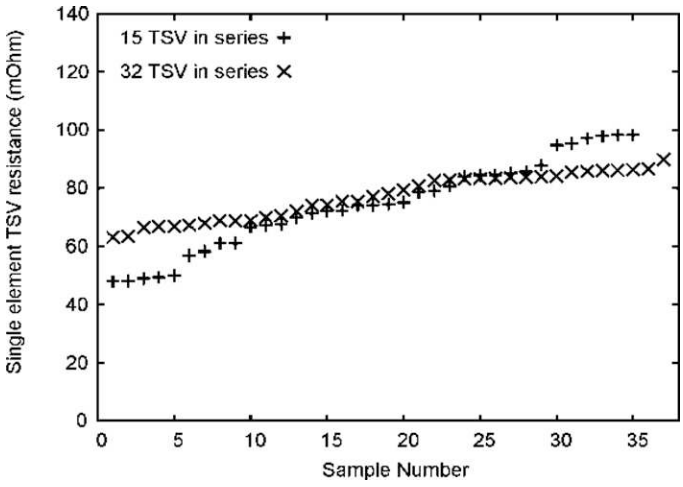

Fig. 12. Daisy chain element resistance for 50 µm TSV using spin-on polymer liner and bottom-up Cu fill, which includes the central Cu plug and top and bottom routing lines, obtained from the measurement of daisy chains composed of 15 and 32 TSVs in series.

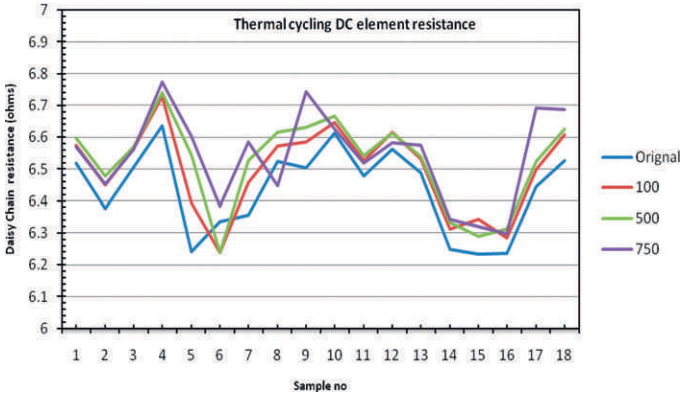

Fig. 13. Thermal cycling of 50 µm TSV dice; after 1000 thermal cycles, no electrical failure is observed.

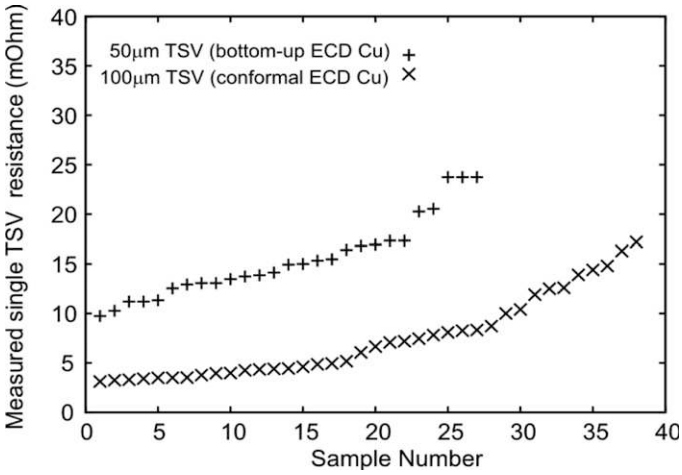

Fig. 14. Single TSV resistance measured through Kelvin structures for 50 and 100 µm TSV.

IC fabricated device wafers. Table I summarizes the key aspects of the two TSV approaches.

In short, a three-mask process sequence is implemented for fabrication of all TSV types, however, the TSV shape, the process flow, and the Si thickness are different for each one of them. For the 100 µm thick Si TSV approach, a traditional TSV process is implemented with low AR and low density; the target dimensions are 100 µm via top and 70 µm via bottom diameter. For the higher AR and higher density, 50 µm thick Si TSV approach, the target dimensions are 60 µm pitch and 35 µm TSV diameter. All processes employed in the fabrication of the TSVs are performed at low temperature (<200°C) for post CMOS compatibility.

The test vehicle used to develop the TSV technologies include daisy chains of various lengths connecting different numbers of TSVs to determine the TSV resistance and yield.

Table I
Summary of the TSV Specifications

	TSV in 100 µm Si	TSV in 50 µm Si [4]
Si thickness	100 µm	50 µm
TSV Ø (µm)	70/100	35
TSV pitch (µm)	>160 µm	60 µm
Electroplated Cu	Conformal	Bottom-up
Dielectric liner	Conformal coated spin-on polymer	Spin-on polymer filling
Measured TSV resistance	5-20 mΩ	10-15 mΩ
Wafer yield	<90%	<95%
Yield after 1000 thermal cycles	Limited yield loss	No yield loss

A high yield of TSV connectivity is achieved for both TSV types. The resistance of a single TSV in the 100 µm thick flow is 4-20 mΩ, and for the 50 µm thick flow the resistance is 10-15 mΩ. Thermal cycling from –40°C to +125°C of TSV dice are also done for both TSV types; and after 1000 thermal cycles no or limited electrical failure is observed.

Acknowledgment

The authors thank the 3D team for their contributions.

References

[1] E. Beyne, P. De Moor, W. Ruythooren, R. Labie, A. Jourdain, H. Tilmans, D.S. Tezcan, P. Soussan, B. Swinnen, and R. Cartuyvels, "Through-silicon via and die stacking technologies for microsystems-integration," in IEEE Technical Digest of International Electron Devices Meeting, pp. 1-4 (2008).

[2] B. Majeed, M. Van Cauwenberghe, D.S. Tezcan, and P. Soussan, "Failure analysis and process improvement for through silicon via interconnects," in Proceedings of the Materials Research Society (MRS) Symposium, p. 1156 (2009).

[3] N.P. Pham, D.S. Tezcan, B. Majeed, P. De Moor, K. Baert, B. Swinnen, and W. Ruythooren, "Lithography for patterning inside through-Si vias," in Proceedings of the Electronic Components Technology Conference (ECTC), pp. 120-124 (2007).

[4] D.S. Tezcan, F. Duval, H. Philipsen, O. Luhn, P. Soussan, and B. Swinnen, "Scalable through silicon via with polymer deep trench isolation for 3D wafer level packaging," in Proceedings of the Electronic Components and Technology Conference (ECTC), pp. 1159-1164 (2009).

[5] F. Duval, D.S. Tezcan, B. Swinnen and P. Soussan, "Polymer deep trench filling for through silicon via technology," in Proceedings of the 13th Meeting of the Symposium on Polymers for Microelectronics (2008).

[6] R. Agarwal, W. Zhang, P. Limaye and W. Ruythooren, , "High density Cu-Sn TLP bonding for 3D integration," in Proceedings of the Electronic Components Technology Conference (ECTC), pp. 345-349 (2009).

[7] Y. Civale, D.S. Tezcan, H.G.G. Philipsen, P. Jaenen, R. Agarwal, F. Duval, P. Soussan, Y. Travaly, and E. Beyne, "Die stacking using 3D-wafer level packaging copper/polymer through-Si via technology and Cu/Sn interconnect bumping," in Proceedings of the IEEE International Conference on 3D System Integration (3DIC), pp. 1-4 (2009).