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Development and Characterization of Tapered Silicon Etch Process by Topography Modeling for TSV Application

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***Abstract*—A dual-etch via tapering technology has been presented which combines Bosch process and isotropic etch process. It has been shown that the dual-etch process technology provides a high degree of process flexibility to the user by independently controlling and optimizing the etch rate and profile tapering process. Based on experimental work, RIE process models have been set up using ELITE simulation software from Silvaco. Detailed DOE has been done to optimize the RIE models so that the experimental and simulation results match over a wide range of via geometries and aspect ratios. The optimized models have been further used to predict the aspect ratio induced RIE lag effects.**

***Keywords*—Topography modeling, TSV, DRIE, tapered profile, isotropic etch**

Introduction

As microfabrication technology becomes more complex with the increase in the number of processing steps, modeling of the surface topography evolution becomes increasingly important for predicting the performance of the technology [1]. Simulation also allows accurate prediction and optimization of the performance of a part or whole of the process technology with changing dimensions and materials, without the need to make any expensive prototype. Surface topography affects the performance of photolithography and etching steps, both of which are universal and critical in the microfabrication technology. As the feature size becomes smaller, the surface topography variations and its impact on lithography and etch gain greater significance [2]. Whatever be the physical details, the etching process can in many cases be modeled as a series of surface etching phenomena. Etch process simulation starts from an initial profile that moves through a medium in which the speed of etching propagates as a function of position and other variables that determine the final profile. The following simulation tools are commonly used for etch process simulation and modeling.

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- SPEEDIE, a 2D simulator from Stanford University based on physical models for deposition and etching [3, 4]
- SAMPLE, from University of California [4, 5]
- ELITE, a topography simulation tool from Silvaco [6, 7]
- VICTORY, 3D etch simulation software recently developed by Silvaco [8]
- RECIPE, a 2D and 3D DRIE etch process simulation tool developed by Intellisense [9, 10]
- TRAVIT, an analog process simulator supplied by Abeamtech [11].

The study presented here focuses on deep silicon via etch topography modeling with an Athena Elite simulation tool. Following an overview of the reactive ion etch (RIE) process modeling and its use in simulating deep silicon via etch profile for TSV application, experimental characterization work has been done for a tapered silicon etching process developed in the ICP DRIE system of Surface Technology System. Trenches of width varying from 10-100 μm have been experimentally characterized and subsequently modeled by using Elite. The objective of this study is to demonstrate that experimental and simulation results can be correlated well and that they can be used in making further predictions on profile evolution as a function of process time.

Topography Simulation with Athena Elite

Athena is a high level simulation platform provided by Silvaco which integrates several process simulation modules in an interactive and user-friendly environment. Various etch process modes are modeled by defining a machine and invoking the machine to perform the required etch. Elite is a 2D topography simulator for modeling physical etching and deposition by using a string algorithm to describe topographical changes that occur during etching processes. Jewett et al. were among the pioneers who attempted to model the surface advancement by string algorithm [12, 13], wherein the surface is approximated by a series of points joined by straight line segments forming a string as shown in Fig. 1. The string algorithm approximates the etched surfaces as a string of a joined set of points formed in response to a particular process condition. During the simulation, the segments joining adjacent points are kept roughly equal in length by adding points in regions of expansion of the front, and by deleting points in regions of contraction. Elite links the string to simulation

grinds such that during etching the simulation cuts into the grid patterns as the etch advances.

Elite provides a set of basic etch models corresponding to different etch mechanisms. Any one of these models can be selected to define a machine that can then be invoked to perform processing on the structure by using a series of statements [14]. There are two isotropic etch models in Elite. The WET.ETCH parameter in the RATE.ETCH statement specifies isotropic wet chemical etch. In wet etching, the reactive precursors chemically react with the exposed surface in all directions. Another isotropic etch model is invoked by using parameter RIE in the RATE.ETCH statement. Note that in RIE mode, the isotropic etch is coupled with physical etch. In the RIE model, the etching process consists of both isotropic and physical etch. The RIE etch model is built in the RATE.ETCH statement defined by the RIE parameters, isotropic, directional, chemical, and divergence. Hence, we can model ion milling (physical etching), isotropic etching (chemical etching) and beam divergence models, which emulate the effect of angular incidence of reactive ion flux. Therefore, the divergence parameter can be specified only if a nonzero value of chemical etch rate is specified as the divergence of beam always results in some degree of lateral etch. Fig. 2 shows a typical example of the modeling of the tapered etch process by using some of the statements shown in Table I.

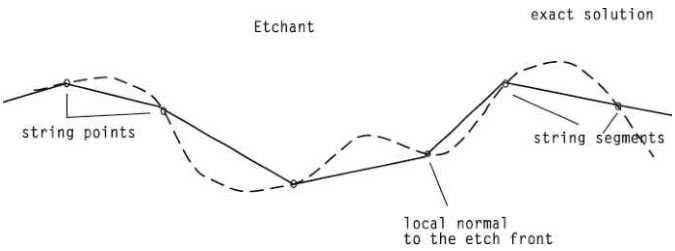
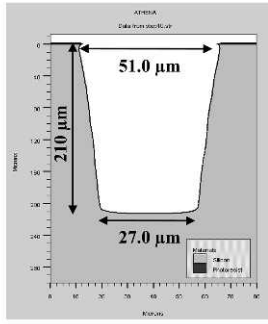
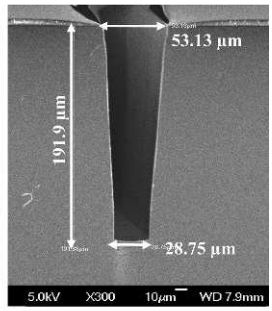


Fig. 1. String odel approximation to model the etch front [14].

```
go athena
# X-Grid definition
line x loc=0.00 spac=10.00
line x loc=10 spac=1.0
line x loc=20 spac=1.0
line x loc=30 spac=0.50
line x loc=50 spac=0.50
line x loc=60 spac=1.0
line x loc=70 spac=1.0
line x loc=80 spac=10
# Y-Grid definition
line y loc=0.00 spac=0.50
line y loc=50 spac=0.50
line y loc=300.0  spac=2.0
# Define substrate
initialize silicon orientation=100
# Photoresist mask patterning
deposit material=photoresist  thick=13.0 divis=13
etch material=photoresist start x=30.0 y=-13
etch                cont  x=30.0 y=0
etch                cont  x=47.0 y=0
etch                done  x=47.0 y=-13
structure outfile=step0.str
# DRIE etch process
rate.etch machine=STS-DRIE rie silicon u.m iso=0.36
dir=3.88 chemical=0.1 divergence=50
rate.etch machine=STS-DRIE rie material=photoresist
u.m iso=0.14 dir=0 chemical=0.1 divergence=100
etch machine=STS-DRIE time=50 minutes dx.mult=1
structure outfile=step10.str
# Print simulation results
tonyplot -st step*.str
quit
```



Simulated tapered etch profile



Experimental results of actual tapered etch profile

Fig. 2. Simulation f tapered deep silicon etch process using the isotropic and RIE etch models. SEM image shows the experimental result. Note that the scale of the *x*-axis is different from the *y*-axis of the simulation result.

Experimental Characterization of Dual-Etch Tapered Silicon Etch Process

A. Conceptual Approach

The dual-etch technology consists of two silicon etching steps. The first etch step consists of a high etch-rate process to form deep silicon vias of the required depth followed by photoresist stripping and post-etch polymer removal process. The second etch step consists of a maskless global isotropic etch process which results in a widening of the top of the vias/trenches more than the bottom to form a graded or tapered etch profile. The first etching step is designed to provide a high anisotropic etch rate and throughput, while the second etch step is designed to provide a high isotropic etch rate. The main advantage of this approach is that it helps in maintaining high overall etch rates and still tailor the required via profile. Fig. 3 shows step by step how the tapering can be achieved. While the isotropic etch process helps in tapering or flaring the via, it also helps in removing or rounding off some of the surface defects such as microcracks formed during the wafer thinning

Table I
Summary of Important Athena Elite Statements

Statements	Descriptions
Go Athena	GO ATHENA starts the simulation program
Line x	
Line y	LINE specifies a mesh line during grid definition
Initialize	INITIALIZE specifies the initial starting material and background doping levels and crystal orientation
Deposit	DEPOSIT deposits a layer of specified material
Etch	ETCH simulates an etch process
Rate.etch	RATE.ETCH specifies the etch rate parameters for a machine, which is used in a subsequent ETCH statement
Structure Infile	STRUCTURE writes the mesh and solution information. INFILE specifies the name of the section file generated during simulation
Structure Outfile	OUTFILE specifies the name of the file to be written
Tonyplot	Tonyplot starts the graphical postprocessor TONYPLOT
Quit	QUIT terminates execution of ATHENA

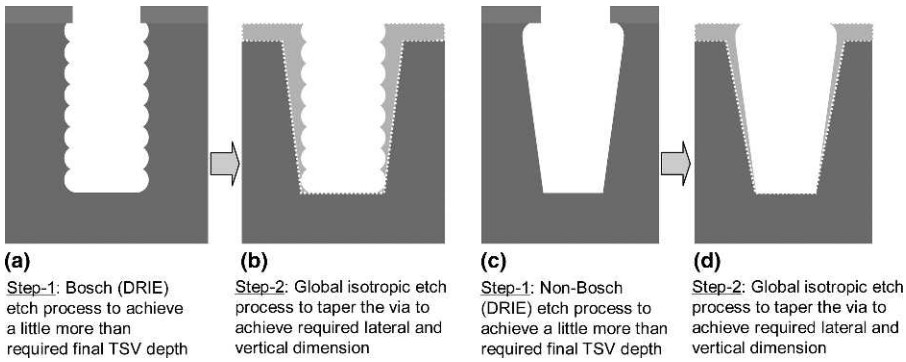


Fig. 3. Conceptual approach of silicon via tapering process with Bosch and non-Bosch etch process as first step and global isotropic etch process as second step. Note that the profile looks similar after the second etch step.

Table II
Etch Rate Characterization Results of Bosch Etch Process

Trench width (μm)	Top width (μm)	Bottom width (μm)	Trench depth (μm)	Aspect ratio	Etch rate (μm/min)	RIE lag (μm)
10	21.6	22.0	262.0	12.0	2.2	
20	29.5	30.9	291.1	9.6	2.4	29.10
30	39.8	42.2	307.0	7.5	2.6	15.90
40	50.2	51.1	317.8	6.3	2.6	10.80
50	60.9	65.2	323.4	5.1	2.7	5.60
60	70.3	75.0	328.1	4.5	2.7	4.70
70	79.2	85.3	335.6	4.1	2.8	7.50
80	89.5	95.6	336.6	3.6	2.8	1.00
90	100.3	105.5	339.4	3.3	2.8	2.80
100	108.8	116.7	345.5	3.1	2.9	6.10

Increasing RIE Lag

Bosch etch process		
Etch parameters	Etch	Pass
C_4F_8 (sccm)	0	110
SF_8 (sccm)	130	0
O_2 (sccm)	13	0
Argon (sccm)	0	0
Cycle time (sec)	8	5
Coil power (W)	600	600
Platen power (W)	23	0
Pressure (mtorr)	27-29	16-18
Total process time (min)	115	

process [15, 16] which precedes the TSV etch process in via-last 3D integration technologies [17, 18].

B. Experimental Characterization

In this work, a standard Bosch process, summarized in Table II, has been used to demonstrate the via tapering technology described in Fig. 3. The dual-etch process consisting of Bosch and global isotropic etch process has been characterized in great detail for trench/via width from 10-100 μm and for different aspect ratios. The plasma etch reaction and fundamental etching mechanism responsible for these processes have also been discussed. The experimental results obtained are used to set up simulation models to match the experimental and simulation results.

1. Characterization of First Etch Step by Bosch Process

The Bosch etch process is based on independent control of short isotropic etch and sidewall passivation chemistries based on $SF_6 + O_2$ and C_4F_8 plasmas. As a consequence, it is capable of a high degree of anisotropicity and high etch rate. However, an increase in etch rate results in increased sidewall scallops and reentrant profile due to the isotropic nature of SF_6 based etch chemistry. The etch mechanism due to mixture of SF_6 and O_2 gases can be explained as follows

$$SF_6 + e^- \rightarrow S_xF_y^+ + S_xF_y^* + F^* + e^-(\text{generic reaction})[19] \quad (1)$$

$$SF_6 + e^- \rightarrow SF_5^+ + SF_5^* + F^* + e^- \ (\text{dominant reaction})[20] \quad (2)$$

$$O_2 + e^- \rightarrow O^+ + O^* + 2e^- \quad (3)$$

$$Si(\text{from surface}) + xO^* \rightarrow SiO_x(\text{surface passivation}) \quad (4)$$

$$SiO_x + yF^* \rightarrow SiO_xF_y(\text{surface Passivation})[21] \quad (5)$$

$$Si(\text{surface}) + 4F^*(\text{free radical in plasma}) \rightarrow SiF_4(\text{gas}) \quad (6)$$

$$S + O_2 \rightarrow SO_2(\text{gas}) \quad (7)$$

where S_xF_y*, F*, and O* represent neutral species coming from the plasma reaction.

In the etch cycle of the Bosch process, SF_6 dissociates into atomic fluorine (F) and heavy SF_5^+ ions as shown in eqs. (1) and (2). Silicon is then subsequently etched by the F-radicals according to the final reaction in eq. (6). During the passivation phase of the Bosch process, CF_2 is formed from C_4F_8, as shown in eq. (8)

$$C_4F_8 + e^- \rightarrow C_3F_6 + CF_2 + e \quad (8)$$

The CF_2 shown above then adsorbs on the surfaces and forms a Teflon-like polymer shown in eq. (9)

$$nCF_2 \rightarrow (CF_2)_n \quad (9)$$

The sidewall passivation layer $(CF_2)_n$ and SiO_xF_y are deposited by the reactions in eqs. (9) and (5) during the passivation and etch cycles, respectively. During the etch phase, these two inhibiting layers are removed by a combination of physical ion sputtering [eq. (2)] and chemical reactions [eq. (6)]. The physical component in the Bosch process is contributed by positively charged SF_5^+ and the chemical etch is mainly due to F and O_2 which are generated from etch step. The scallops shown in Fig. 3(a) are due to the isotropic etching reactions from eqs. (1) and (6). Fig. 3(b) shows that after the second etching step or the global isotropic etching step, the scallops are effectively removed to form smoother sidewalls. Hence, scallops can be tolerated in the first etching step in the dual-etch process.

Table II and Fig. 4 shows some cross-sectional results after the Bosch etch process for vias and trenches of width ranging from 10-100 μm and depth in the range of 250-350 μm. Figs. 5(a) and (b) show the plot of etch depth, etch rate, and RIE lag as a function of varying trench diameter from 10-100 μm. RIE lag has been measured as the difference in etch depth between adjacent trenches as the trench width is varied by increment of 10 μm.

2. Characterization of Second Etching Step by Global Isotropic Etch Process

The objective of the second etch process is to taper the profile of the TSV structure. This is accomplished by an isotropic etch chemistry which is rich in free radicals as shown in eq. (1). Fig. 3 illustrates the fundamental mechanism responsible for the tapering of the silicon trenches and vias. The second etch step is a non-Bosch etch process which uses SF_6 and O_2 in an unswitched mode in the ICP system. Instead of using C_4F_8 as the passivation precursor, O_2 has been used as it leads to less accumulation of polymers and also allows more F-radicals to be available to etch silicon at a higher rate. The ratio of SF_6 to O_2 is therefore crucial to maintain a good balance between silicon etching with F-radicals and sidewall passivation with the inhibiting layer SiO_xF_y to maintain a good via or trench profile [21, 22]. However, as the via depth or aspect ratio increases, the reaction becomes more diffusion limited by

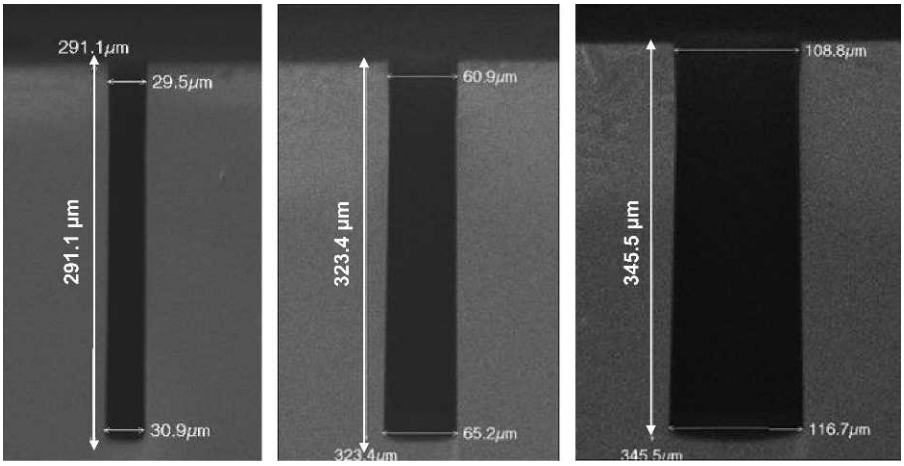


Fig. 4. SEM cross sectional micrographs of trenches of three typical widths and corresponding depths after etching with the Bosch process. A detailed summary of width and depth for different dimensions of the trenches are shown in Table II.

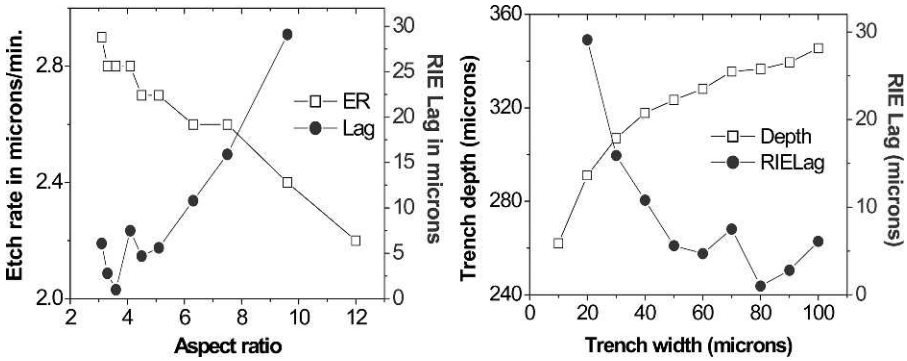


Fig. 5. Plots of etch rate, etch depth, and RIE lag with variation of trench/via width from 10-100 μm using the Bosch etch process. The aspect ratio decreases with increasing trench width and the RIE lag shows a decreasing trend while the etch rate increases and eventually flattens.

F-radical which is confined only to the top as its diffusion is limited with depth and width of the trench opening. The RIE etch mechanism can be modeled based on three etch components as explained by Volland et al. [23].

Etch rate (R_{Si}) = Isotropic rate R_{iso} + Anisotropic rate (R_{aniso}) − Passivation etch rate (R_p)

$$R_{Si} = \eta_F \Phi_F + K_e \Phi_i - R_p \quad (10)$$

where

η_F = Reaction rate coefficient of fluorine radicals (F)
Φ_F = Fluorine radical flux or neutral flux
Φ_i = Ion flux
K_e = Reaction rate enhancement coefficient

$$\eta_F = K_0 \exp\left(\frac{-E_a}{k_B T}\right)[23] \quad (11)$$

E_a = Activation energy of F-Si reaction
K_0 = Constant
k_B = Boltzmann's constant

In the second etch process (global isotropic etch), the isotropic etch (R_{iso}) process dominates over the anisotropic etch process (R_{aniso}) [refer to eqs. (10) and (11)]. As no sidewall passivation process takes place, R_p in eq. (10) is ≈0. The tapering process therefore requires enhanced chemical etching with radical/neutral flux (Φ_F) to flare the via at the top. Some amount of ion flux also helps by ion-assisted tapered sidewall etching and by pushing radical flux further down the trench/vias through inelastic collisions. The ion flux is controlled by platen power which also contributes to profile flaring without etching at the bottom. This ion-angular etch function is taken care of by chemical and divergence parameters in the Elite RIE model (see the previous section, Topography Simulation with Athena Elite). Fig. 6 shows SEM images taken after performing the dual-etch process shown in Table III. The tapered etch results achieved for 10-100 μm wide trenches have been used to develop appropriate simulation models and match the experimental results with simulation results.

Topography Modeling of Dual-Etch Via Tapering Process

A. Approach

The topography simulation of dual-etch via tapering process is done by modeling the first and second etch steps independently and then combining them as in a dual-etch process. The first etch step is defined by a geometric etch model to represent the Bosch process with vertical profile. The second etch step is modeled by varying the three RIE model parameters, divergence, chemical, and isotropic etch. The directional etch term has been set to zero as it is not capable of simulating the dependence of the lateral and vertical etch rate due to the size of the trench/vias. Design of experiments (DOE) was done to determine the optimum RIE model parameter that matches the experimental results, as explained in the next section.

B. Model Parameter Optimization by Design of Experiments

A two-level three-factorial design of experiments (DOE) was done with DOE software Design Expert-6 from Stat-Ease [24]. Nine experimental runs were designed based on the three

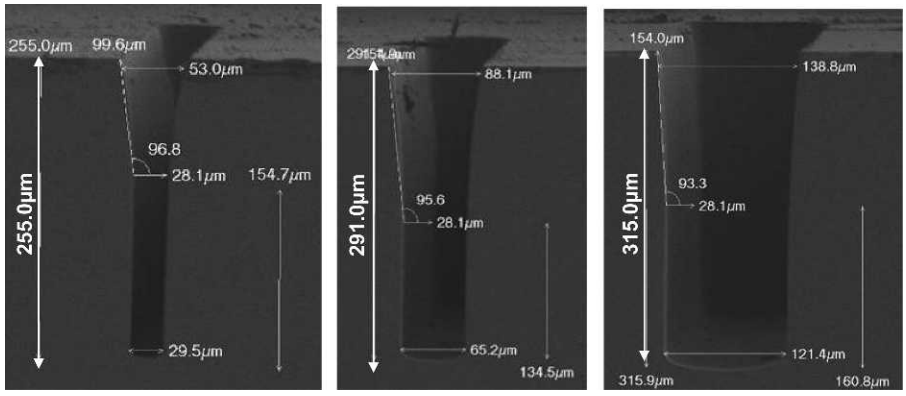


Fig. 6. SEM cross sectional micrographs of trenches of three typical widths and corresponding depths after etching with Bosch process and global isotropic etch process. A detailed summary of top/bottom width, slope, and depth for different dimensions of the trenches are shown in Table VII-.

Table III
Dual-Etch Via Tapering Process Using Bosch and Global Isotropic Etch Process

First etch step (Bosch etch process)	Etch cycle: Pressure = 27-29 mt; Coil power = 600 W; Platen power = 23 W; SF_6 = 130 sccm; O_2 = 13 sccm; Cycle time = 8 s Passivation cycle: Pressure =16-18 mt; Coil power = 600 W; Platen power = 0 W; C_4F_8 = 85 sccm; Cycle time = 5 s Platen Temperature: 10°C; Total process time: 120 min. Etch rate: 2-3μm/min on 15-20% exposed area. Etch selectivity to resist mask = 82-100:1
Second etch step or global isotropic etch process	Pressure = 32 mTorr (APC: 82.2%); SF_6 = 180 sccm; O_2 = 18 sccm; Coil power = 600 W; Platen power = 30W; Platen Temperature: 10°C; Process time: 5-30 min depending on required slope. Etch rate: 1.2-1.5 μm/min

variables, divergence, chemical, and isotropic etch rate. The nine simulation runs were programmed (see Fig. 2) to analyze the corresponding simulated topography results in the form of tony plots. The DOE experiments were designed to fit with experimental results corresponding to smallest trench width of 20-21 μm, as summarized in Figs. 4 and 6. The top and bottom dimension of the simulated trench widths and trench depths were extracted from the tony plot of each DOE run. The experimental matrix and output parameters are shown in Table IV. The optimization was done by specifying a close range of experimental constraints on the top critical dimension (CD), the bottom trench CD, and the trench depth as shown in Table V. The optimum values of the RIE model parameters obtained are summarized in Table VI which were subsequently used in simulating the dual-etch process for trench widths from 10-100 μm.

Table IV
2-Level 3-Factorial Experimental Matrix with Simulation Experimental Results

Run#	Divergence	Chemical etch	Isotropic etch	Top CD	Bottom CD	Depth
1	200	1	1	101	83.5	231
2	200	0	0	20	20	262
3	10	1	0	61.6	38.4	238
4	200	1	0	44.4	21.9	234
5	105	0.5	0.5	61.6	50.7	250
6	200	0	1	80	80	260
7	10	0	1	80	80	260
8	10	1	1	106	104	242
9	10	0	0	20	20	262

Table V
Summary of Constraints for Optimization

Constraints name	Goals	Lower limit	Upper limit	Lower weight	Upper weight	Importance (0-5)
Divergence	is in range	10	200	1	1	3
Chemical etch (μm/min)	is in range	0	1	1	1	3
Isotropic etch (μm/min)	equal to 0	0	1	1	1	3
Top CD (μm)	minimize	45	46	1	1	3
Bottom CD (μm)	minimize	21.5	22	1	1	3
Depth (μm)	minimize	235	239	1	1	3

Table VI
DOE Solution After Optimization

Divergence	Chemical etch	Isotropic etch	Top CD	Bottom CD	Depth
200.00	0.82 μm/min	0.00	45.67 μm	21.33 μm	238.71 μm

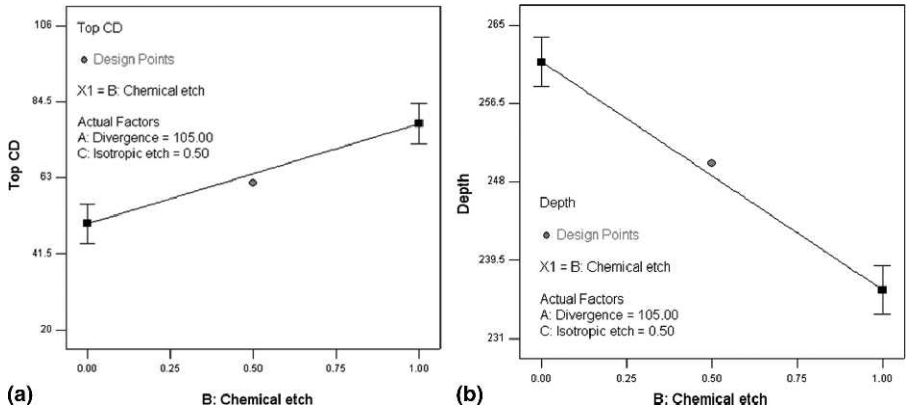


Fig. 7. The effect of the chemical etch parameter on top CD and depth of the etched trench is shown. (a) The top CD increases with increasing chemical etch rate in the second etch step of the dual-etch process. (b) The depth of the trench/via decreases with increasing chemical etch due to selective silicon etch at the top.

The experimental trend of the model parameters based on the DOE is shown in Figs. 7-9. The effect of chemical etch rate as a function of top CD and depth is shown in Fig. 7.

Results and Discussion

Based on the optimum model parameters (see Table VI), the etch topographies for trenches with widths varying from 10-100 μm were simulated and compared with experimental etch profiles (see Fig. 6). It can be seen that there is a close correlation between the simulated etch topographies and the experimental results as shown in Table VII. Fig. 10 shows a plot comparing the simulated and experimental etch trend of the dual-etch via tapering process. It can be seen that there is a close correlation within 10% deviation.

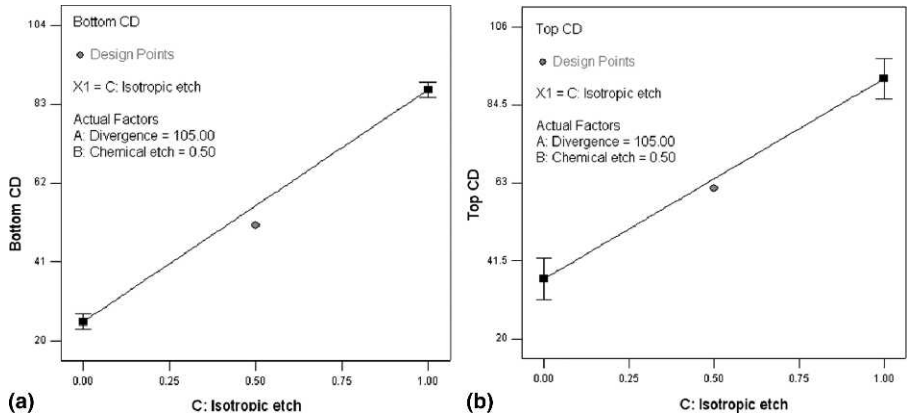


Fig. 8. Effect of the isotropic etch parameter on the top and bottom CD of the trench is shown. (a) The bottom CD increases with increasing isotropic etch rate. (b) The top CD increases with increasing isotropic etch rate in second etch step.

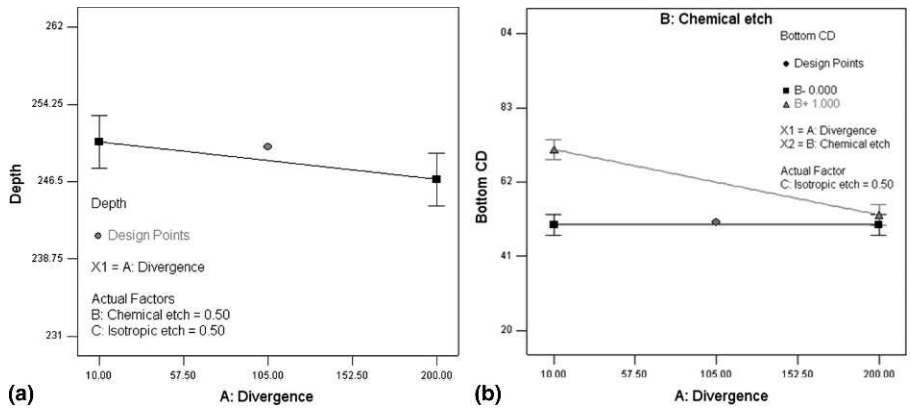


Fig. 9. Effect of ion flux divergence on the trench/via depth and bottom CD is shown. (a) The depth decreases with increasing flux divergence. (b) The bottom CD decreases with increasing flux divergence. It can also be seen that when the chemical etch is zero, there is no effect of divergence of the bottom CD.

Table VII
Comparison of Experimental and Simulation Results of the Dual-Etch Process

		Experimental results after	al Isotropic etch for 30min			Athena elite simulated results		
rench width after first etch (μm)	Trench depth after first etch (μm)	Top width (μm)	Bottom width (μm)	ench depth (μm)	Etch rate (μm/min)	Top width (μm)	Bottom width (μm)	Trench depth (μm)
21.6	262.0	48.3	21.6	237.7	2.2	46.4	22.1	237
29.5	291.1	53	29.5	255	2.4	56	32.6	264
39.8	307.0	66.1	40.3	268.6	2.6	67.1	43.4	285
50.2	317.8	76.9	51.6	283.6	2.6	77.6	54.3	299
60.9	323.4	88.1	65.2	291.1	2.7	88.3	64.4	296
70.3	328.1	98	73.1	294.8	2.7	98.3	75.2	309
79.2	335.6	106.4	85.3	301.9	2.8	108	85.2	309
89.5	336.6	121.4	96.1	301.9	2.8	119	96.1	325
100.3	339.4	128	107.8	309.8	2.8	129	107	313
108.8	345.5	138.8	121.4	315.9	2.9	139	117	317

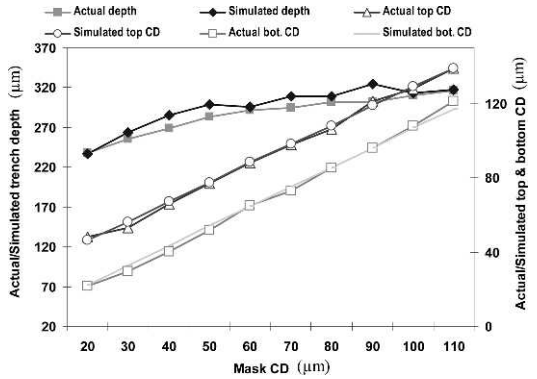


Fig. 10. Comparison is made between simulated and experimental results of dual-etch tapered via etch process. It can be seen that there is a very close match between the two results, within 10% tolerance.

Table VIII
Simulation Results of Via Tapering Etch Process with Varying Etch Process Time

Etch time (min)	Top width (μm)	Bottom width (μm)	Final trench depth (μm)	Taper depth (μm)	Aspect ratio	Isoetch rate (μm/min)	Depth loss (μm)
5	26.1	20.2	258	39	11.1	0.8	4
10	29.2	20.6	254	72.2	10.2	0.8	8
15	33.9	20.9	249	122	9.1	0.87	13
20	37.7	21.4	244	147	8.3	0.9	18
25	41.6	21.7	239	191	7.6	0.92	23
30	45.6	22	235	234	7	0.9	27

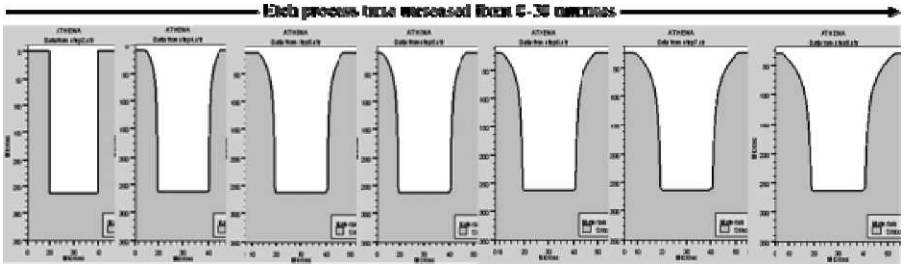


Fig. 11. Simulation of via tapering effect as the function of global isotropic etch process time from 0-30 min.

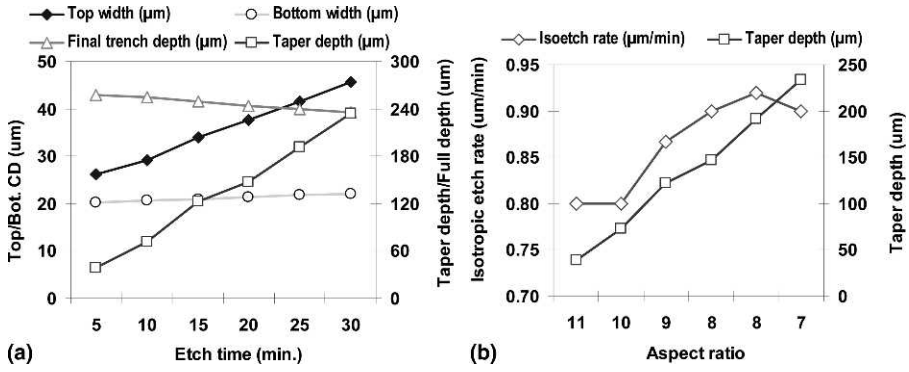


Fig. 12. Simulated results plotted as a function of isotropic etch time and aspect ratio. (a) The trench depth decreases with increasing etch time while the taper depth increases with etch time. The top width of the trench increases linearly with etch time while the bottom of the trench is unaffected due to diffusion limited etching. (b) The isotropic etch rate based on depth loss increases and stabilizes with decreasing aspect ratio. The taper depth also increases with etch time.

After establishing a dual-etch process model, it was used in further predicting the etch profile evolution as a function of isotropic etch time. Figs. 11 and 12 show the predicted results when the via tapering etch process is applied with different isotropic etch time from 5-30 min for a 20 μm wide trench/via structure (See Table VIII). It can be seen that while the depth of the trench/via decreases linearly, the depth of the taper increases with increased etch time. It is also seen that bottom of trench is least affected even after a longer etch from 5-30 min. This confirms that the basic etch mechanism for the second etch step is a diffusion limited etch process.

Conclusions

A dual-etch deep silicon via tapering process for TSV application was presented. Experimental characterization of the first and second etch step of the dual-etch process was done for trenches of widths varying from 10-100 μm and with depths ranging from 250-350 μm. Etch topography simulation process was setup with ELITE and optimized by doing a two-level three-factorial design of experiments with Design Expert-6. Based on the optimized simulation parameters, the etch topographies of simulated and experimental results were correlated

and shown to be close to 10%. It was further shown that the simulation models can be used to study the evolution of tapered silicon via when etch time is varied.

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