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# Critical Issues of TSV and 3D IC Integration

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***Abstract*—Moore's law has been the most powerful driver for the development of the microelectronic industry. This law is grounded in lithography scaling and integration (in 2D) of all functions on a single chip, perhaps through system-on-chip (SoC). On the other hand, the integration of all these functions can be achieved through system-in-package (SiP) or, ultimately, 3D IC integration. However, there are many critical issues for 3D IC integration. In this study, some of the critical issues will be discussed and some potential solutions or research problems will be proposed.**

***Keywords*—3D IC integration, TSV with RDL, solder microbumps, MEOL, thin wafer handling, thermal management**

## Introduction

The invention of the transistor by Bardeen, Brattain, and Shockley of Bell Laboratory in 1947 (which earned them the 1956 Nobel Prize) foreshadowed the development of generations of computers and smart phones. The invention of the silicon integrated circuit (IC) by Jack Kilby of Texas Instruments in 1958 and 6 mo later by Robert Noyce of Fairchild Semiconductor excited the development of generations of integrations. The proposal (for minimum cost) of doubling the number of transistors on an IC every 24 mo by Gordon Moore in 1965 (also called Moore's law) has been the most powerful driver for the development of the microelectronic industry in the past 44 y. This law arose from the field of lithography scaling and integration (in 2D) of all functions on a single chip, and has been true through the system-on-chip (SoC) advances.

Taking it to the next level, integration of all these functions can be achieved through system-in-package (SiP) or, ultimately, 3D IC integration, which is one of the "*more-than-Moore*" applications. (Based on the silicon platform technology, anything that involves the integration of electronics, photonics, mechanics, chemistry, heat, magnetics, biology, etc., for functionality and system performance when interacting with people and the environment, is known as more-than-Moore.)

TSV is the heart of 3D integration technology. Fig. 1 shows the patent "Semiconductive Wafer and Method of Making the Same" filed on October 23, 1958 and granted on July 17, 1962 by William Shockley. Yes, the same William Shockley, who coinvented the greatest invention of all time in Electronics Industry—the transistor. Please see "Who invented TSV and When?" posted at 3D InCites on April 24, 2010 (http://www.semineedle.com/posting/31171).

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It should be pointed out that besides TSV there is another group of much smaller vias ($\leq$0.1 μm in diameter) on a chip as shown in Fig. 2. These tiny vias are connected to devices such as transistors (four tiny vias for each transistor) to build the first metal layer. Today, the number of these tiny vias, for many chips, already exceeds the world population of over 7 billion. These vias, which the semiconductor foundries can do best, are one of their core competences and major businesses. On the other hand, for the "huge" vias that we called TSV for 3D IC integration, the number is many times fewer and the size is many times larger. These TSV are done best by packaging assembly and test houses. Also, they build 3D IC integration packages for the TSV chips and to perform the final tests. Then, they ship only the good ones to EMS (electronics manufacturing services) who perform the PCB assembly, in-circuit test, final assembly, system (also called final or functional) test, and ship the product to the system houses' hubs for distribution. Some system houses prefer to have their EMS ship them the in-circuit tested good PCBs, perform the final test in-house, and then ship the product. This is the infrastructure and how the electronics industry works. Of course, for some special reasons or niche applications, there are always a few exceptions.

3D IC integration is the key technology for electronic products which must meet the following requirements:

(1) Form factor, smaller is better. For example, PDAs, cameras, cell phones (COMS image sensors).
(2) Performance, faster is better. For example, shorten local and global interconnect lengths.
(3) Cost, cheaper is better. For example, system improvements without the high cost of scaling.
(4) Reliability, low-risk is better. For example, it still works after drops.

The Holy Grail of 3D IC integration (e.g., heterogeneous integration) is shown in Fig. 3, where all the chips, for example, microdisplay, MEMS, memory, microprocessor, optoelectronic, multiple output dc-dc converter, digital signal processor, microbattery, and analog-to-digital (A/D) mixed signal are combined and stacked in three dimensions. It can be seen that, in general, the electrical performance of 3D IC integration is better than that of 2D SoC. However there are many critical issues in questing for the Holy Grail. Some of the critical issues will be discussed and some potential solutions or research problems will be proposed in this study.

## 3D Integration

Fig. 4 shows three different groups of 3D integrations, namely: (1) 3D IC packaging, (2) 3D IC integration, and

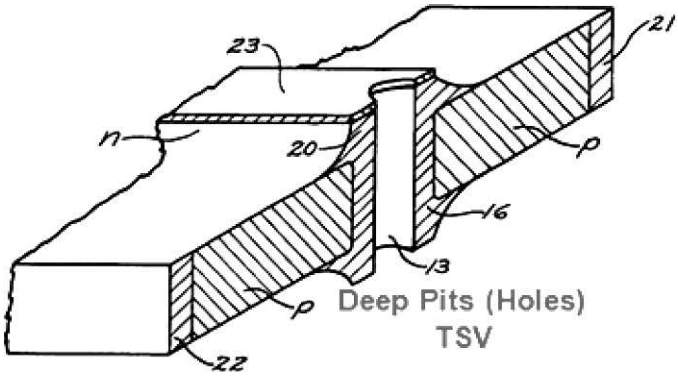


Fig. 1. TSV invented by Shockley (US Patent # 3,3044,909, filed on October 23, 1958 and granted on July 17, 1962).

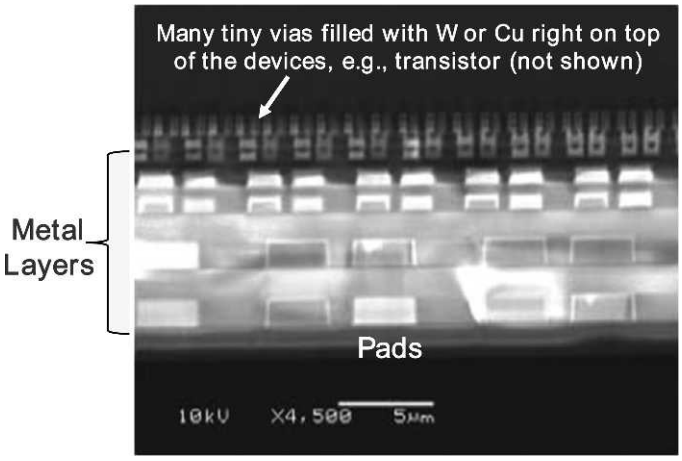


Fig. 2. Tiny vias (not the TSV for 3D IC integration) in a chip. (65 μm Cu/low-k by *GlobalFoundries*, 2006.) Today, the number of these tiny vias, for many chips, already exceeds the world's population of over 7 billion.

(3) 3-D Si integration. It can be seen that 3D IC packaging is a mature technology and in mass production; thus it will not be discussed herein. The biggest difference between 3D IC packaging and 3D IC/Si integrations is that the integrations two use TSV and 3D IC packaging does not. The biggest difference between 3D IC integration [1-41] and 3D Si integration [42-61] is that 3D Si integration is assembled only by the method of wafer-to-wafer bonding and is bumpless. A 3D integration roadmap is shown in Fig. 5. Since there is no volume production in sight of the 3D Si integration in the next 10 years, it will not be discussed herein.

### *A. FEOL, BEOL, and MEOL*

FEOL (front end of line) is usually performed in wafer fabs (to pattern the active devices, e.g., transistors, resistors, etc.) and the process is from a bare wafer to passivation, which covers everything except the bonding pads for the next level of interconnect. BEOL (back end of line) is usually performed

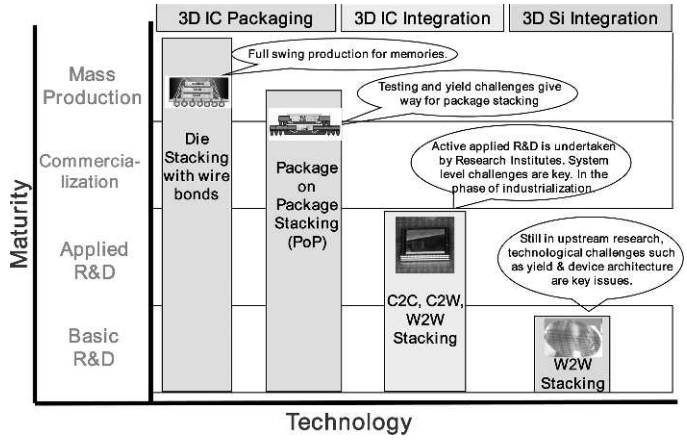


Fig. 4. Status of 3D integration technologies.

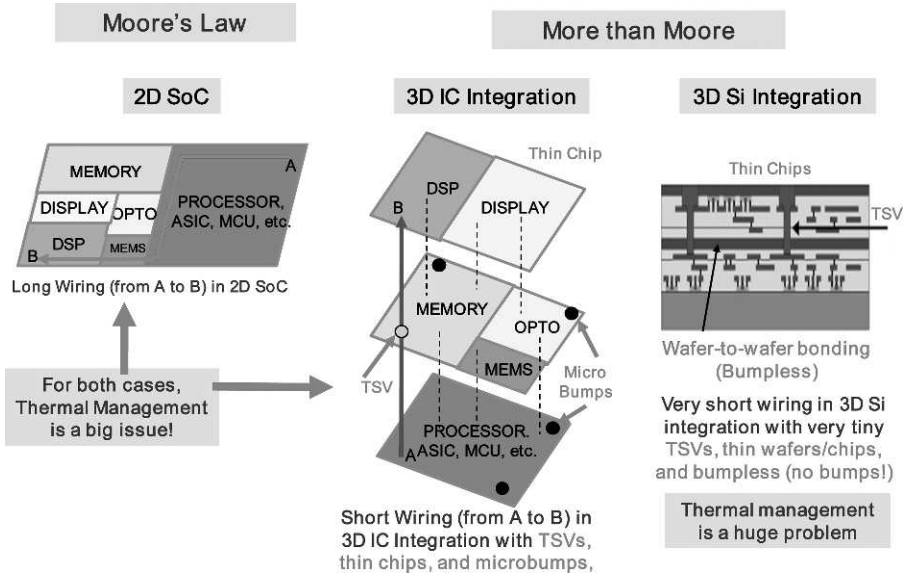


Fig. 3. Moore's law (2D SoC) versus more-than-Moore (3D IC/Si integrations).

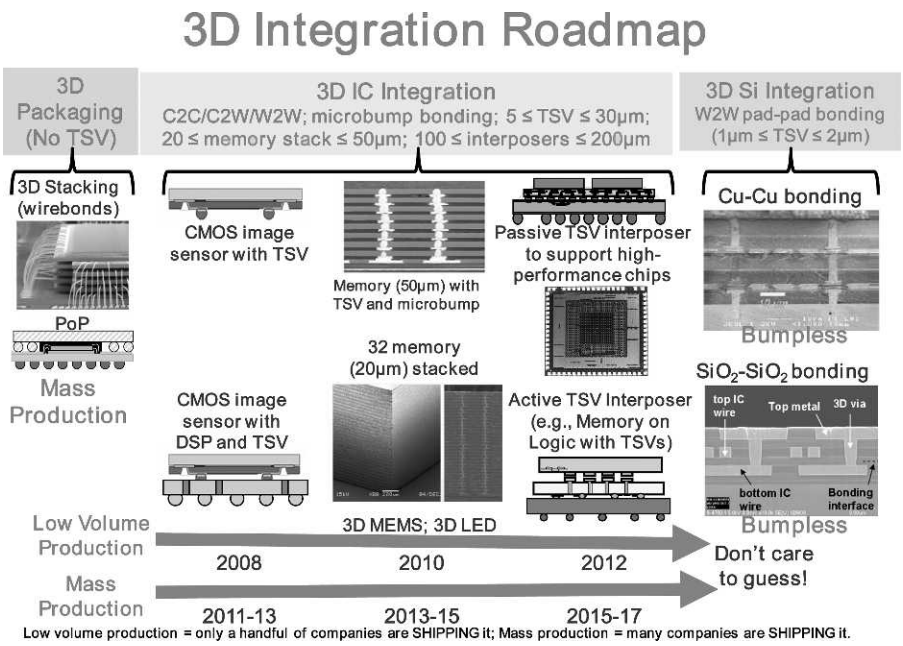


Fig. 5. 3D integration roadmap.

in packaging assembly and test houses and it involves everything after passivation, for example, UBM (under bump metallurgy), wirebonding, metallization, wafer bumping, backgrinding, and dicing. MEOL (mid end of line) is usually performed by integrating the FEOL and BEOL technologies into a 3D IC integration technology which involves, for example, TSV, microbumps, thin-wafer handling, metallization, UBM, wafer bumping, backgrinding, and dicing. (Please note that semiconductor people have a slightly different definition of FEOL and BEOL.)

### *B. Critical Issues of 3D IC Integration*

Just as with many other new technologies, 3D IC integration still faces many critical issues. In the development of 3D IC integration, the following must be noted and understood [1-41].

(1) Known good dice (KGDs) are required.
(2) Design guidelines and software are not available.
(3) Test methods and equipment are lacking.
(4) TSV with redistribution layers (RDL) usually are required.
(5) Microbumps usually are required.
(6) Wafer thinning and thin-wafer handling during processing are necessary.
(7) High equipment accuracy is necessary for alignments.
(8) Fast chips mix with slow chips.
(9) Large chips mix with small chips.
(10) 3D IC stacking inspection methodology is needed.
(11) 3D IC stacking expertise is lacking.
(12) 3D IC stacking infrastructure is lacking.
(13) 3D IC stacking standards are lacking.
(14) Thermal issues: the heat flux generated by stacked multifunctional chips in miniature packages is extremely high.
(15) Thermal issues: 3D circuits increase total power generated per unit surface area.
(16) Thermal issues: chips in the 3D stack may be overheated if proper and adequate cooling is not provided.
(17) Thermal issues: the space between the 3D stack may be too small for cooling channels (i.e., no gap for fluid flow).
(18) Thermal issues: thin chips may create extreme conditions for on-chip hot spots.

It can be seen that key enabling technologies for 3D IC integration are, among others: (1) TSV with and without RDL, (2) thin-wafer strengthening and handling, (3) microbumping and assembly, and (4) thermal management, which will be briefly discussed herein. Please note that design, test, reliability, and cost are always important, but they are beyond the scope of this study.

### *C. TSV with and without RDL*

The most important key enabling technology for 3D IC integration is TSV with and without RDL. They provide advanced vertical interconnects and SiP solutions such as C2C, C2W, and W2W stacking; wafer-level packaging and redistribution; interposer packaging; and the shortest electrical path (vertical electrical feed through) between two sides of a silicon chip or interposer. With the TSV, every chip can have two surfaces with circuits allowing for 3D vertical integration as shown in Fig. 6. Just as with many other new technologies, TSVs still face many critical issues. In the development of TSVs, the following must be noted and understood [1-41].

(1) TSV cost is higher than that of wire bonding, at least for now.
(2) The only TSV volume product is CMOS image sensors.
(3) Developments on memory devices are just in the talking stages.

(4) High-speed logic and processors will come even later.
(5) TSV design software is lacking.
(6) TSV design guidelines are not commonly available.
(7) Copper filling helps on thermal problems but increases TCE (thermal coefficient of expansion).
(8) Void-free copper filling usually takes a long time (low throughputs).
(9) The TSV cost for poor-yield IC wafers is high because many TSVs are wasted on the bad dices.
(10) TSV wafer yields are high (>99.99%).
(11) There is a high cost for low TSV wafer manufacturing yield, especially for high-cost dices.
(12) Single-point touch-up on the TSV wafer is difficult.
(13) TSV wafer warpage is a problem owing to the TCE mismatch between the silicon and copper.
(14) Thin TSV wafer handling is necessary during all the processes.
(15) TSV with high aspect ratios are difficult to manufacture at high yield.
(16) Test methodology and software for TSV are lacking.
(17) High-volume production tools are lacking and/or expensive.
(18) TSV inspection methodology and software are lacking.
(19) TSV expertise, infrastructure, and standards are lacking.
(20) It is not known which are the cost-effective and reliable TSVs and for specific IC devices.
(21) It is not known how large the TSV market is.
(22) The life cycle of TSV is not known.

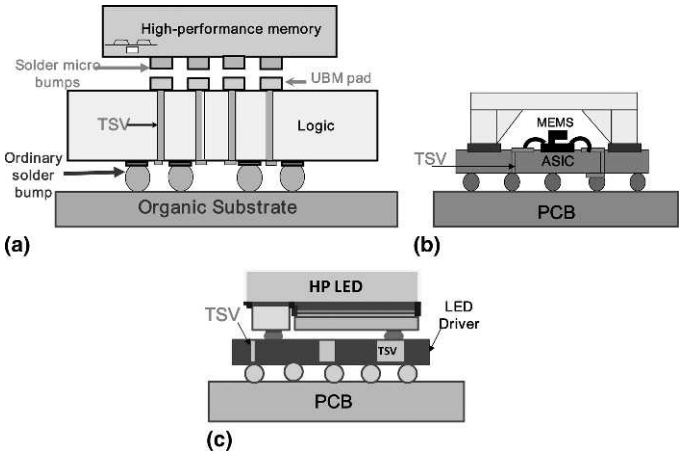


Fig. 6. For 3D IC integration, with TSV for electrical feed-through, every chip can have two surfaces with circuits. (a) A high-performance memory is supported by a logic (active TSV interposer). (b) A MEMS device is supported by an ASIC with TSV. (c) A high-power LED is supported by an LED driver with TSV.

There are many ways to make the TSV for 3D IC integration, for example, via first, via last, via middle, and so on. The most likely manufacturing process used by the industry for making the TSV 3D IC integration is shown in Fig. 7. There are five key steps to making the TSV.

(1) Via formation by either deep reactive ion etch (DRIE) or laser drilling.
(2) $SiO_2$ deposition by either thermal oxidation for passive interposers or PECVD (plasma enhanced chemical vapor deposition).
(3) Barrier and seed layers deposition by physical vapor deposition (PVD) or electrografting (eG).
(4) Cu plating or W (tungsten) sputtering to fill the vias.
(5) CMP (chemical and mechanical polishing) of Cu plating residues (overburden).

It should be noted that for bare wafers such as those for passive interposers, a layer of $SiO_2$ is needed before the photoresist. For active memory and logic chips and active

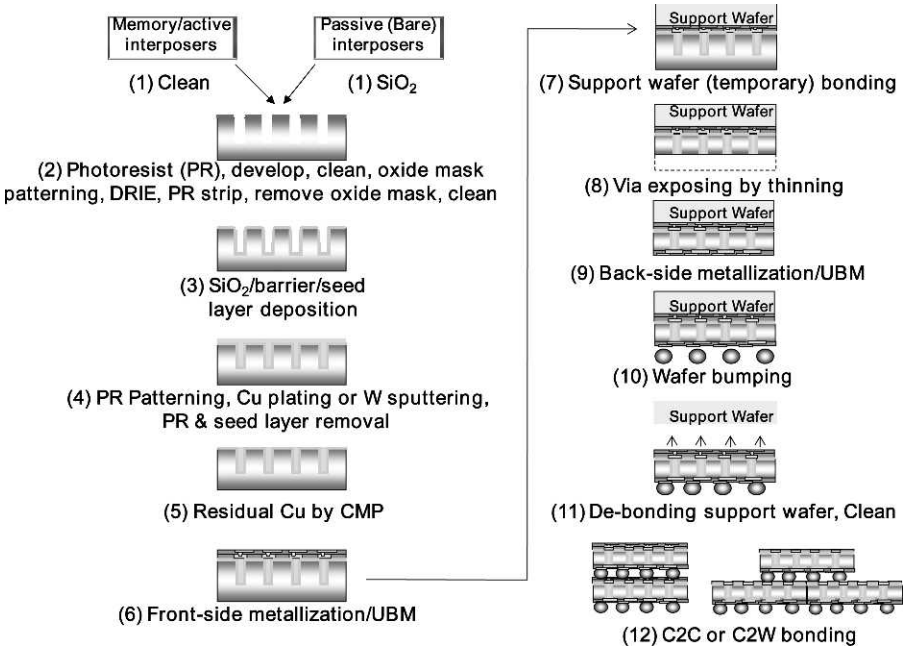


Fig. 7. The most likely manufacturing process of TSV with RDL for 3D IC integration.

interposers (e.g., ASIC and processor) because of their passivation layer, only cleaning is needed. The front-side metallization/UBM can be made next on the blind TSV wafer.

In most of the 3D IC integration applications, the thickness of the passive/active interposers ranges from 100 μm to 200 μm and the stacking memory chips range from 20 μm to 50 μm. Thus, a support wafer is needed for the remaining processes.

As soon as the support wafer is temporarily bonded to the blind TSV wafer, it can be thinned down to expose the TSV. This step is followed by back-side metallization/UBM and wafer bumping. After that, the support wafer is debonded from the TSV wafer. Finally, the TSV wafer is ready for either W2W bonding (only recommend for high yield IC wafers) or diced into individual chips for C2C or C2W bonding.

Fig. 8 shows a high performance chip (which cannot be supported by the BT-substrate), and the chip is supported by a passive TSV interposer with two redistribution layers on top and one redistribution layer at the bottom [18]. A simple BT substrate is used to fan out all the I/Os, powers, and grounds to the PCB. Fig. 9 shows the TSV with RDL wafer and the chip with its cross section clearly showing the two RDLs on the top side and one RDL at the bottom side of the interposer [18].

The TSV size should be as small as possible (≤30 μm). The reasons for this are because: (1) there is less thermal expansion mismatch between the Si and Cu, (2) there is less Cu plating, (3) there is higher throughput, and (4) there is more space for routing. Vias of 5-10 μm are not uncommon for 3D IC integration. It should be pointed out that for 3D Si integration the via size could be ≤1 μm.

## Thin Wafer Handling

In order to have low-profile products with 3D IC integration technology, the thickness of the chips/wafers is usually very thin. Making the wafer thin is not a big problem. Most of the backgrinding machines (e.g., Disco) can do the job and grind the wafers to as thin as 5 μm. However, handling thin wafers through all the semiconductor fabrication and packaging assembly processes is difficult. Usually, the thin-device wafer is temporarily bonded on a support wafer. Then it goes through all the semiconductor fabrication processes, such as metallization, passivation, UBM, and the packaging processes, such as backgrinding and solder bumping. After all these are done, removing the thin wafer from the support wafer poses another big challenge. This study discusses a few methods for handling thin wafers.

The new 3M+SUSS wafer support system [62] enables conventional backgrinding equipment to be used to produce wafers with a final thickness as low as 20 μm. The key to the system is its ability to provide a rigid, uniform support surface to minimize stress on the wafer as the silicon is removed, resulting in less cracking and chipping. The system includes both the equipment and consumables [3M UV-Curable Liquid Adhesive LC-2201, glass support plate (typically recycled, can be reused many times), and 3M light-to-heat Conversion Solution] necessary for mounting, demounting, and removing adhesive from the wafer.

In the 3M+SUSS system, a glass plate is used to support the wafer through the backgrinding process. A UV-curable liquid adhesive is used as the bonding agent between the device wafer and the glass plate (support wafer). After the backgrinding process, the thinned device wafer is transferred onto a dicing tape, and the support glass is removed by laser debonding of the adhesive-glass interface using a light-to-heat conversion (LTHC) layer. The adhesive can then be removed from the wafer, leaving behind less residue than typically seen with backgrinding tapes. This system also works for other semiconductor and packaging processes as long as the thermal expansion mismatch between the device wafer and the glass plate is within the allowable tolerance.

EVG+Brewer Science have developed a solution that enables temporary bonding of a device wafer to a right carrier substrate (support wafer) and allows not only thinning but also a full range of subsequent processes, including high-temperature deposition, etching, lithography, dielectric application, and curing, plating, and chemical cleaning [63].

### A. Temporary Bonding

The front side of the device wafer and the support wafer are coated with the WaferBOND, an HT Brewer Science adhesive

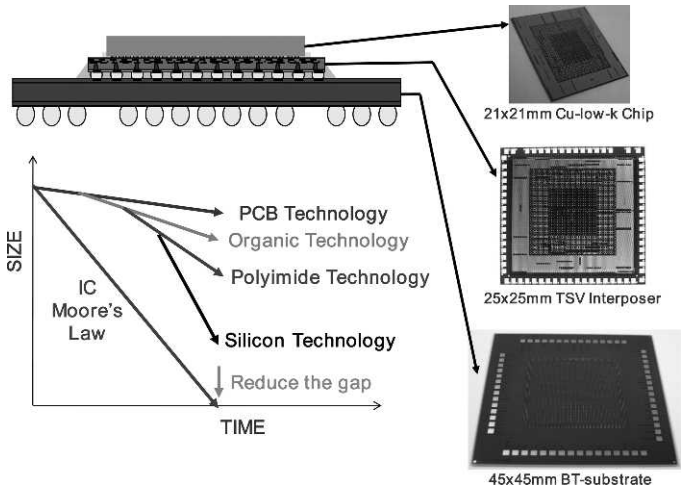


Fig. 8. A high-performance chip supported by a passive TSV interposer soldered on a BT substrate.

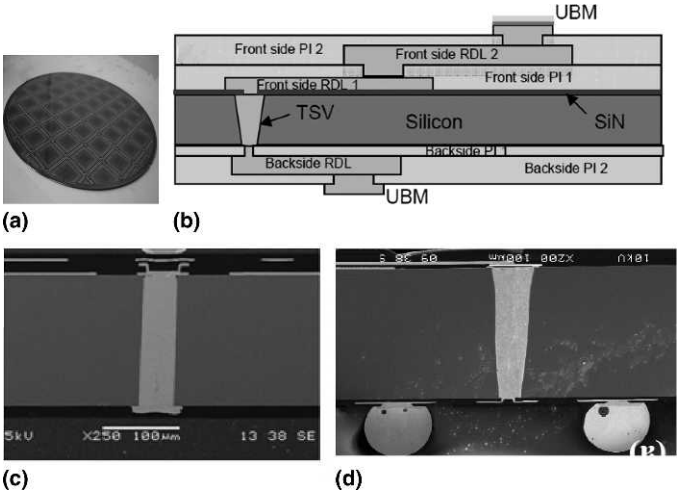


Fig. 9. TSV wafer (with two RDL on top and one RDL on the bottom) made by the process shown in Fig. 7.

material, by using a coating chamber that includes spin and spray coat capability. Both wafers then are transferred to a bond chamber, where they are carefully centered and vacuum bonded at elevated temperatures. Once the device wafer is temporarily bonded to the support wafer, it is ready for backside processing, including backgrinding, etching, metallization, TSV formation, and so on.

### *B. Debonding*

During the debonding process, the thin wafer is debonded first via a thermally activated slide liftoff approach from the support wafer, cleaned in a single-wafer cleaning chamber to remove the remaining adhesive residues, and then transferred to the appropriate output format, such as a film-frame carrier, a dedicated wafer cassette, or a coin-stack packing canister. The support wafer is also cleaned and can then be reused immediately for another debonding process.

A simple support wafer method for thin wafer (50 μm) handling is shown in Fig. 10 [27]. One of the key problems encountered in the support-wafer method is wafer debonding. The 50-μm-thick device wafer is easily broken during the wafer debonding process. This key problem is resolved by optimizing the wafer debonding process to minimize residual stress. The first step is to reduce the pitch of the release hole on the perforated support wafer from 3.5 mm to 2 mm. The second step is to increase the number of perforations on the edge of the support wafer. These two optimized debonding methods allow more chemical solution to uniformly penetrate into the bonding adhesive and eventually debond the wafers successfully. For example, the thin (50 μm) device wafer is attached to a support wafer and is handled and put in the PECVD chamber for $SiO_2$ deposition. No wafer cracking is observed during wafer handling and after silicon oxide deposition. Some engineering and process development are required, though.

## Low-Cost Lead-Free Solder Microbumps

As mentioned earlier, the thickness of chips for 3D IC integration application is thin and thus the conventional flip chip solder bumps (~100 μm) cannot be used for connecting the thin chips. Instead, tiny bumps in the range of 20-30 μm are needed. Fig. 11 [10-12] shows the cross sections of the bonding of two Si chips (the bottom one is with TSVs). It can be seen that the lead-free solder is pure Sn, the pitch is 15 μm, and the circular pad is only 8 μm. Underfill is usually needed between two chips, one of which has Cu-plated TSV because of the thermal expansion mismatch. (The equivalent CTE of a copper-filled TSV silicon chip could be as high as $10 \times 10^{-6}$/°C.) Due to the tiny gap between the chips, smaller filler size underfills (max $\leq$ 3 μm and ave $\leq$ 0.5 μm) are required.

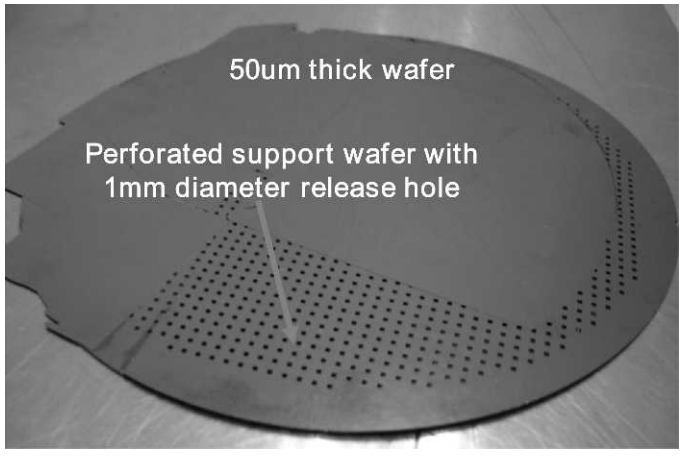


Fig. 10. A simple support wafer method for thin wafer handling.

## Thermal Management of 3D IC Integration

As mentioned earlier, thermal management of 3D IC integration system is important. Two examples are shown in this study. For other results, please see [7]. Fig. 12 shows the temperature maps on a chip for various chip thicknesses. It can be seen that the heat on the chip surface is well dissipated for chip thicknesses of 100-200 μm subjected to a generated power of 0.2 W. For the 200-μm-thick chip, the temperature distribution is almost uniform and equal to 35°C. However, the hot spot temperature on the chip increases to 69°C (0.2 W power) if the chip thickness is reduced to 10 μm, and the hot spot area is clearly shown.

Fig. 13 shows the effect of two heat sources at a distance apart (gap) on the thermal performance of two stacked copper-filled TSV chips. There are two distinct heat sources (each with 0.1 W and on $0.2 \times 0.2$ mm area) on each chip ($5 \times 5 \times 0.05$ mm). It can be seen from the left-hand side and upper curve of the figure that (1) the larger the gap ($b/a \leq 0.7$)

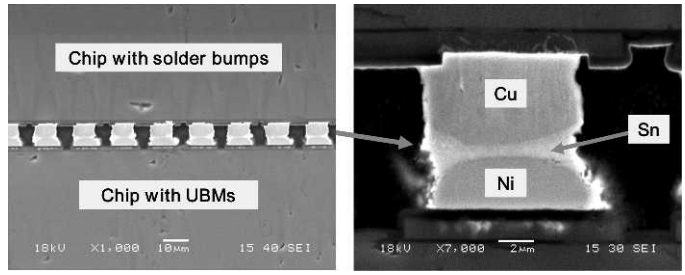


Fig. 11. SEM images of the assembly cross section of an Si chip and Si carrier with lead-free microbumps on 8 μm pads and 15 μm pitch.

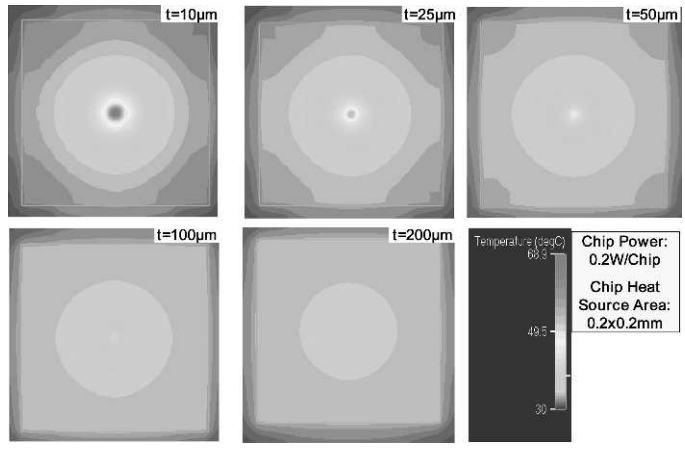


Fig. 12. Temperature maps on a TSV chips with various thickness (hot spot is clearly shown for chip thickness $\leq$ 25 μm).

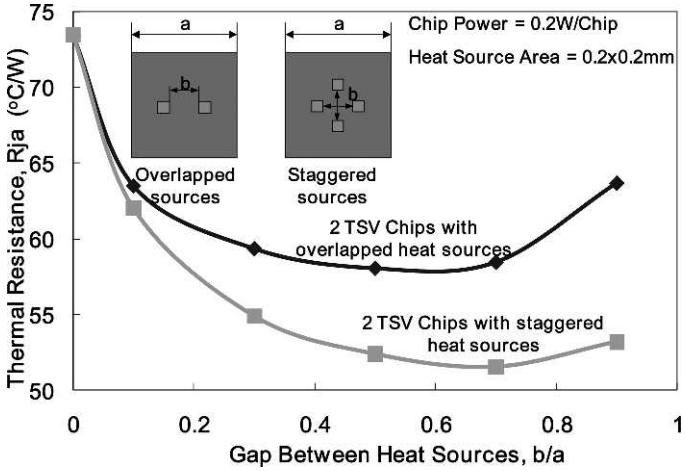


Fig. 13. Thermal resistance of a 3D integration of two Cu-filled TSV chips subjected to two distinct overlapped heat sources and staggered heat sources.

between the two heat sources, the better is the thermal resistance, and (2) when the gap between the two heat sources is larger than 0.7 (i.e., the heat sources are too close to the edge of the chip), the thermal performance is weaker. This is due to suppressible spreading effects near the edges of the chips.

In addition to the case of overlapping heat sources discussed in the preceding paragraph, the orientation effect (staggered heat sources) of two stacked chips, each with two heat sources at a certain distance apart, on the thermal performance of a 3D SiP is presented in the right-hand side and lower curve of Fig. 13. It can be seen that (1) similar to the case of overlapping heat sources, the larger the gap ($b/a \leq 0.7$) between those two pairs of staggered heat sources, the lower are the maximum junction temperature and thermal resistance, (2) when the gap between the two pairs of staggered heat sources is larger than 0.7 (i.e., the heat sources are too close to the edge of the chip), the thermal performance is weaker, and (3) the maximum thermal resistance of the 3D SiP with two TSV chips subjected to two pairs of staggered heat sources are lower than those with two pairs of overlapping heat sources. This is so because the staggered heat sources avoid the superimposition of heat sources and thus lead to better thermal performance. This result is useful for the design and layout of 3D SiP because it permits relocation of the heat sources and/or rotation of the chip.

## Summary and Recommendations

Some critical issues (challenges and opportunities) of TSV and 3D IC integration have been discussed and some potential solutions or research problems have also been proposed in this study. Some important results and recommendations are summarized in the following.

(1) 3D IC integration is the key technology for electronic products which must meet the requirements of form-factor, performance, cost, and reliability.
(2) TSV, thin wafer handling, microbumping and assembly, and thermal management are the key enabling technologies for 3D IC integration.
(3) TSV (with the concept that every chip can have two surfaces with circuits) opens the door for many new and useful applications.
(4) TSV size should be as small as possible ($\leq$30 μm). A size range of 5-10 μm for 3D IC integration is not uncommon.
(5) The thickness of interposers (both passive and active) ranges from 100-200 μm and for the stacking memory chips, the thickness ranges from 20-50 μm.
(6) The size of low-cost micro bumps connecting the thin chips should be $\leq$25 μm.
(7) The most likely manufacturing process of TSV for most 3D IC integrations is shown in Fig. 7.
(8) Today, a supporting wafer (carrier) with a special adhesive is necessary for thin wafer handling.
(9) More developments are needed on low-cost and high-quality (such as adhesiveless and carrierless) thin wafer handling methods.
(10) More research needs to be done on strengthening (such as material improvements and special geometry of) the thin wafers.
(11) More works need to be done on reliable ultra fine-pitch microbumping and assembly. Underfills with fine filler sizes are needed.
(12) Cost-effective thermal management methods for 3D IC integration systems are desperately needed.
(13) Due to very thin chip thickness, special attention should be paid to hot spot temperature.
(14) The focus of this study is on the technology such as the TSV (the heart) of 3D IC integration. It should be pointed out that the soul of 3D IC integration lies in design and testing.
(15) The industry should build an ecosystem such as the standards and infrastructures for the 3D IC integration as soon as possible; so the EDA (electronic design automation) vendors would seriously and systematically write the software for the design, simulation, analysis and verification, manufacturing preparation, and testing of 3D IC integration SiP.

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