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Chip on Board Packaging and Thermal Solutions for a 100 W Large Monolithic LED

Jay G. Liu,* Daxi Xiong, and Paul Panaccione

Abstract—**Thermal challenges are now widely recognized as one of the key barriers to LED's fast penetration to broader market. This paper demonstrates an effective packaging and thermal solution for a commercial realization of a large area monolithic LED of 12 mm^2, with high current operation and total input power as high as 100 W. A direct chip on board (COB) die attach method was used to eliminate one level of interface such as existed in an SMD LED on an insulated metal substrate. High thermal conductivity LED submount and copper core board were designed for effective heat spreading without a dielectric in the thermal path. The thermal resistance of the 12 mm^2 LED from junction to heat sink, including core board and associated TIM1 and TIM2, is as low as 0.7°C/W. A thermal model was developed using FEA to describe the temperature and thermal resistance at each interface, and is shown to be in agreement with measured data. The LED chipsets described here have been used to power systems such as rear projection TVs and front projectors.**

Introduction

Over the past few years, major advances in material and device technologies have improved the performance of LEDs, leading to higher current, higher power, brighter LEDs which penetrate into new lighting applications that were never before possible [1, 2]. One notable example is the commercial availability of a new class of LED which uses the photonic lattice technology, PhlatLight^{TM} developed by Luminus Devices [3, 4]. Applying microstructures of feature sizes on the order of a wavelength onto a vertical structure LED that uses unique processing to transfer active layers to a metal submount, PhlatLight technology made it possible to build large-area LEDs that operate at input powers as high as 100 W and are orders of magnitude brighter than conventional power LEDs [5]. The enhanced light extraction and beam shaping enable the ultra-high power light sources for projection and other illumination applications [6, 7].

Although LED lighting is much more efficient than traditional lighting, the majority of its input power is dissipated as heat. At 100 W for a 12 mm^2 LED, the dissipated heat can be equivalent to a power density of over 700 W/cm^2. This level is much higher than in current microprocessors, and is not just limited to hot spots. In PhlatLight chips, the power density is continuous over the entire surface area. At such high heat flux density, handling the dissipated thermal power presents a design and packaging challenge. It is clear that to keep the PhlatLight device properly operating at this high power requires a packaging platform with extremely low thermal impedance. Without effective thermal management, the heat generated by high power LEDs cannot be properly dissipated, thus resulting in a higher junction temperature. This leads to reduced lumen output, change in color, and forward voltage, as well as a shorter lifetime. The following section describes some of the design issues we tackled and the process and technical considerations we took into account in developing the PhlatLight package. Reliability data are also presented. The rigorous design effort and clever thermal solution resulted in the first LED based DLP TV using a single RGB chipset of 12 mm^2 PhlatLight LEDs.

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Luminus Devices Inc., Billerica, Massachusetts 01821
*Corresponding author; email: jliu@luminus.com

Package Design and Materials

In designing the package for PhlatLight LEDs with high power density over a large die area, the objective is to minimize the thermal resistance from junction to ambient. Selecting the right materials and optimizing the physical dimensions and interfaces are key to this effort, while at the same time considering the mechanical stress and reliability. Fig. 1 illustrates the 12 mm^2 PT120 package. The die is typically red, green, or blue, but can be white as well. For the specific projection application, no lens encapsulation is required. Instead, an AR coated window is used. Since the photonic lattice produces a certain degree of collimation, the air cavity design is advantageous as it reduces optical extent and allows more efficient optical designs. It also enhances reliability beyond that of a silicone encapsulated package. Fig. 2 shows a schematic of the cross-section of the package including each layer of materials and interfaces in the construction.

Table I lists the effective thermal conductivity and thickness of the packaging materials. Note that the effective thermal conductivity for TIM1 and TIM2 includes both bulk and interfacial resistances as shown in the equation below.

$$R_{\text{eff}} = R_{\text{interface1}} + R_{\text{Bulk}} + R_{\text{interface2}}$$

In order to reduce the thermal impedance, two basic approaches have been taken: (1) minimize the number of thermal interfaces in the package, and (2) minimize the thermal resistance (bulk + interfacial) of each constituent of the package [8]. The interfacial resistance can be a significant bottleneck in the case of TIM1 and TIM2.

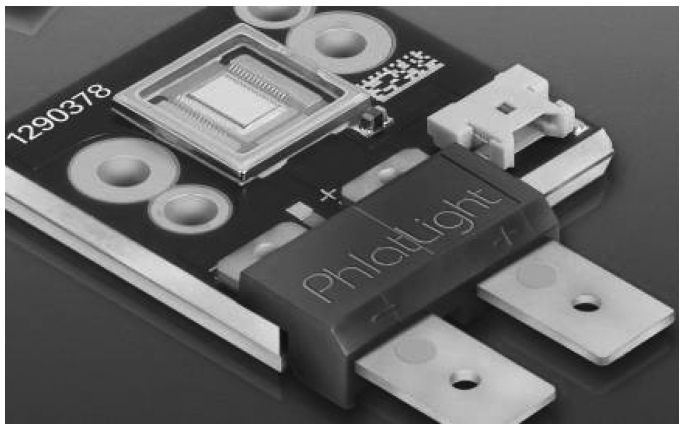


Fig. 1. PT120 chip on board package with a 12 mm^2 die.

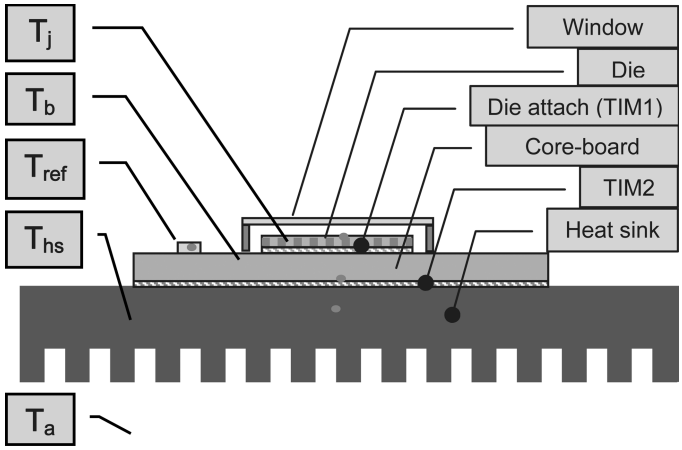


Fig. 2. PT120 package construction and different thermal layers and interfaces.

A. Minimizing the Number of Thermal Interfaces

For thermal improvement, the PhlatLight package uses a direct chip on board die attach method. This way, it does not include an SMD package, thus eliminating the relatively resistive SMD substrate, a layer of solder (often void-prone), and their associated interfacial resistances. Another unique feature of the package is that the dielectric has been eliminated from the insulated metal substrate (IMS) or MCPCB directly under the die that is normally required for creating isolation and coplanarity for SMT soldering.

B. Minimizing Thermal Resistances of Each Material and Interface

1) LED die: A unique wafer level process was used to transfer the active layers to a metal submount with conductivity of about 185 W/mK, an order of magnitude higher than the original wafer material such as sapphire or GaAs. New materials are being evaluated within Luminus that may further double the conductivity.
2) Die attach material (TIM1): We have worked closely with our TIM1 supplier in developing an Ag-epoxy formulation with an exceptionally high bulk conductivity as well as good adhesion for our material set. The interfacial resistance can be a significant bottleneck and can dominate the bulk resistance. A balance of nonconductive resin and conductive silver particles segregated at the die and substrate interfaces is critical for low impedance die attachment. There are TIM1s in development at Luminus using nanotechnology that may further increase the bulk conductivity by an order of magnitude and virtually eliminate the interfacial resistance as illustrated in Fig. 3.
3) Metal core board: The metal core board has been designed to reduce sensitivity to a TIM2 by taking into account thickness, area, material, and clamping for good pressure distribution. Both copper and aluminum have been modeled using FEA and their dimension and thickness are compared, as shown in Fig. 4. For the 12 mm^2 die, we picked 3.2 mm thick copper board of 26 mm × 28 mm to give sufficient heat spreading and room for locating holes and mounting holes used for optic and heat sink mounting.
4) Board to heat sink interface material (TIM2): Many TIM2's are available, including phase change materials, reworkable dry films, or thermal pads, greases, liquid metal, indium alloy foils, and so on. We have studied various materials as a function of torque force that is important to ensure good interface during board to heat sink attachment as shown in Fig. 5.

TABLE I
Materials and Properties

	Effective thermal conductivity (W/mK)	Nominal thickness (mm)
Chip on metal submount	185	0.22
Die attach (TIM1)	17.6	0.063
Metal core board	400	3.2
Thermal pad (TIM2)	1.35	0.105
Heat sink	240-400	—

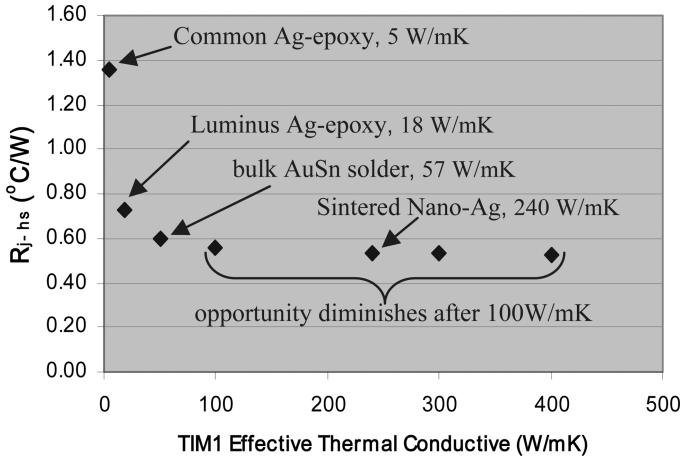


Fig. 3. Thermal resistance improvement opportunity from TIM1 material, on a 12 mm^2 LED COB package.

Chip on Board Process

Having selected the materials and designed the package, the next challenge is how to assemble the LED and materials

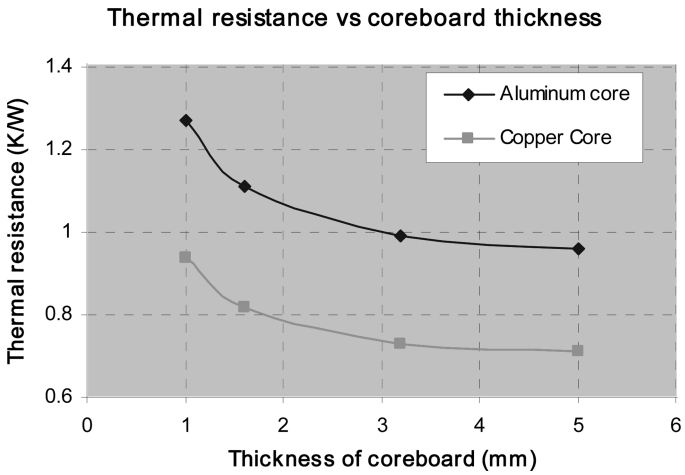


Fig. 4. Thermal resistance as a function of core board thickness for both Al and Cu.

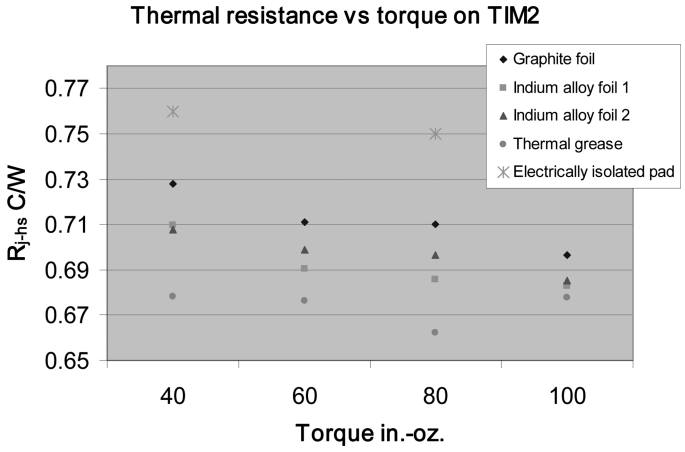


Fig. 5. Resistance as a function of torque for different types of TIM2 materials

together without significant deviation from the thermal model. A great deal of design of experiment (DOE) was carried out to select the right process and optimize the process input and output parameters. This is especially true for the silver epoxy die attach as it is closest to the die heat source and has typically been the bottleneck for thermal conduction.

For the epoxy die attach process, the critical parameters include epoxy thickness, fillet formation, voids in the bulk material, and interfacial bonding.

A. Bond Line Thickness (BLT)

The general approach is to minimize the BLT, since it reduces the bulk resistance. A typical commercially available silver epoxy has a thermal conductivity an order of magnitude lower than that of metal or even solder. However, when specifying the BLT, the overall thermal mechanical performance needs to be considered. Stress due to the difference in the thermal expansion coefficients (CTE) between the LED die and core board needs to be evaluated so that the package can survive the thermal excursion during processing or during a thermal cycling test. A 2.5 mil BLT was found to be optimum for a 12 mm^2 die. This optimum BLT is die-size dependent. A smaller die can use a slightly thinner BLT due to the short neutral distance.

B. Filet Formation

An epoxy fillet should be formed around all four sides and used as an indicator for gap/void visual inspection. Fillets add to the total thermal interface area and thus provide additional heat spreading from the die to the core board. However, care must be taken to maintain the fillet height not to exceed half of the die height to prevent electric shorting to the die surface.

C. Void and Interfacial Adhesion

Voids need to be minimized so the resistance will not increase. One of the key process controls to achieve void-free epoxy bonding is to optimize the curing process. This is in addition to a proper epoxy material pot time control and dispensing parameter optimization. DOE has been carried out to study the ramp rate, holding time, and cooling rate. A two-stage curing process was developed to achieve the best cured properties. Die shear and adhesive failure mode are the critical output parameters for SPC during production.

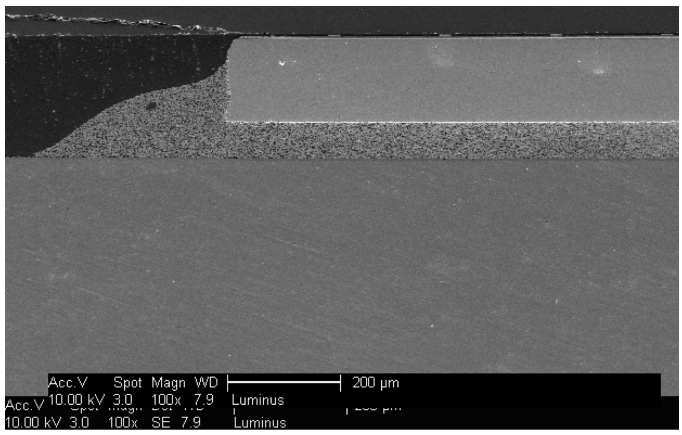
The interfaces between the epoxy and the bonding surfaces are as critical as the bulk epoxy. Resin tends to accumulate at the interface due to surface tension for wetting. As the resin is not a conductor, too much resin would reduce both thermal and electrical conductivity. However, if the interface is full of the silver particles, no adhesion bonding could be realized, resulting in low die shear force and cohesive failure. Fig. 6 shows the SEM cross-sections of the epoxy joint. As can be seen, there is no void noticeable in the bonding area. The epoxy resin (darker regions) and silver particles (light regions) are uniformly distributed across the interfaces and the bulk epoxy joint.

System Level Considerations

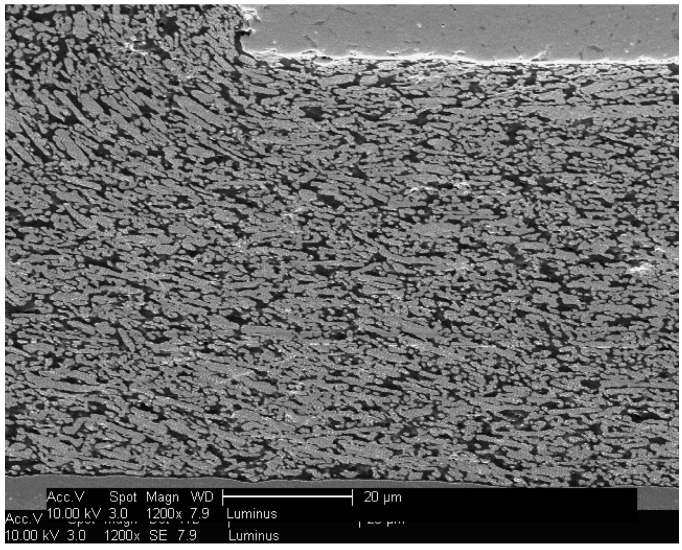
In addition to an effective die and packaging level design, the low thermal impedance and high drive current of Phlat-Light LEDs require a system level approach. These include heat sink design with passive or active cooling, electrical driver design, and optical coupling.

Beyond the package, users can employ commonly used active and passive thermal management methods for heat dissipation, as were demonstrated in our projection TV applications [9]. Decisions on active cooling such as with a fan or passive cooling with natural convection depend on application requirements such as input power, available space, noise, and cost. This is also true for the selection of heat sink size and geometry. Fig. 7 shows the modeled data comparing different cooling capacities for both COB and SMD packages on a heat sink. It is clear that the COB package has a significant thermal advantage over the SMD package, especially if active cooling or a larger heat sink is used.

From an electrical perspective, driver solutions need to be developed. Because of the commercial success in projection TV, driver solutions have become available from several large power semiconductor companies. The need for grounded common anode configurations has recently been addressed by



(a)



(b)

Fig. 6. SEM cross-section of the silver epoxy under (a) low magnification, and (b) high magnification.

National Semiconductor with the introduction of their LM3433 devices designed specifically for high current common anode applications [10].

From an optical design perspective, the large emitting area die in a low profile package allows the primary optical elements to be close to the emitting surface to avoid etendue losses. By using the photonic lattice, the light reabsorption due to the difference in index of refraction at the LED surface is minimized [5]. Luminus is able to optimize light extraction, engineering the design to modify the far-field distribution for unique benefits that are unavailable from any other LED technologies.

Thermal Performance and Modeling

Although some of the thermal calculation can be done using the one-dimensional steady state heat flow equation [8], finite element analysis (FEA) is needed when considering the complex system boundary conditions and the heat spreading effect. Fig. 8 illustrates an FEA model for the PT120 with an input

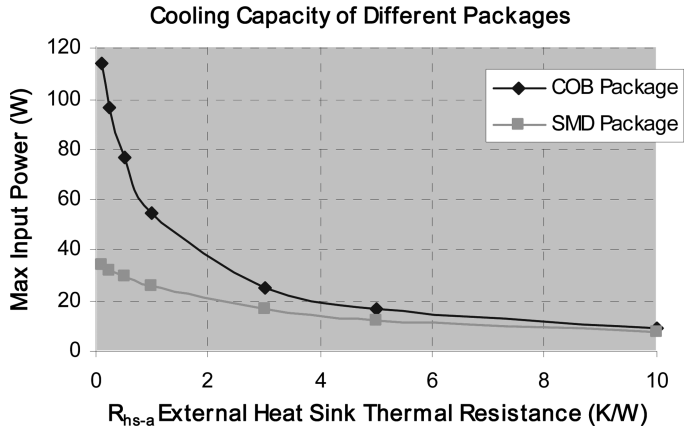


Fig. 7. The maximum power for a 12 mm^2 die as a function of external thermal resistance for both COB and SMD packages.

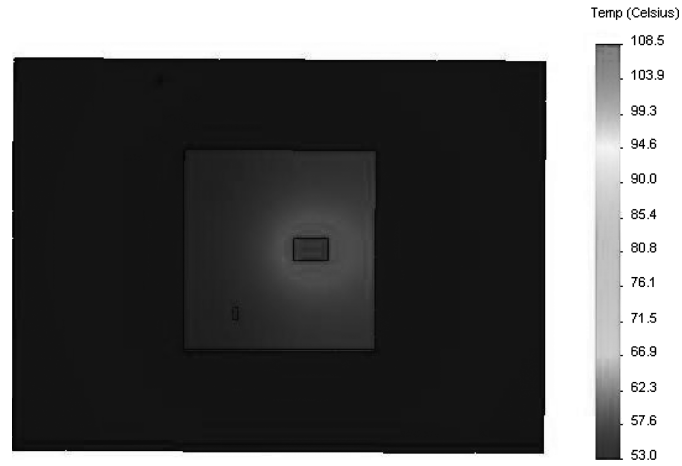


Fig. 8. FEA model shows the temperature distribution at different locations.

power of 70 W under a condition of external cooling thermal resistance of 0.25°C/W, at an ambient temperature of 35°C.

The modeled data agree well with the measured data as shown in Table II. The junction temperature measurement was done using a well known testing method that utilizes the wavelength shift over junction temperature change on a red die that is well calibrated.

The model also provides additional thermal information that is impractical for accurate direct measurement. The thermal resistance data at each individual layer and interface provide important guidance on where the thermal bottleneck is, and thus effort can be focused to tackle that area. Under this specific thermal condition, TIM1 and the spreading thermal resistance from the TIM1 interface to the core board are the two areas contributing most to the total thermal resistance. Future development activity will be centered on these areas.

Applications and Reliability

The PT120 projection chipset features individual red, green, and blue PT-120 devices. The large 12 mm^2 emitting area makes this chipset ideal for use in both front projectors and rear projection TV with DLP® microdisplays. The PhlatLight LED provides the following benefits over traditional arc lamp:

TABLE II
Comparison of Modeled and Tested Thermal Resistance

	Thermal resistance stack-up (C/W)	
	FEA model	Test data
Die	0.091	—
TIM1	0.259	—
Spreading from die to core board	0.238	—
Subtotal	0.588	0.61
Core board	0.023	—
TIM2	0.096	—
Spreading from core board to heat sink	0.012	—
Heat sink	0.007	—
Total	0.736	0.73

- Wide color gamut that exceeds the NTSC standards
- Instant turnon
- Mercury-free, RoHS compliant, environmentally-friendly technology
- Fast switching properties enable electronic control of color points and light intensity on a frame by frame basis
- Outstanding reliability with median lifetimes greater than consumer products

The photonic lattice technology and large emitting area make PhlatLight LED unique in comparison with other LED products. The effective package design as well as system integration produce 100% uniform surface emission for high collection efficiency and low optical losses. An RGB PT120 chipset under continuous operation can produce over 3000 white lumens at 8000K color temperature. Between 2006 and 2008, Samsung launched a series of LED powered RPTVs in sizes ranging from 50 to 67 in. Excellent field reliability was demonstrated. This is a result of extensive reliability tests Luminus has conducted on these LED devices and packages. Fig. 9 shows the reliability data based on operating life test for the PT120 under both pulse and CW drive current. These curves are generated by extrapolation of the median time to failure (MTTF) data using activation energies. As shown in Fig. 9, MTTF exceeds 60,000 h for operation at 2.0 A/mm^2 CW or 2.5 A/mm^2 pulse conditions. The recommended operating conditions for the stated lifetime are 70-80°C for red and 100-120°C for blue and green.

In addition to multicolor, white PhlatLight LEDs are also available for high performance illumination applications other than microdisplay projection. The variants of PT120 with chip sizes ranging from 4 mm^2 to 12 mm^2 and different aspect ratios have been introduced to other specialty lighting markets. White LEDs are developed and packaged with and without lens encapsulation to meet different requirements. For certain applications where design flexibility and ease of manufacturability are preferred over thermal performance, SMD packages have also been developed and are becoming available.

Summary

Thermal consideration is an important part of the power LED package design. For a PhlatLight LED with power up to 100 W on a single large die, the development of vertical structure on a metal submount, effective chip on board packaging, state-of-the-art die attachment material and processes, and the use of a highly conductive heat spreader proved to be critical. This paper presented detailed design considerations and thermal test results. The design and process control lead to the junction to heat sink thermal resistance of 0.73°C/W for a 12 mm^2 die which is in good agreement with the thermal model prediction. The low thermal resistance and the optimized package design ensured the high performance and high reliability of the PhlatLight product, which became the first LED light source capable of replacing traditional arc lamp in very large screen projection TVs.

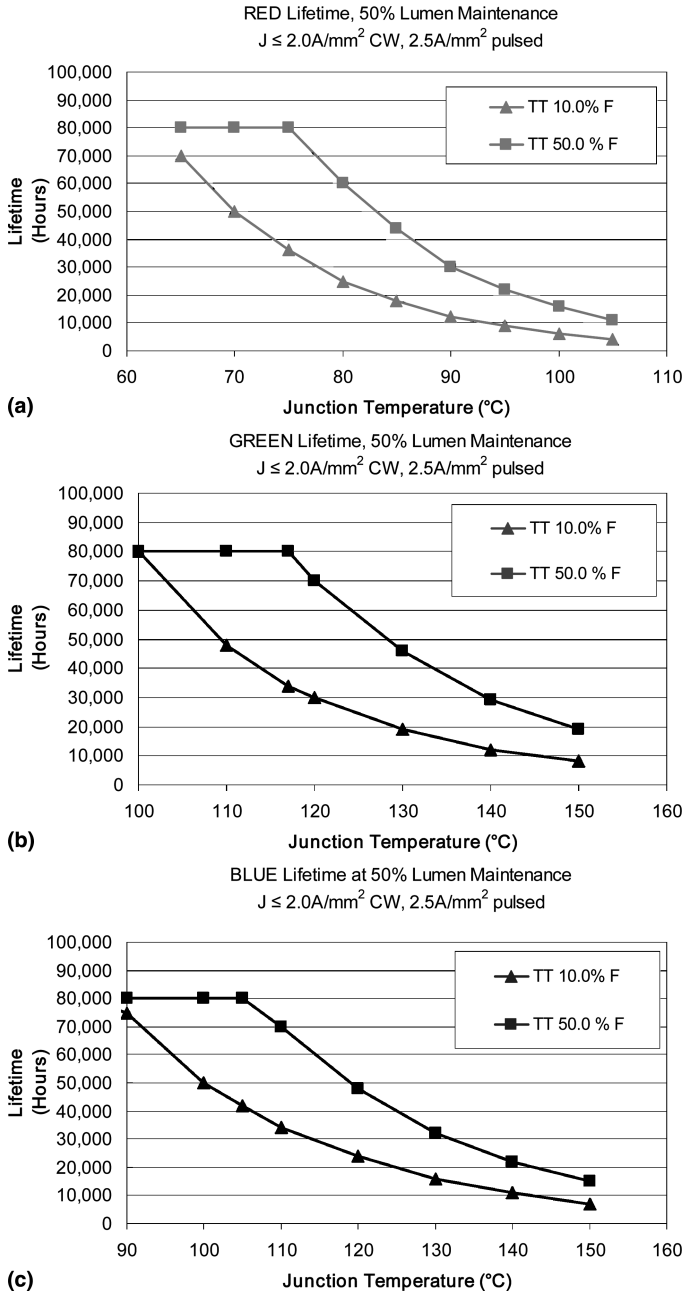


Fig. 9. TTF for 50% and 10% of population at 50% lumen maintenance for R, G, and B, respectively.

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