Development of High Reliability Via on IVH (VONI) for High Density Interconnect Circuit Boards

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Abstract

Via on interstitial via hole (VONI) technique is a complex set of technologies for blind and buried vias in traditional sequential lamination cycles with external layers, and micro via holes (MVH) for true high-density packaging. However, when VONI is repeatedly subjected to thermal stress, the interstitial via hole (IVH) in its structure often creates problems such as IVH barrel cracks, and layer-layer delamination. To solve VONI's reliability problems, such as IVH barrel crack and layer-layer delamination, the authors have investigated the relationship between the CTE difference and the effect of moisture. Through using different types of plugging inks, it was clearly indicated that delamination was related to the chemical properties of the plugging inks. For example delamination was dominated by the inks property of water adsorption, which induced vapor pressure when it undergoes thermal shock testing. The authors have solved the delamination problem by reducing the ratio of water adsorption in the plugging ink.

Keywords

Via on IVH, High density interconnects (HDI), Delamination, IVH barrel crack, plugging ink, moisture adsorption.

1. Introduction

Due to higher pin counts and narrower pitches, the density of the printed circuit boards required by the market today is higher than ever. As a result, the adoption of 'build-up printed circuit board' has become widespread, particularly in the areas of communication fields and industrial devices such as IC testers [1-2]. The method used for manufacturing build-up printed circuit boards generally employs the prepreg process to produce the build-up material and copper plating to ensure electrical connections. In the case of filled via holes, excellent reliability of the individual electrical connections are provided by the micro via holes (MVH). Moreover, an advantage of adopting filled via holes is the via-on-via structure (stacked via hole). This structure, in which filled via holes are stacked, provides more flexibility in the design of circuits and makes it possible to achieve higher density circuits.

However, some of the challenges associated with this technology are related to the proximity of the vias to the surface mount (SMT) and ball grid array (BGA) lands. To reduce inductance and increase density, via pads are being placed close to the SMT/BGA lands. Many designers are searching for methods to resolve these issues while meeting cost objectives [3-5].

With MVH techniques, the authors have already developed an original stacked via method, called Samsung Any Via (SAVIA), to lead the next generation of printed circuit industries. Especially, Via on IVH (VONI) technology is capable of products with very fine geometries resulting in extremely high component density with a high degree of reliability and reproducibility. The VONI technique combines the complex technologies of blind and buried vias in traditional sequential lamination cycles with external layers and MVH for true high-density packaging. The ability to place a via closer to the SMT/BGA land is generally a

function of filling materials, not the printed circuit board (PCB) laminate or prepreg materials [6].

Via fill materials contain 99 %~ 100 % solids and are designed to completely fill the via and undergo little to no shrinkage during curing. They usually have a lower CTE than the PCB resin making them useful for pre-filling blind and buried vias prior to sequential lamination. The intent is to completely fill the via with a material with essentially no voids such that the surfaces are nearly flat. This material is usually plated over with copper during the through hole plating process for the non-filled holes [7-9].

However, when MVHs were stacked on IVHs, there are differences in the thermal expansion of the copper and the glass epoxy base materials. In order to verify the reliability of the stacked via hole connections, a numbers of stacked via hole layers, material types (FR4, high-Tg FR4, low thermal expansion materials, etc.), and IVH diameters (0.2~0.4 Φ). The boards were examined through DC current induced thermal cycling test (TCT) to determine the reliability of the various samples. After TCT, the IVH structure encountered some problems, such as IVH barrel crack, and layer to layer delamination. Both problems are significant for VONI's reliability. IVH delamination induces stacked MVH delamination and barrel cracks can cause open circuits.

In our research on the reliability of these types of connections as functions of base materials, IVH hole size, and plugging inks, it was found that certain design rules and material properties had to be established to ensure the reliability of these products.

2. Experimental Work

2.1 Process of VONI Manufacturing

Figure 1 shows a schematic diagram for the VONI process. Since copper clad laminates (CCLs) and prepregs were built-up by a vacuum press, a CNC drill was applied to make the IVH. The vias were filled with plugging ink and a cap plating layer was added on the filled IVH layer. Furthermore, MVH was stacked on IVH layer by CO_2 layer drilling and a fill plating technique. To apply electric current, all of via holes were interconnected through a plating layer.

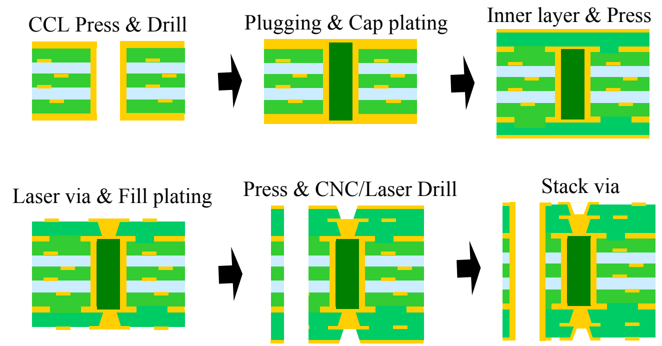

Figure 1: Schematic diagram for the process of VONI manufacturing.

2.2 Design Rules for VONI Structures

Figure 2 shows a schematic diagram for the design rules of the VONI structure. To produce VONI structure in a PCB, accurate design rules and process controls are required. First the plating thickness on the IVH was decided to be a total of 30 μm which contained a base Cu (6 μm) layer, panel plating (9 μm), and cap plating (15 μm). In addition, design rules for the sizes for holes and lands of IVH and MVH were also decided as followings; IVH (hole/land) was decided as 200/450 μm and MVH (hole/land) was as 100/285 μm, respectively. Finally, to achieve these values the process controls for VONI were considered with accumulate Cu thickness and tolerance. The base Cu was 12(-6) μm and ±2 μm, compared with conventional PCB as 12 μm and no spec. Also, 1st panel plating was 24(+18) μm and ±4 μm, compared with conventional PCB as 30(+18) μm and ±4 μm, respectively. For the buff process, it was decided as 15(-9) μm and ±3 μm, and then, 2nd cap plating was decided as 30(+15) μm and ±4 μm.

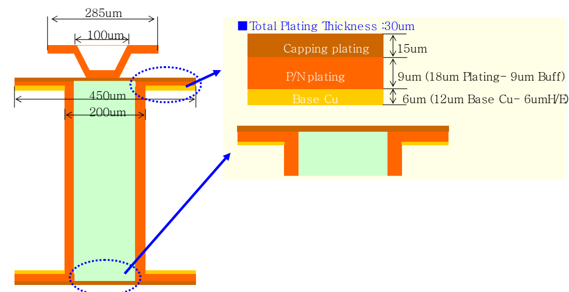

Figure 2: Design rules of VONI structure.

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2.3 Optimization of the Manufacturing Process

To optimize the buff quality for VONI manufacturing, grinding conditions and positioning deviation were thoroughly evaluated. Figure 3 shows various types of infeed directions. Infeed speeds were tested with the range from 1.0 m/min to 2.0 m/min and leveling wheel (L/W) were also evaluated from 1.0 A to 2.0 A. Since the optimal buff condition was selected, positioning deflection during the buff grinding process was compared with conventional condition currently used in production (pressure-high cut 2.0 A, L/W 1.5 A, speed: 1.8 m/min, one time).

To stack MVH on IVH, two plating steps were done on the base Cu (6 μm). The panel plating was 9 μm (18 μm-plating, 9 μm-buff) and the cap plating was 15 μm. Therefore, ideal total plating thickness was 30 μm on IVH. Panel plating was applied with current density (2.2 ASD) and plating speed (0.44 micron/min). To reduce the deflection of plating thickness from 10μm to 5μm, the clamp position of capping plating was evaluated since current density and plating speed were decided as 1.9 ASD and 0.7 m/min, respectively.

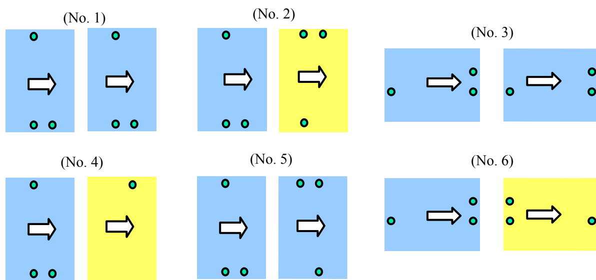

Figure 3: Infeed direction into buff process; Blue color indicated component side on PCB and yellow color represented solder side on PCB, respectively.

2.4 Simulation of VONI Structures with Different Materials

The maximum stress was evaluated with various kinds of IVH hole sizes and raw materials. IVH (hole/land) sizes were tested with 200μm/450μm, 250μm/500μm, and 300μm/600μm. Moreover, various properties of raw materials, such as poisson's ratio, x, y, z axis of CTE, flexural modulus, were used to estimate maximum stress in certain IVH structures.

2.5 Chemical Properties of Plugging Ink

Table 1 lists plugging inks that were used for filling materials in IVH. The plugging inks were carefully selected according to their chemical properties, such as viscosity, Tg, and CTE. Filling condition of plugging ink was changed because IVH hole size was downsizing from 0.3 Φ to 0.2 Φ. The stirring process and screen printing parameters were changed to include vacuum stirring and Slik # 270 (liquid 30 μm) screen instead of Slik # 150.

Table 1: Chemical properties and ingredient of plugging inks for IVH filling.

		a	b	c	d	f
Viscosity (dap.s/25℃)		500	400	400	400	700
Peel strength (N/cm)		5	8	6~7	8~9	7.8
Filler size		3μm (max.15)	5.2μm (max.15)	2~3μm (max.15)	2~3μm (max.15)	5μm (max.15)
Tg (℃)		154	150	168	160	163
CTE	α1	49	42	39	32	36
	α2	114	111	105	83	83
Water Adsorption		0.86%	0.3%	0.23%	0.15%	0.05%
Filler Ingredient		$CaCO_3$ (50wt%)	$CaCO_3$ SiO_2	$CaCO_3$ (50wt%)	$CaCO_3$ (55wt%)	Cu (80wt%)

2.6 Thermal Reliability Test

Based on the IPC-TM-650 method, we examined the thermal shock reliabilities of these assemblies using temperature cycling and solder shock testing. First, a thermal shock reliability test was performed with 100 cycles under the condition of -65 °C (30 min)/ 10 min/ 125 °C (30 min). And after that, the reliability was evaluated according to the results of resistance change and microsection tests. In addition, samples were dipped in an oil bath (260 °C, 20 sec, 1 cycle), and then its reliability was determined by microsection observation [10-11].

3. Results and Discussions

3.1 Manufacture of VONI

With two different types of layer constructions, named 10HN_C and 10VN_D, settled design rules of VONI were as follows; chip scale package (CSP) pad pitch was 0.5 mm, line/space (L/S) was 75 μm/ 75 μm, Via/Land was 0.1 mm/ 0.25 mm, build-up material was laser drillable prepreg (LD PPG), and IVH/Land was 0.2 mm/ 0.45 mm. Figure 4 shows two different types of manufactured VONI structures.

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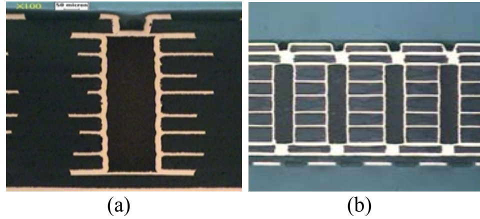

Figure 4: Microsection pictures of two different types of manufactured layer constructions on VONI structures; (a) 10HN_C type, (b) 10VN_D type.

3.2 Consideration of the Buff and Cap Plating Processes

The buff process is essential to stacked MVH on IVH with good registration and shape after the completion of filling the plugging ink into IVH. However, in the mass product process, different buffing amounts would frequently occur according to the board input direction and position. Although this difference had been ignored for the conventional PCB, in the case of VONI structures, it was found to be the dominant factor for structural reliability. We tested the different buffing amounts in 9 positions when samples were inserted with 6 different directions (see Figure 3). Figure 5 shows the buffing amount profiles according to sample infeed direction. Based on the 6 different infeed directions, we measured 9 points on the component and solder sides of the PCB panels. As shown in Figure 5, the samples that were inserted by no. 5 and no. 6 directions indicated higher buff amounts, however, these conditions were difficult to apply in manufacturing because of reduced productivity. Among the other samples, the specific sample (no. 3) showed the average amount of grind as 8.9 μm and a small declination of buff amount as 1.3 μm between each point in the PCB panel.

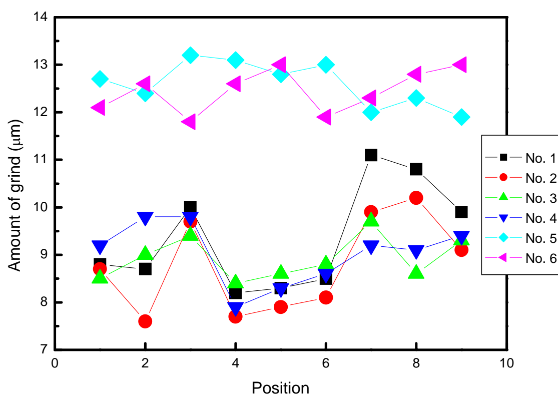

Figure 5: Amount profiles of grind according to the infeed directions and buff positions.

Figure 6 shows the declination of grinding amount between the component and soldering side. According to the result from Figure 6, the buffing amount on the component side, which was inserted first into the buff process, was larger than on the soldering side, at 0.7 μm. It was considered that infeed order could affect the grinding amount. Compared with the grinding amount on the solder side, the component side indicated 1 μm higher grinding amount and lower declination between each point.

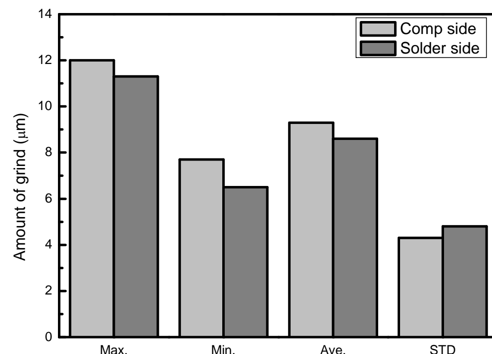

Figure 6: The comparison of grind amounts on the component side and soldering side.

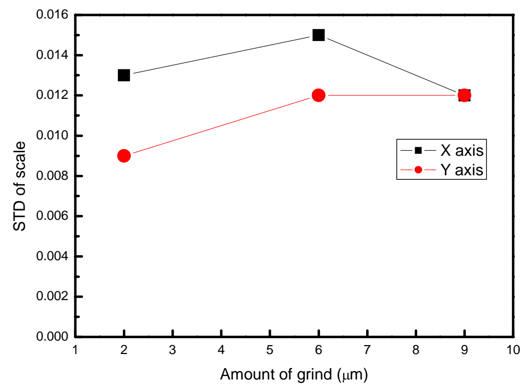

Figure 7: Scale changes of X and Y directions on PCB panels as a function of grind thickness.

The authors also investigated the scale change after the buff process because scale changes induce serious problems such as errors in layer registration and delamination.

Figure 7 shows the scale change in the X and Y directions on PCB panels after the buff process. The buff process was tested with 3 different conditions as follows; 2 μm (2.0m/min, one time), 6 μm (1.5m/min, 2 times), and 9 μm

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(1.0m/min, 2 times). As shown in Figure 6, the grind amount affects the X and Y axis scale. The smallest changes were obtained when the 9 µm condition was used for the grind amount.

The vertical electroplating process, which was used for cap plating in the VONI manufacturing process, was adopted with the cathode as the clamp. However, the electrical field on the cathode surface is never uniform, and therefore induces a difference in the deposit thickness. While there will be a perfect balance of the quantity of charge passed through the cell and the quantum of metal deposited, there is no control on the distribution of the deposited metal over any given cathode surface. There are many attempts to obtain uniform deposit thickness in electrodeposition, such as current thieving, shielding, directional anodes, conforming anodes, and pulse current. Based on these attempts, we tried to obtain uniform plating thickness by changing the clamp position during the cap plating process, named panel plating (PNP), and repeating the process for a total of two platting steps.

Table 2 shows the effect of clamp position on plating thickness. The electric field density on the cathode substrates, was highly concentrated at the lower edge of cathode substrate, therefore, panel plating was much thicker in this location than at the center and upper edges. Through two panel plating steps, we tried to obtain uniform electric fields by change the clamp position between the two processes. As a result, we reduce the thickness deviation of cap plating from 10 µm to 5 µm.

Table 2: Thickness of cap plating when two PNP processes were applied on CCL.

		Deviation of CCL (µm)			
		Avg.	Range	STDEV	DEV%
CCL (0.6T H/H)		17.4	0.9	0.22	1.3
1st PNP		35.2	3.9	0.76	2.2
2nd PNP	Clamp (same position)	58.3	6.5	1.3	2.2
	Clamp (reverse position)	58.8	4.2	0.9	1.6

*1st PNP was done under the condition of 2.2 ASD, 0.7 m/min.
**2nd PNP was plated under 1.9 ASD, 0.7 m/min.

3.3 Thermal Stress Simulation for VONI Structures

To predict the results of thermal shock reliability test, we investigated thermal stress simulations with variations between IVH sizes and build-up materials. At the same temperature conditions, thermal stress distributions on IVH structure were simulated from -65 °C to 125 °C. For all of the simulated results, it was known that the maximum strain stress was distributed at the center of the IVH. Figure 8 shows the simulated results of thermal stress distributions. According to the simulation results, we investigated the maximum strain stress for the different materials at -65 °C and 125 °C.

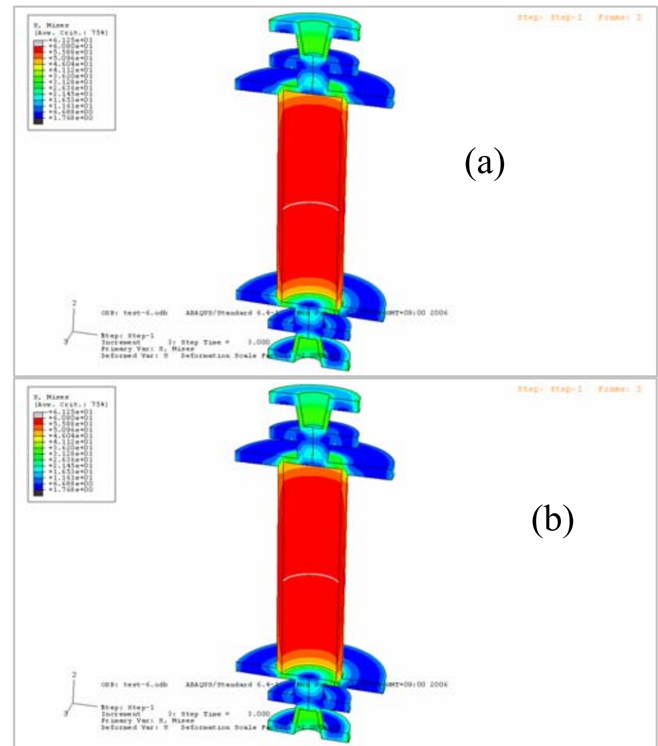

Figure 8: Simulation of thermal stress distribution after thermal cycling from -65 °C to 125 °C; (a) thermal stress distribution between 25 °C and -65 °C, (b) thermal stress distribution between 25 °C to 125 °C.

The authors tested 6 cases as follows; case 1 was with low Tg/middle Tg materials were used for core/lay up materials and the IVH hole size was used as 0.2 *Φ*, case 2 was middle Tg/middle Tg and 0.2 *Φ*, case 3 was high Tg/high Tg and 0.2 *Φ*, case 4 was high Tg/high Tg and 0.25 *Φ*, case 5 was high Tg/high Tg and 0.3 *Φ*, and case 6 was high Tg non filler/high Tg filler and 0.2 *Φ*. Furthermore, case 7 was used to represent the combination between IVH size and materials used in the conventional process. Figure 9 indicates strain stress distributions with different bases material and IVH hole sizes. As shown in Figure 9(a), the smallest strain stress was distributed in sample 6 when the core (high Tg non filler) and lay-up (high Tg filler) were combined as build-up materials. Also, we predicted the accumulated stress after

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thermal cycling test (100 cycles). The results are shown in Figure 9(b). Equivalent plastic strain (PEEQ) was indicated by the degree of damage from cycling loading. From the comparison among sample 3, 4, and 5, the larger the IVH hole size the lower the PEEQ value. Although this indicates that large sizes of IVH hole could reduce thermal stress, the effect was not that significant. Therefore, the dominant factor for thermal stress reduction was the combination of proper base materials for the core and lay-up. Samples 2 and 6 were shown to have the highest durability for thermal stress after thermal cycle testing.

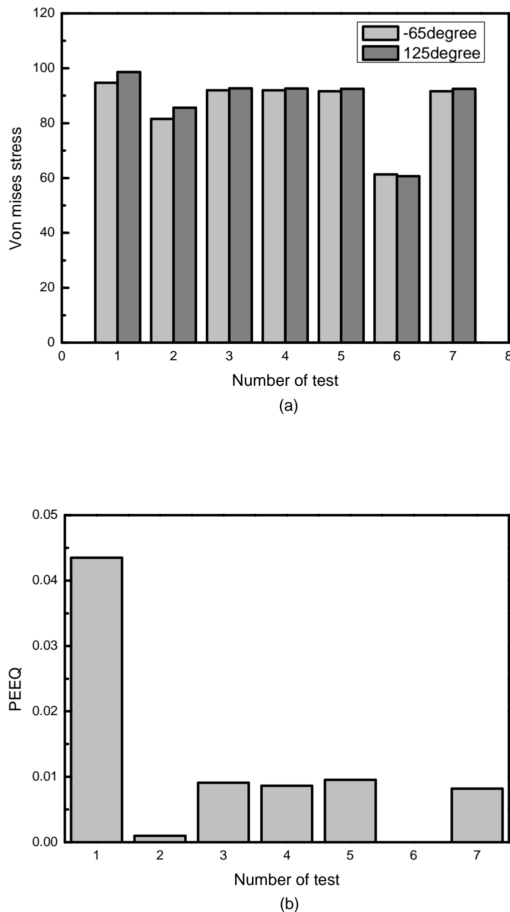

Figure 9: Simulated thermal stress distribution according to base materials and IVH hole size; (a) the comparison of strain stress with 6 cases, (b) PEEQ values which were calculated from the variations between IVH sizes and build-up materials.

3.4 Effect of Plugging Ink

There are several traditional examples of the types of applications that require a via fill process capability: preventing acid residue from attacking the Cu plating at the through-hole opening, which can in turn cause an open circuit, preventing mishandling due to loss of vacuum during board-level assembly or during vacuum-assisted transport in production, preventing blowout of flux and/or solvent residue during assembly and solder reflow, preventing flux from dripping through holes to the opposite side of a PCB, preventing solder resist ink from migrating into through-holes during screen printing, which can cause formation of nodules at the through-hole opening during solder plating and/or gold plating. Additional examples include: enhancing planarity of solder resist on the surface of filled through-holes and for planarity of the core layer, enhancing stability of solder paste printing volume for via-in-pad designs, and finally, preventing migration of solder into through-hole in via-in-pad designs. The filling of through-holes with nonconductive resin and conductive materials using dispensing, screen-printing, and roll-coating methods has been extensively evaluated and tested. Of the three basic methods described earlier, screen printing is the most common process that allows for efficient, selective filling of large numbers of through-holes [12-13].

To stack MVH, the IVH should be filled with ink in its inner layer because panel plating and cap plating must placed on the top of IVH. To fill the vias with ink, we had been using the screen printing method, however, there were problems with insufficient fill using this conventional process because the IVH hole sizes became smaller from 0.3 Φ to 0.2 Φ. In order to address this issue of smaller IVH hole sizes, we changed the silk fabric of the screen, the squeeze speed, and stirring pattern. Using these improved conditions, the insufficient fill problem was solved with increased fill capability, such as speed and stirring (see Table 3). However, there was still a problem remaining for the reliability although the fill problem was resolved.

The IPC reliability test of small diameter holes has established that 100 cycles of thermal cycling, between -65℃ to +125℃, with 30-min dwell time at each temperature extreme is the most discriminating test to distinguish between holes of good and poor reliability. This test reveals both early life and wear out failures. In order to satisfy the reliability requirements, the IVH must meet two criteria: a solder float test and temperature cycling tests such as IPC-TM-500. The solder float test simulates soldering and rework operations in the manufacturing process. The evaluation of the reliability after this test is usually done by inspection of microsections.

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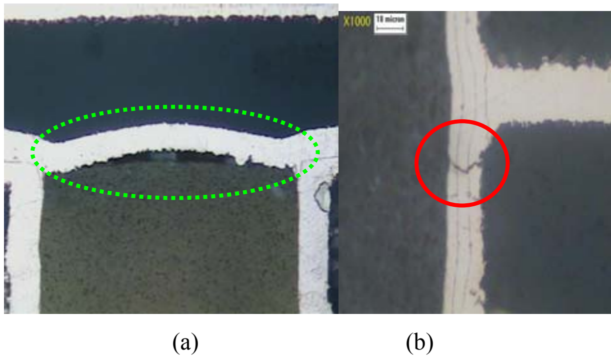
Table 3: IVH via fill conditions

		Conventional condition	Improved condition
IVH hole size		0.3 Φ	0.2 Φ
Screen		Silk#150 (15 μm)	Silk#270 (30μm)
Plugging jig		Step height jig	Step height jig
Squeegee angle		75°	75°
Squeegee pressure		80 kgf	80 kgf
Squeegee speed		0.15 m/s	0.4 m/s
Stirring		Atmosphere	Vacuum
Dry	Pre-cure	135 °C, 20 min	80 °C, 30 min 130 °C, 20 min
	Main cure	150 °C, 30 min	150 °C, 30 min

When VONI was repeatedly subjected to thermal stress IVH barrel cracks, layer-layer delamination was observed in some samples. Some examples of VONI structures with these reliability problems are shown in Figure 10.



(a) (b)

Figure 10: Schematic diagram of VONI and its reliability problems; (a) IVH delamination, (b) IVH barrel crack.

Both problems are serious issues for VONI's reliability. IVH delamination induces stacked MVH delamination and barrel crack can cause open circuits. Normally, it has been thought that these phenomena were dominated by the difference in thermal expansion between the copper plate and the base material. However, the effect of moisture was frequently ignored because these reliability problems were induced by thermal cycling test, thermal shock, and reflow tests. Moisture in the base materials is vaporized when it is settled under severe high temperatures, and then the vapor pressure induces crack and even popcorning. Therefore, to solve VONI's reliability problems such as IVH barrel crack and layer-layer delamination, we have investigated the relationship between the CTE difference and the effect of moisture.

As shown in the experimental section, reliability problems only occurred when a specific plugging ink (sample a) was used. The results of the dipping test indicated that layer-layer delamination occurred in some samples. The delamination was related to the chemical properties of the plugging inks. As shown in Table 1, compared with the CTE value of sample a, other plugging inks had relatively lower CTEs. However, it was initially thought that the degree of the difference between CTEs was not a strong factor for inducing layer-layer delamination. Actually, table 1 shows that the delamination was dominated by the property of water adsorption, which was induced vapor pressure when it undergone thermal shock testing. According to this result, we solved the delamination problem by reducing the ratio of water adsorption in the plugging ink. Compared with the results when the base material changed, IVH delamination and barrel crack formation were independent of the properties of the base materials. As a conclusion, IVH reliability problems were mainly affected from the properties of plugging ink, especially, moisture adsorption.

4. Conclusions

To develop advanced PCBs, the most important issue is the optimized IVH structure because MVH should be clearly placed on the top of IVH. Therefore, we focused on the optimization of the process controlling factors such as the design rules, buff condition, cap plating method, distribution of thermal stress, and especially the via fill ink for IVH. As a design rules for VONI structure, several rules were decided as followings; plating thickness on the IVH was decided to be a total of 30 μm which contained a base Cu (6 μm) layer, panel plating (9 μm), and cap plating (15 μm). Moreover, design rules holes and lands of IVH and MVH were also decided as follows: IVH (hole/land) was decided as 200/450 μm and MVH (hole/land) was as 100/285 μm, respectively. The buff condition, that played an important role in the plating clearance and lamination of plating layer, was investigated with infeed conditions and scale change of X, Y axis by the comparison of the grinding amounts. According to the comparison of 6 cases, the No. 3 method was decided as the optimal buff condition with 9 μm (1.0m/min, 2 times) of grinding amount. The declination of cap plating was optimized to obtain a uniform plating thickness through a change of the clamp position. As a result, we reduced the thickness deviation of cap plating from 10 μm to 5 μm. Finally, the optimization of the via fill ink, which had been considered as the main factor to fabricate versatile advanced PCB with the IVH structure, was carefully investigated with several fill methods, reliability testing, and changes in the ink properties. The fill method was optimized as follows for small IVH hole sizes (from 0.3 *Φ* to 0.2 *Φ*): the silk fabric of the screen was changed (silk#270 (30 μm), squeegee speed (0.4 m/s), and stirring pattern (vacuum). Based on the improved conditions, the insufficient fill problem could be

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solved with increased fill capability. It has been demonstrated that the layer-layer delamination and barrel cracks were caused by vapor pressure from moisture in the fill ink. Therefore, 6 different via fill inks were investigated to reduce the amount of water adsorption and a new ink was demonstrated to resolve the reliability problems. As a result of that, we achieved versatile advanced PCBs with VONI structures.

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