A New Method of Determining the Thermal Resistance of Microelectronic Packages

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Abstract

A critical literature review on the determination of thermal resistance in a package is presented. Finite element simulation of three types of packages, namely, Leadless Chip Carrier (LCC), Bump Chip Carrier (BCC) and Plastic Ball Grid Array (PBGA) as representative of the packages used in the electronic industry, is carried out both at package level and board level separately. Based on the results obtained from 204 simulations, a new methodology of determining the junction temperature even in cases where the specification of the board is not known a priori is developed. The prediction of the junction temperature from the new methodology agrees well with the results of the package and the board simulated simultaneously. The junction temperature obtained by simulation agrees well with experimental data or literature value. A methodology is presented to transform the results for a JEDEC standard board to a non-JEDEC standard board. The coefficient of performance of a non-JEDEC standard board has been introduced and evaluated. The effect of junction temperature in a given package on the reliability has been investigated. Some cases where components failed due to temperature effect are presented.

Key words

Thermal resistance, JEDEC, footprint, junction temperature.

1. INTRODUCTION

The current technologies trend for electronic packaging and interconnects places great importance and focus on the miniaturization, lower weight, less power consumption, increased functionality, advanced interfacing, wireless connectivity, fashionable styling, and environmental friendliness. The market is characterized by reduced product-life-cycle, increased production volumes, faster time to market and increased complexity and diversity of the products. To keep up with these changes, processes used for electronic packaging and assembly have to change. Consequently, many innovative electronic packages were developed and processed in meeting this market demand.

Thermal resistance from junction to case (θ_{jc}) or junction to ambient (θ_{ja}) is used in electronic packages. The JEDEC (Joint Electron Device Engineering Council) [3] definition of thermal resistances θ_{ja} is a measure of the ease of heat flow from the junction (active circuitry on the die surface) to air for a package mounted to a test board and located in either the natural convection chamber or a wind tunnel. Since the standard test environment and board design differ significantly from those in many applications, the proper use of θ_{JA} is to provide a thermal performance ranking of packages and not to simulate a particular end-use application. On the other hand, θ_{jc} indicates the ease of heat flow from the junction to the top or bottom surface of the package (the case), which, during the test, is kept in contact with an isothermal surface. This quantity relates to the

thermal performance of a package when used with an external heat sink. In a particular environment, the thermal resistance for heat to flow from the junction to location X is determined from the following equation:

$$\Theta_{JX} = \frac{T_j - T_x}{P} \qquad (1)$$

where TJ is the junction temperature, TX is the temperature at the specified location, and P is the total dissipated power.

The JEDEC standard is being developed to create a uniform method of characterizing IC packages in order to establish a frame work by which the performances of different packages housing similar devices, or different devices in similar packages, can be compared. The standard consists of different documents, some of which are still being developed. The approved documents to date include JESD51 (Overview), JESD51-1 (The Electrical Test Method), JESD51-2 (Natural Convection Environment Standard) and JESD51-3 (Low Thermal Conductivity Test Board for Leaded Surface Mount Packages). So far, only surface mount boards have been addressed.

The JEDEC JC-15.1 subcommittee which is responsible for developing this standard is presently working on board specification for through-holes and other packages. Other documents that are yet to be completed and approved include Infrared Test Method, ETM Implementation, Forced Convection, Heat Sink, High Conduction Thermal Test Boards, Resistive Heating Thermal Test Die, Active Device Thermal Test Die, and Thermal Modeling. The list may grow in the future to accommodate inputs from the industry and changes in packaging technologies. The present greatest challenge is to cope and address the issues arising from many Non-JEDEC packages while attempting to meet current thermal standards in daily routine.

In spite of the existence of several thermal standards, many problems are encountered in determining the thermal resistance of a specific single package. It has been known for a long time that existing thermal resistance θja component characterization techniques are inadequate. The associated errors are too great and uncertain, thus there is a need to evaluate a new methodology for applying the calculated thermal resistance to the actual operating conditions. An attempt is made to provide the connectivity between JEDEC and non-JEDEC thermal resistance results. This is carried out by splitting the problem into two portions in which the package and PCB thermal resistances will be determined separately and matched for a given operating environment. In this case, the common element that links the package-PCB thermal resistance is the footprint temperature of the package and PCB temperature at package footprint locations.

The objective of this paper is to establish a new methodology of determining the thermal resistances of a package taking into account the actual operating conditions. Thus, the scope of the present work is to divide the effort into the following steps:

i. Evaluate the package thermal resistance exposed to a given ambient with respect to several footprint temperatures.
ii. For a given temperature at the footprint of the package, the heat dissipation capability of the PCB under various environmental conditions is evaluated.
iii. To match the performance of the package and the board for a given environment.
iv. Connecting the results obtained for a standard JEDEC board to a non-standard JEDEC board.

2. ANALYSIS

The above objectives are achieved by performing a series of numerical analyses on a selection of different types of electronic packages. Finite element analysis (FEA) is carried out using commercially available software, ANSYS. ANSYS is capable of performing static, dynamic, heat transfer, fluid flow and electromagnetic analyses. In this case, all the analyses carried out are 3-dimensional steady state heat transfer thermal analysis. Three types of industry marketed packages are selected in the above-mentioned study. They are Leadless Chip Carrier (LCC), Bump Chip Carrier and Plastic Ball Grid Array (PBGA). The selection criteria is based on the overall package size ranging from 1.2 x 1.4mm to 27.0 x 27.0mm, mounting technology and other factors that are in line with current electronic packaging trends and requirements.

The LCC consists of a ceramic substrate with vias to connect bond pads on one side, with solder pads on the other side. Die is mounted on the substrate and connected with wire bonds to the bond pads. In addition, the internal and external contact metals are connected through Tungsten filled vias for electrical grounding as well as thermal dissipation. Die and wire bonds are encapsulated with molded epoxy compound. The cross-sectional schematic of a LCC assembly is indicated in Fig. 1. The overall package size of an LCC is 1.4mm x 1.2mm with the package height not exceeding 0.8mm. The Silicon semiconductor die size used in this FEA was 0.26mm x 0.26mm x 0.20mm. However, this LCC package is capable of housing die sizes up to 0.6mm x 0.6mm. The design of an LCC package is an adaptation of chip-scale packaging technology which is meant to provide viable solutions to the space restrictions found in the newer generation of hand-held and portable

electronic products such as handset, digital camera, mobile computer, memory card, modem, etc.

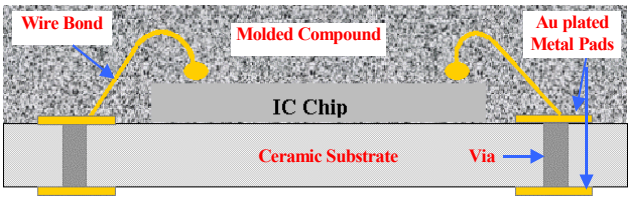

Figure 1. Cross-section schematic of LCC package.

In addition, a low effective thermal conductivity printed circuit board (PCB) based on JESD51-3 standard is also modeled for LCC mounting in a θja study at varying airflow velocities in forced convection. Currently, there is no JEDEC standard PCB available for small packages like an LCC. Therefore, the PCB type for package sizes measuring less than 27mm as stated in JESD51-3 is used in this study. The thermal conductivity of each material as well as other important dimensions and parameters are summarized in Table 1 and Table 2 respectively.

Table 1
Thermal conductivity of material used in LCC and JEDEC PCB

Component	Thermal Conductivity (W/mK)
Die (Silicon)	150.0
Encapsulant (Mold compound)	0.60
Ceramic Carrier (Alumina)	16.7
Thermal Via (Tungsten)	163.3
Metallization (Au/Ni)	150.0*
Die Attach	2.50
FR4 PCB substrate	0.38
JEDEC PCB Copper Trace Layer	386

* The effective thermal conductivity of the Au/Ni metallization is calculated as follows:

Au thickness = 0.5um, K_{Au} = 300 W/mK

Ni thickness = 1.27um, K_{Ni} = 90 W/mK

$$K_{effe.} = \frac{1.27 \times 90 + 0.5 \times 300}{1.77} \approx 150 \text{W/mK}$$

Table 2
Important dimensions and parameters for LCC simulation

Component & Parameter	Dimension (mm)
Package Size	1.4 x 1.2 x 0.8
Chip Size	0.26 x 0.26 x 0.2
PCB Size	114.3 x 76.2 x 1.57
PCB Trace Thickness	0.071
Die Attach Thickness	25.0 [μm]

The BCC package selected in this study is larger than the LCC package, has 32 pins and measures 5.0mm x 5.0mm x 0.8mm with thermal pitch of 0.50mm.

BCC is a leadless surface mount package that uses array lands on the bottom of the package to provide electrical contact to the board. It also has an enhanced thermal design through the incorporation of an exposed die attach paddle on the bottom of the package surface to provide an efficient heat path when soldered directly to the board. This metal paddle or bump consists of 4 layers of different metal structures including the outermost layer of plated Gold material measuring less than 0.01mm. These layers of material are combined with the solder paste as a single material with total thickness of 0.05mm and equivalent thermal conductivity during solid modeling. The cross-sectional view of BCC is shown in Fig. 2.

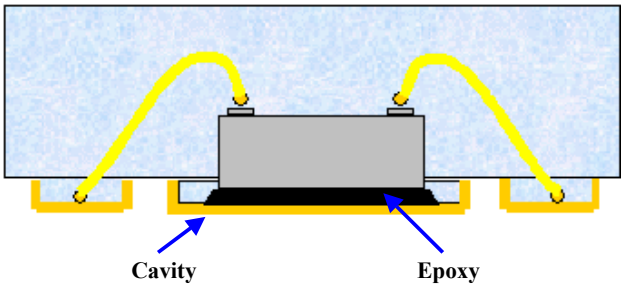

Figure 2. Cross-sectional structure of BCC.

In view of the BCC package geometrical symmetry about two axes, only a quarter model is used for the thermal analysis. Similar to the LCC dealt previously, the BCC package is also modeled with a JESD51-3 standard PCB for θ_{ja} simulation at varying airflow velocities in forced convection. The thermal conductivity of each material as well as other important dimensions and parameters are summarized in Table 3 and Table 4 respectively. The solid modeling approach and boundary conditions for BCC simulation are similar to the ones used in LCC thermal

analysis study, hence no further illustration is indicated here.

The PBGA package used in this study is adopted from the Amkor's [5] PBGA family with the overall package size of 27mm x 27mm, 225-pin counts. It is designed with 15 x 15 full array solder ball matrix at 1.50mm ball pitch. It consists of a silicon IC, gold wires, die attach ad pad, molding compound, BT epoxy substrate, solder balls, vias for ground/signal/thermal, plated copper conductor, and a solder mask. Most of the PCBs for PBGA applications are made of FR4 epoxy/glass. The cross-sectional view of PBGA package is illustrated in Fig. 3.

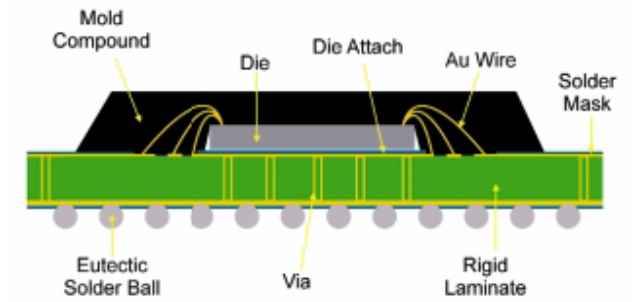

Figure 3. Cross-sectional structure of PBGA225.

Table 3
Materials thermal conductivity of BCC and JEDEC PCB

Component	Thermal Conductivity (W/mK)
Die (Silicon)	150
Encapsulant (Mold compound)	0.67
Die Attach (Silver paste)	3.0
Solder and Bump	51.40
FR4 PCB substrate	0.38
JEDEC PCB Copper Trace Layer	386

Table 4
Important dimension and parameter for BCC simulation

Component & Parameter	Dimension [mm]
Package Size	5.0 x 5.0 x 0.8
Chip Size	2.0 x 2.0 x 0.254
PCB Size	114.3 x 76.2 x 1.57
PCB Trace Thickness	0.071
Die Attach Thickness	5.0 [μm]

A few modifications to the PBGA225 package have been made for simplification purpose and a quarter model is used for 3D finite element model construction. The gold wire and solder masks were neglected in the simulation. The spherical shape solder balls were simplified into a cylindrical taking into account the same volume for both structures. The solder ball height and diameter are modeled at 0.50mm and 0.70mm respectively. The PBGA materials thermal conductivity, package size, JEDEC PCB details, chip power and ambient temperature are summarized in Table 5 and Table 6 respectively.

Table 5
Materials thermal conductivity of PBGA and JEDEC PCB

Component	Thermal Conductivity (W/mK)
Die (Silicon)	150
Encapsulant (Mold compound)	0.70
Die Attach (Silver paste)	5.0
BT Substrate	0.20
Die Pad (Copper)	386
Solder Balls	53
FR4 PCB substrate	0.38
JEDEC PCB Copper Trace Layer	386

Table 6
Important dimension and parameter for PBGA simulation

Component & Parameter	Dimension [mm]
Package Size	27.0 x 27.0 x 2.13
Chip Size	10.0 x 10.0 x 0.7
PCB Size	76.2 x 76.2 x 1.57
PCB Trace Thickness	0.071
Die Attach Thickness	5.0 [μm]

A parametric study of different case temperatures is carried out to obtain the corresponding package thermal profile and junction temperature (Tj) for junction to case thermal resistance (θjc) calculation. The case temperature is actually the temperature restraint that is fixed at the bottom surface of metal contact pad of the package, i.e metallization for LCC and BCC and solder balls for PBGA225. The analysis is performed under natural cooling condition with heat transfer coefficient of 10 W/m2K on the external package surfaces. This methodology is

employed to determine θ_{jc} when the detailed information of PCB is not available. On the other hand, the junction to ambient thermal resistance (θ_{ja} or R_{ja}) is also obtained with the knowledge of junction temperature of a package mounted onto a PCB operating under the forced convection environment. A smaller equivalent size of JEDEC FR4 PCB is used for PBGA225 simulation in order to reduce the discretization and computation time during the simulation.

An important assumption made for the above method is that the PCB attachment to the device must provide sufficient area for heat dissipation to take place and its temperature at any point should not exceed the case or restraint temperature. The boundary conditions used for the thermal resistance simulation for above packages are summarized in Table 7.

The junction temperature and case temperature for each footprint temperature at a given chip power is obtained and the respective thermal resistance is calculated. The effect of varying footprint temperature and chip power on junction temperature, junction-footprint thermal resistance (θjf) and junction-case thermal resistance (θja) obtained from steady state thermal analysis are discussed subsequently.

Table 7
Thermal analysis boundary conditions & loading

Material	Thermal Resistance Analysis
Metal contact	Case Temperature T_c [°C] 30, 50, 70 & 90
Mold Compound	Heat Transfer Coeff. [W/m^{2}K] 0m/s 1m/s 2m/s 4m/s 16.42 54.45 77.00 108.89
PCB	Heat Transfer Coeff. [W/m^{2}K] 0m/s 1m/s 2m/s 4m/s 6.68 13.95 19.72 27.89

The heat dissipation capability of the PCB was carried out by inputting a range of previously established device operating powers onto the package footprint locations of various types of PCB and determines the average PCB temperature at these footprint locations. Basically, there are three types of PCB primarily of different sizes (width and length) that categorized into JEDEC or non-JEDEC type as follows:

i. 76.2mm x 114.3mm x 1.57mm (JEDEC standard, called PCB-S)
ii. 76.2mm x 76.2mm x 1.57mm (Non-JEDEC standard, called PCB-A)
iii. 40.0mm x 60.0mm x 1.57mm (Non-JEDEC standard, called PCB-B).

The center of each package footprint on PCB-S and PCB-A is located at the crossover of 38.1mm x 38.1mm where full or half model will be generated. As in the case of PCB-B, the center of the package footprint is located at the crossover of 20mm x 20mm. A total of 144 simulation runs were performed for JEDEC and non-JEDEC standard PCBs in order to obtain the thermal characteristic of each PCB for LCC, BCC and PBGA packages at different operating environments i.e. natural and forced convection. In this case, the heat transfer coefficient with respect to 0m/s, 1m/s, 2m/s and 4m/s airflow velocity as tabulated in Table 7 is being used throughout the simulation. The symmetrical PCB models of either half or quarter model were used whenever possible depending on the footprint layout of packages to shorten the computation time.

3. RESULTS AND DISCUSSION

The variation of junction temperature with footprint temperature for different chip operating power of each package type are shown in Fig. 4 to Fig. 6. Evidently, the junction temperature varies linearly with footprint temperature for all chip powers. The difference in junction to footprint temperature (or ΔTjf) is calculated to be approximately 20°C with every 20°C changes in the footprint temperature.

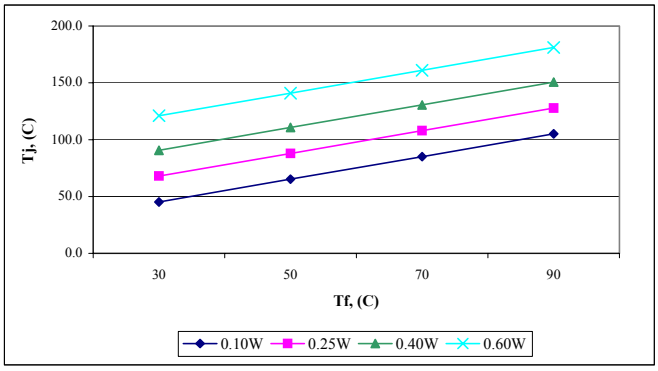

Figure 4. Effect of footprint temperature on junction temperature for varying chip power of LCC.

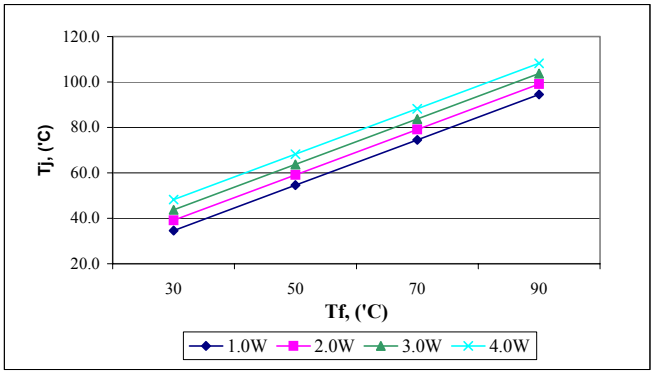

Figure 5. Effect of footprint temperature on junction temperature for varying chip power of BCC.

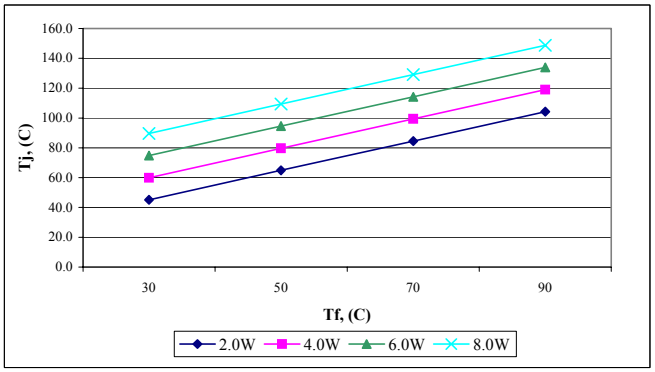

Figure 6. Effect of footprint temperature on junction temperature for varying chip power of PBGA225.

The temperature distribution profiles of each package are obtained from ANSYS postprocessor. However, only a set of results for indicated chip power at footprint temperatures of 30°C are indicated in this paper in view of similar heat dissipation pattern is seen at other operating chip powers. Fig. 7 to Fig. 10 illustrates the temperature profiles of the overall LCC, BCC and PBGA package and the internal construction without the mold compound. It can be seen that the maximum and minimum temperature is always located at Silicon die and package footprint respectively. This observation is expected as the chip is considered as the heat source and the footprint temperature is restraint during the thermal simulation.

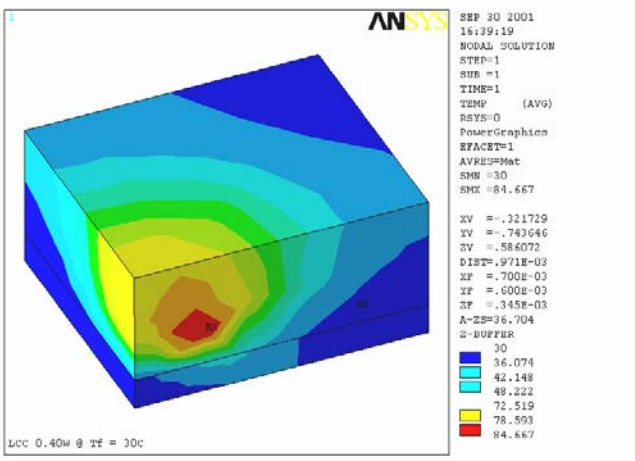

Figure 7. Temperature profile of overall LCC package for T_f at 30°C

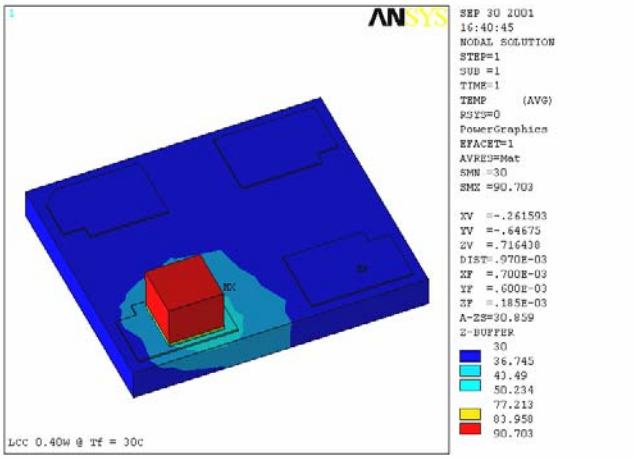

Figure 8. Temperature profile of internal LCC construction for T_f at 30°C.

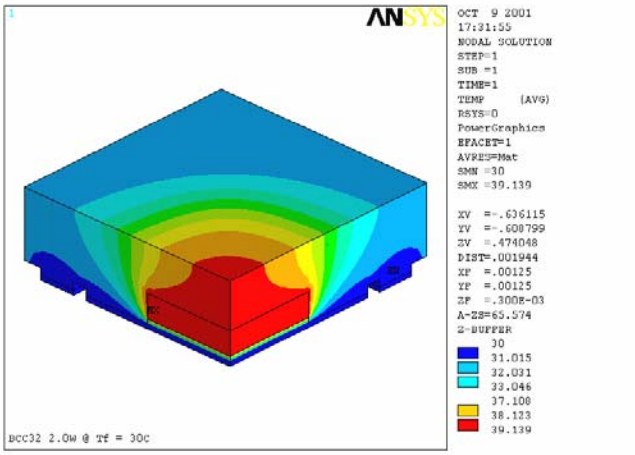

Figure 9. Temperature profile at chip power of 2.0W and T_f at 30°C.

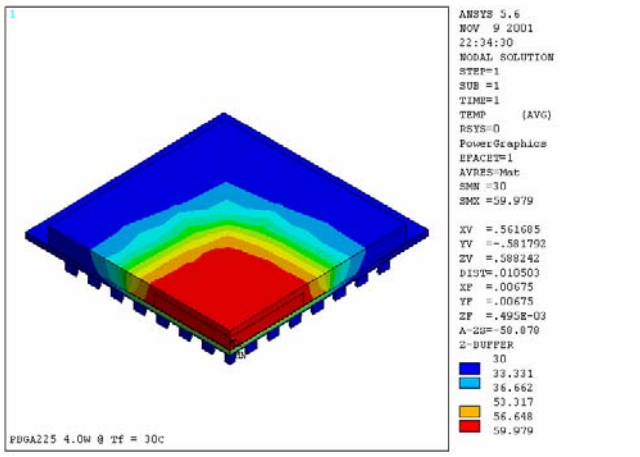

Figure 10. Temperature profile at chip power of 4.0W and T_f at 30°C.

The derived θja simulation results are obtained for both natural convection and forced convection for different airflow velocity of each package as depicted from Fig. 11 to Fig. 13. The typical θja characteristic of decreasing trend with increasing airflow velocity is observed. It can also be seen that the effect of switching from natural (0m/s) to forced convection (1m/s) is well demonstrated with the significant reduction in thermal resistance of 12.76°C/W for LCC package. This observation can be explained as velocity increases, the heat transfer coefficient increases correspondingly. Therefore, more heat can be dissipated through convection mode. However, further increase in airflow rate beyond certain velocity is not productive, as there is only a slight reduction in thermal resistance The discussion on this observation is similar to both BCC and PBGA package and hence not repeated here. The temperature profile plots of each package with PCB for airflow velocity of 4m/s are shown from Fig. 14 to Fig. 16.

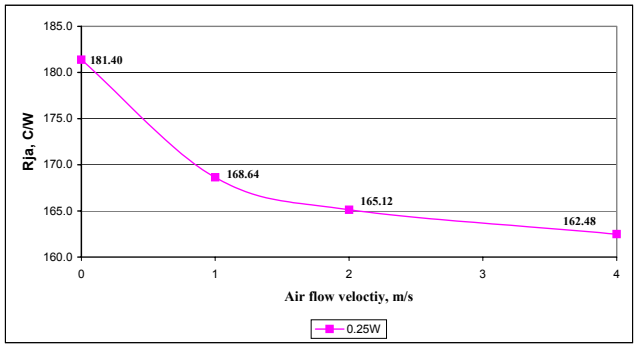

Figure 11. Effect of airflow rate on junction-ambient thermal resistance, θ_{ja} of LCC.

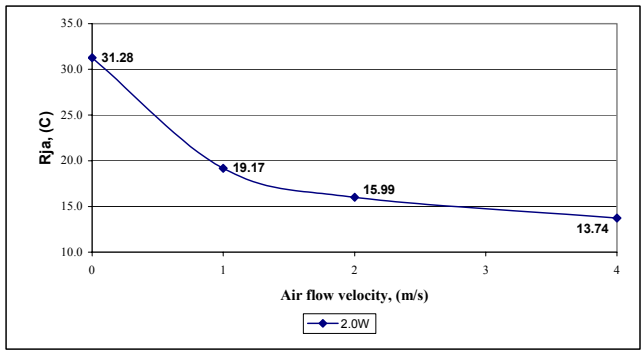

Figure 12. Effect of airflow rate to junction-ambient thermal resistance, θ_{ja} of BCC.

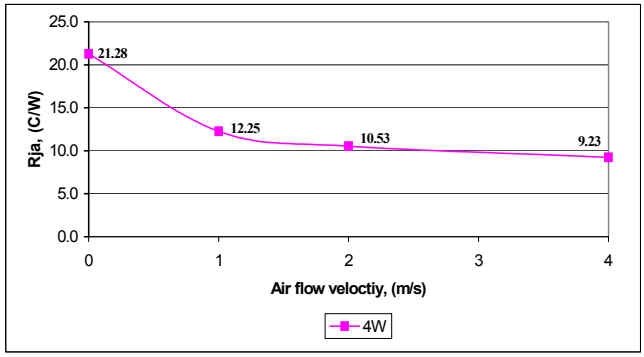

Figure 13. Effect of airflow rate to junction-ambient thermal resistance, θ_{ja} of PBGA225.

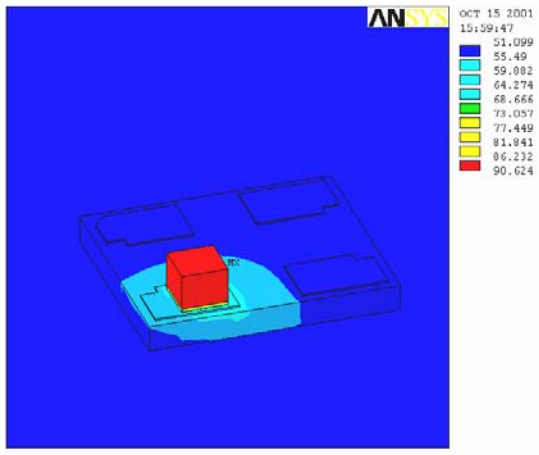

Figure 14. Temperature profile of LCC mount on JEDEC PCB at airflow velocity of 4m/s.

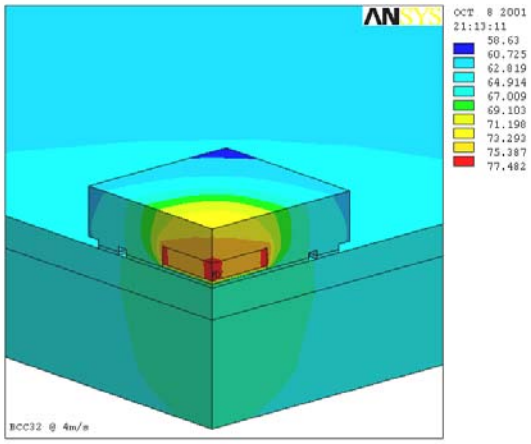

Figure 15. Temperature profile of BCC mounted on JEDEC PCB at airflow velocity of 4m/s.

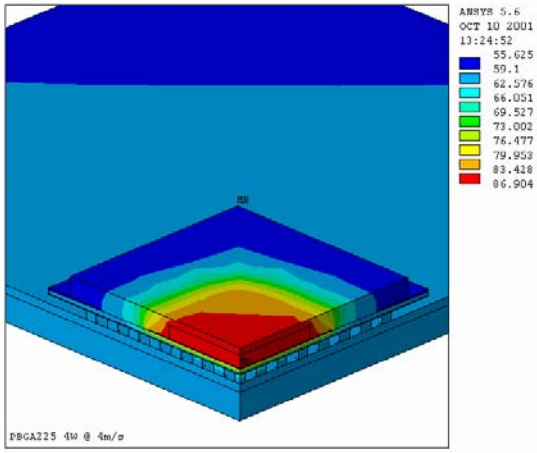

Figure 16. Temperature profile of PBGA mounted on JEDEC PCB at airflow velocity of 4m/s.

It is always recommended that any modeling of a physical phenomenon should be compared with experimental/standard results before the model can be used for the parametric studies through computer simulation. The θjc result of LCC was obtained from the Liquid Crystal (LC) technique. It can be seen from equation (1) that the junction temperature of the device will be virtually the same as the temperature on the surface of the die. Therefore, one can substitute the N-I transistor temperature of the liquid crystal (~130°C) for the Tj in the equation to solve for θjc as follows:

$$\theta_{jc} = \frac{T_{N-I} - T_c}{P_d} \qquad (2)$$

Note: Tc is measured with a thermocouple wire at the case during liquid crystal transition.

The LC measurement was performed on two diodes namely SN1 and SN2. In addition, the measurement was repeated at different biasing powers to obtain a more accurate average θjf value, the measurement results are summarized in Table 8.

Table 8
Summary of LC measurement results

SN	Power P_d (W)	Footprint Temperature T_f (°C)	Channel Temperature T_{ch} (°C)	θ_{jf} (°C/W)
1	0.175	107.0	133.0	148.2
	0.082	120.0	133.0	158.3
2	0.157	110.7	134.6	152.2
	0.028	128.4	133.0	160.4

The average θ_{jf} calculated from LC technique is 154.8°C/W, which is very close to the numerical results of 151.64°C/W that is also obtained as an average for a range of diode operating powers. The error in this case is less than 2%, thus the above numerical methodology used in getting the thermal resistance of LCC has been validated.

In the case of PCB simulation, the board temperature (T_b) at a given airflow condition is being obtained from the simulation and plotted against the range of operating powers. The T_b is defined as average temperature of PCB at the location of package footprints. It is also the location of heat dissipation or power being inputted during the simulation. The plot of T_b against Q for PCB-S are obtained and indicated from Fig. 17 to Fig. 19 for LCC, BCC and PBGA packages.

It can be seen that the Tb increases linearly with heat dissipation at the package footprints across all PCB sizes. This characteristic is identical to the linear relationship of package junction temperature (Tj) and footprint temperature (Tf) at different chip powers. This observation is consistent with the explanation of the primary heat transfer mechanism is through conduction mode for electronic package and it is applicable in the case of PCB.

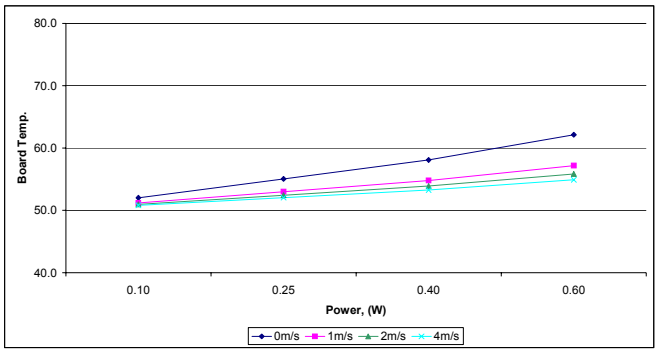

Figure 17. Effect of heat dissipation on LCC footprint-board temperature for PCB-S.

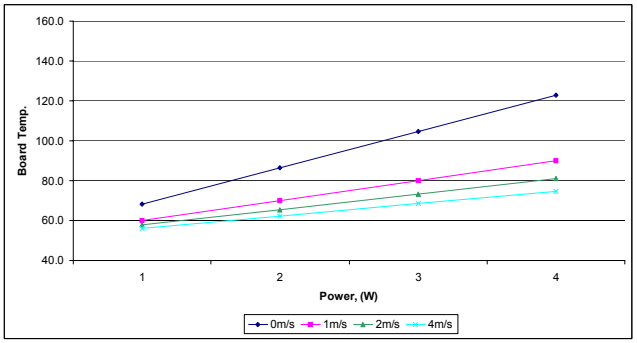

Figure 18. Effect of heat dissipation on BCC footprint-board temperature for PCB-S.

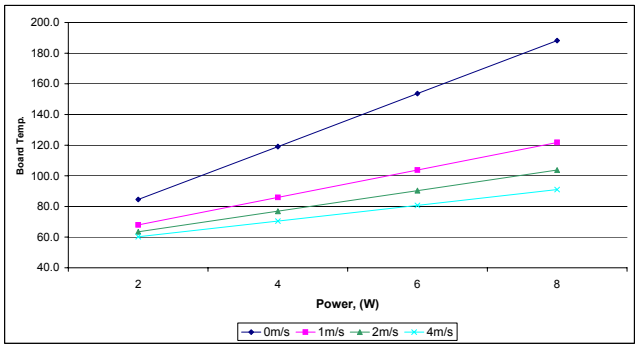

Figure 19. Effect of heat dissipation on PBGA footprint-board temperature for PCB-S.

Based on this set of results, three important relationships with reference to numerical results from the packages can be achieved:

i. To determine the corresponding junction temperature of a given package from a specific heat dissipation of PCB through extrapolation of the plots of T_f against T_j and T_b against Q.
ii. To determine the heat dissipation efficiency of non-JEDEC PCB with reference to JEDEC PCB for each package type.
iii. To match the θ_{ja} results by combining the numerical results of both the package and its mounting PCB.

The above steps can be illustrated by Fig 20 in Appendix I for the case of LCC package mounted on PCB-S as follows:

i. Start from the chip power of 0.25W on the abscissa of the right-side of the figure,
ii. Proceed vertically to meet the curve corresponding to natural convection to get the footprint temperature of 55.06°C.
iii. Proceed horizontally towards the left side of the figure to meet the line corresponding to the chip power of 0.25W.
iv. Proceed vertically downwards to get the junction temperature of the package as 95°C.

The junction temperature obtained by the simulation of the LCC package on the PCB-S board under natural convection is 95.35°C. Thus it can be seen that the present method predicts the junction temperature very close to the simulated results. Fig. 21 shows a graph for LCC package similar to Fig. 20 but for a non-JEDEC board (PCB-A). From this figure, we can determine the junction temperature for a non-JEDEC board following the procedure indicated earlier. Corresponding to the earlier problem mentioned with LCC package, we find that the junction temperature for PCB-A is 97°C which is higher than 95.35°C for PCB-S. We can define the coefficient of performance (COP) of the PCB-A as follows:

$$T_{jPCB\text{-}S} / T_{jPCB\text{-}A} = 0.98$$

Fig. 22 and Fig. 23 shows for the BCC and PBGA package corresponding to Fig. 20 for LCC package. Based on the procedure used in LCC package, we can determine the junction temperature of BCC and PBGA package for a JEDEC board to be 95°C and 140°C respectively. The error for PBGA package was calculated to be 3% as compared to the board and package simulation value of 135.12°C. The estimated junction temperature value for the non-JEDEC board (PCB-A) in the case of BCC and PBGA were 111.0°C and 178°C as depicted in Fig. 24 and Fig. 25 respectively. Therefore, the calculated COP for BCC and PBGA are as follows:

$$\text{BCC:} \quad T_{jPCB\text{-}S} / T_{jPCB\text{-}A} = 0.86$$
$$\text{PBGA:} \quad T_{jPCB\text{-}S} / T_{jPCB\text{-}A} = 0.79$$

In case the package is operating in a forced convection situation, say at an airflow velocity of 1m/s, the above procedure is repeated with left-side of the figure should be

replaced by the forced convection situation with an airflow velocity of 1m/s. However, this figure is not shown here. In order to make use of the above method, it is necessary to get the following two graphs:

i. Run the simulation of the PCB alone with the different average footprint against various cooling conditions and thus a graph of average footprint against power dissipated for various cooling conditions is obtained. These types of graphs have to be generated for various JEDEC PCBs with different trace layers (1oz. or 2oz. etc). This step is common for all packages and hence it is to be carried out only once.

ii. Run the simulation of the package under development to obtain the junction temperature for various footprint temperatures and chip powers in a given cooling environment. Thus, for each cooling environment we do get a specific graph for a given package.

4. CONCLUSION

Thermal analysis of three different packages, varying in size and technology has been carried out using FEM for various operating conditions. Both the package and PCB have been evaluated separately as a function of footprint temperature for various parameters. A total of 204 simulations are carried out during the investigation. From the analysis the following conclusions are drawn:

i. The junction temperature of the package is found to vary linearly with the footprint temperature for all the packages. The simulations are in good agreement with either experimental data (Liquid Crystal Technique) or available data in the literature.

ii. The average footprint board temperature (T_b) is also found to vary linearly with the power dissipated.

iii. Based on the above two observations, a new methodology is presented for the evaluation of the junction temperature for any given operating conditions. The predictions are in good agreement with the simulation of the combination of the package and the board. The theoretical basis of the new methodology is also presented. This new methodology is also applicable in cases where the specification of the PCB is not available a priori.

iv. A method is suggested to transform the results using a JEDEC board to a non-JEDEC board and vice versa. Coefficient of performance of a non-JEDEC board is also introduced.

APPENDIX I

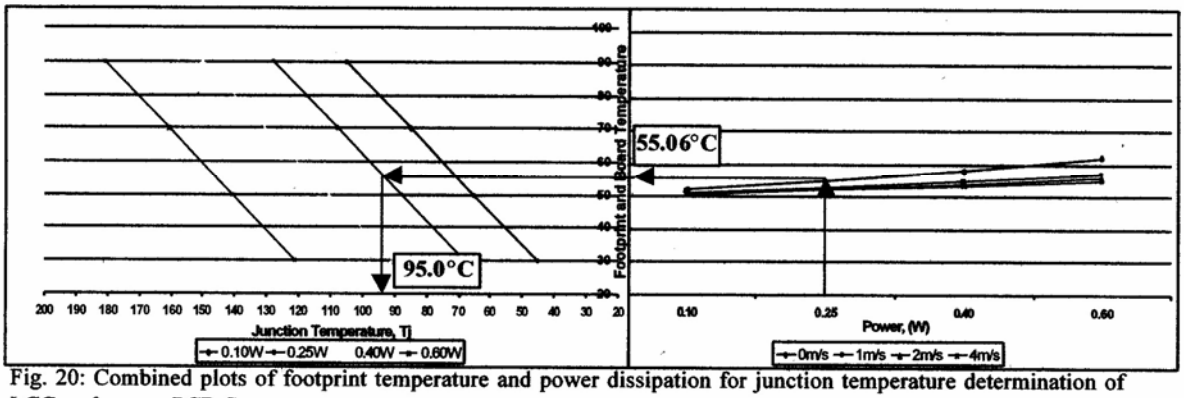

Fig. 20: Combined plots of footprint temperature and power dissipation for junction temperature determination of LCC package on PCB-S.

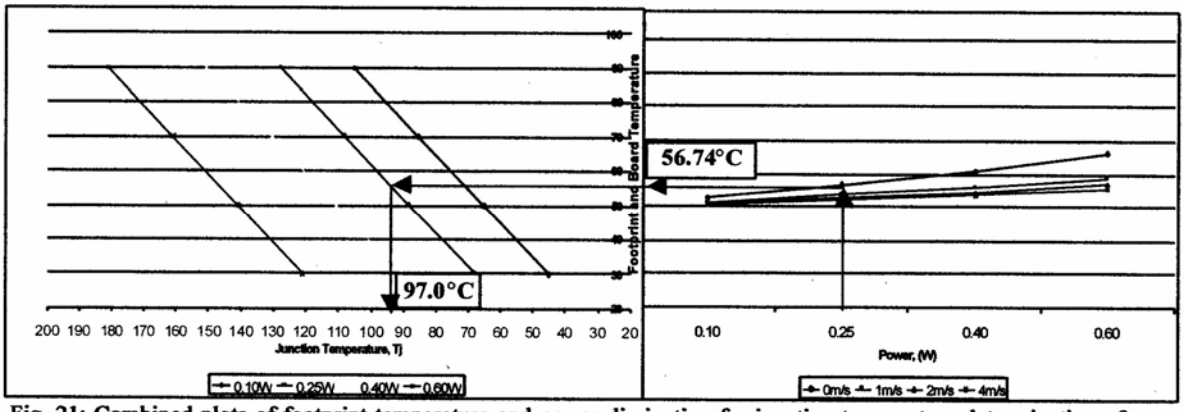

Fig. 21: Combined plots of footprint temperature and power dissipation for junction temperature determination of LCC package on PCB-A.

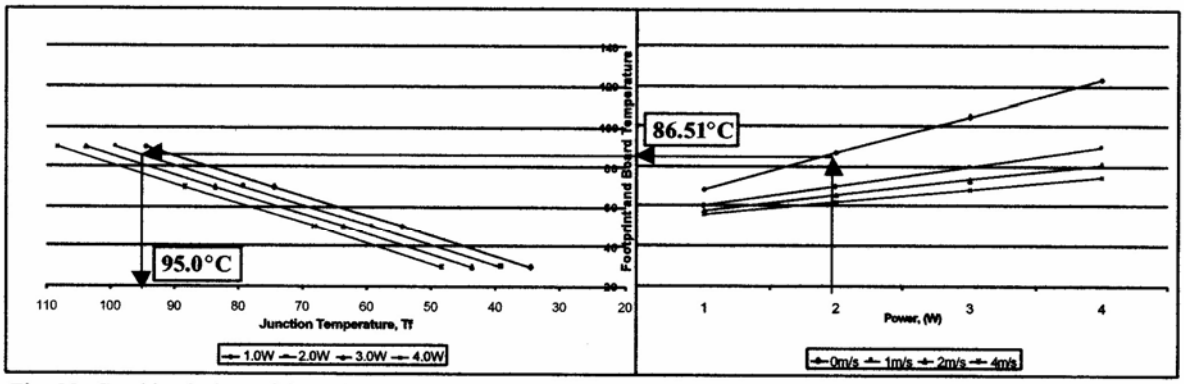

Fig. 22: Combined plots of footprint temperature and power dissipation for junction temperature determination of BCC package on PCB-S.

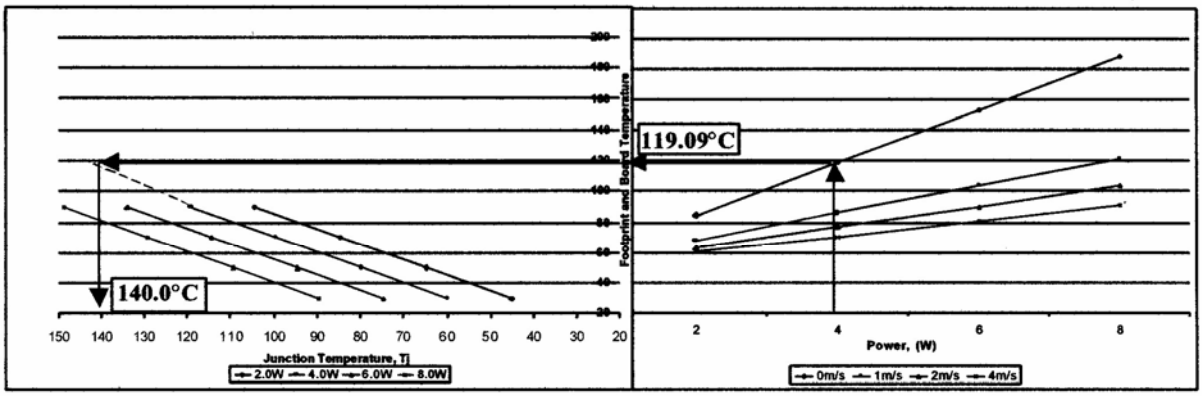

Fig. 23: Combined plots of footprint temperature and power dissipation for junction temperature determination of PBGA package on PCB-S.

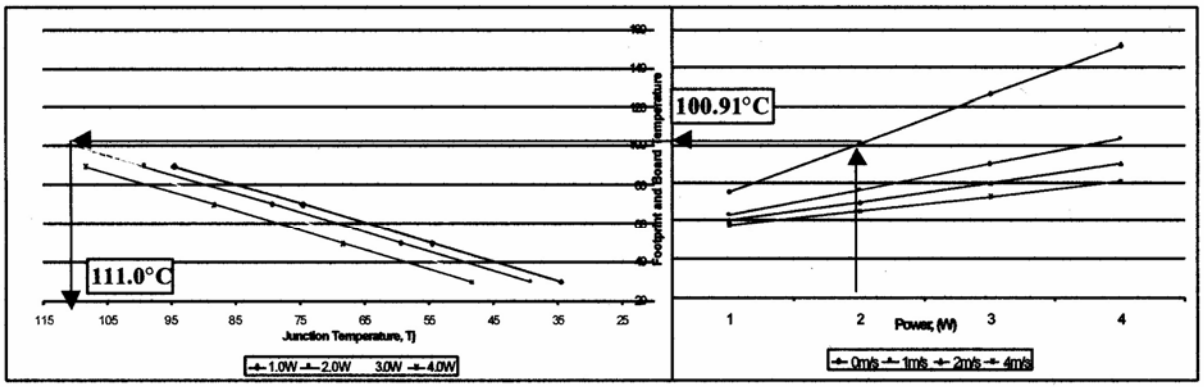

Fig. 24: Combined plots of footprint temperature and power dissipation for junction temperature determination of BCC package on PCB-A.

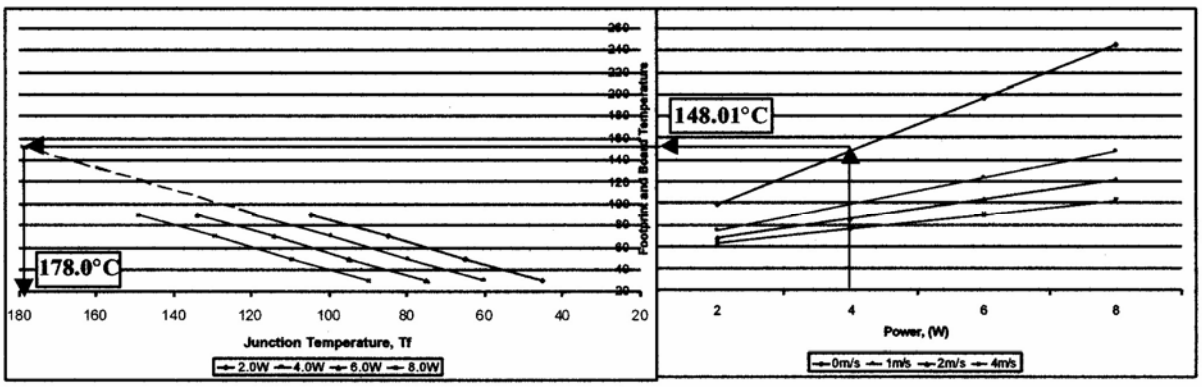

Fig. 25: Combined plots of footprint temperature and power dissipation for junction temperature determination of PBGA package on PCB-A.

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BIOGRAPHIES

King-Long Teoh received his degree in Material Engineering in 1996 and Master degree in Mechanical Engineering (thermal management) in 2002 from University Science of Malaysia (USM). He started his carrer in 1996 with Hewlett-Packard Malaysia as Failure Analysis (FA) engineer working on wide range of LEDs products. He is currently working as a FA specialist engineer in Agilent Technologies Malaysia focusing primary on various types packaging and ICs related failure analysis for RF and microwave Monolithic Microwave Integrated Circuit (MMIC) devices and power modules. His research interests include interconnect and packaging technologies of microwave devices and advanced failure analysis techniques development. King Long has authored and co-authored several published papers on thermomechanical analysis of electronic packages and failure analysis techniques in conference proceedings.

Prof K.N Seetharamu graduated from Mysore University in Mechanical Engineering in the year 1960. He obtained his Masters Degree in Power Engineering in the year 1962 from Indian Institute of Science, Bangalore, India. He obtained his doctoral degree in 1973 in the field of heat transfer from Indian Institute of Technology, Madras, India.

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He has published more than 300 papers in International Journals and conferences. He has authored and co-authored two books on FEM and one book on Engineering Fluid Mechanics. He has also contributed a chapter on thermal management in the book *"Fundamentals of Microsystems Packaging"* edited by Rao Tummala and published by McGraw-Hill in 2001. He has carried out many national and international collaborative projects. He has established IMAPS Malaysia Chapter in the year 1998 and IEEE-CPMT Malaysia Chapter in the year 2000 and continues to be active in this area. He is also active in offering continuing education programs to multi-national companies like Agilent, Intel, AMD etc. on the applications of Finite Element Method to electronic packaging as well as Thermal Management in Electronic Systems. Marquis book "Who is who in the world" makes a reference to Professor K. N. Seetharamu.

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