Journal of Microelectronics and Electronic Packaging (2021) **18**, 123–136

ISSN: 1551-4897

Thermal and Reliability Characterization of an Epoxy Resin-Based Double-Side Cooled Power Module

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***Abstract*—Wide-Band Gap (WBG) power devices have become a promising option for high-power applications due to the superior material properties over traditional Silicon. To not limit WBG devices' mother nature, a rugged and high-performance power device packaging solution is necessary. This study proposes a Double-Side Cooled (DSC) 1.2 kV half-bridge power module having dual epoxy resin insulated metal substrate (eIMS) for solving convectional power module challenges and providing a cost-effective solution. The thermal performance outperforms traditional Alumina (Al_2O_3) Direct Bonded Copper (DBC) DSC power module due to moderate thermal conductivity (10 W/mK) and thin (120 μm) epoxy resin composite dielectric working as the IMS insulation layer. This novel organic dielectric can withstand high voltage (5 kVAC @ 120 μm) and has a Glass Transition Temperature (Tg) of 300°C, which is suitable for high-power applications. In the thermal-mechanical modeling, the organic DSC power module can pass the thermal cycling test over 1,000 cycles by optimizing the mechanical properties of the encapsulant material. In conclusion, this article not only proposes a competitive organic-based power module but also a methodology of evaluation for thermal and mechanical performance.**

***Keywords*—: Double-side cooling, epoxy resin composite dielectric, half-bridge power module, power electronic packaging, thermal modeling, thermal-mechanical modeling**

Introduction

Fig. 1 shows the cross-sectional schematic plot of traditional power modules [1]. Semiconductor devices are soldered on one or more insulated metal-clad ceramic substrates. Insulated substrates are mounted on a thick metal baseplate for better thermal spreading and mechanical support. In addition, a plastic housing/case is attached to the metal baseplate for the silicone gel encapsulation. However, high thermal stress would occur at the solder layer between ceramic substrates and metal baseplate under thermal cyclic loads due to high CTE mismatch. Moreover, the CTE mismatch between substrates and metal baseplate can also cause warpage, resulting in a cyclic force on bond wires [2]. To solve the above reliability issues, Mitsubishi proposed a novel power module configuration using a high thermally conductive insulating metal baseplate (IMB) and epoxy resin encapsulation [1, 3, 4], as shown in Fig. 2. The IMB is similar to metal core PCB (MCPCB) or insulated metal substrate (IMS), but having a high thermally conductive epoxy resin dielectric as an insulation layer. It eliminates the solder layer between insulated substrate and baseplate, leading to lesser potential failure points. In addition, the epoxy encapsulant can mold all the components rigidly due to higher modulus compared with silicone gel and CTE matching with IMB [1-4]. On the other hand, organic packaging yields superior reliability due to CTE matching with the organic mainboard. Last but not least, the cost of organic material and manufacturing is more competitive compared with ceramic substrates [5].

The main thermal path of conventional power modules is through the baseplate side to air or coolant. For maximizing the heat dissipation capability of the module, the thermal resistance from junction to case (bottom surface baseplate) has to be minimized. Common approaches include using higher thermally conductive materials, increasing the area along the thermal path, reducing the thickness of low thermally conductive components, enlarging the contact area of interconnection components, and optimizing the thickness of conductor layers for the best heat spreading effect [6]. However, these approaches had been explored for decades and can't meet the rapidly rising demand of power density mainly due to the single-side cooling limitation. Therefore, to effectively decrease the thermal resistance, a double-side cooled (DSC) concept is proposed and realized by dissipating the heat to both the top and bottom sides of the power module. Several articles indicate a significant reduction of thermal resistance as well as electrical parasitics (e.g., resistance and inductance) [7-13]. It not only pushes the heat dissipation capability and power density to a higher level but increases system efficiency with lower parasitics.

The state-of-art DSC power modules employ top and bottom metal-clad insulated substrates for a large contact area and planar connection to dual-side solderable dice, instead of extremely small contact of conventional bond wires. Some of the DSC power modules have to have spacers for adjusting the height difference of power devices (e.g., insulated gate bipolar transistor [IGBT] and diode), improving mold flow quality of the encapsulation process, and controlling the insulation distance between terminals and cooling components (e.g., heat sink and cold plate). Cooling components can be mounted on two substrates for transporting heat from die to ambient, as shown in Fig. 3.

Due to superior thermal/electrical/mechanical performance and mature manufacturing, metal-clad ceramic substrate, e.g.,

The manuscript was received on February 1, 2021; revision received on June 2, 2021.accepted on June 19, 2021.

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doi:10.4071/imaps.1427774

direct bonded copper (DBC) is the most popular candidate for high-power modules. Preferred ceramic materials and the physical characteristics are shown in Table I [14]. The 96% Alumina (Al_2O_3) is commonly used in conventional power module substrates due to the low cost. For higher power dissipation, reliability, and electrical insulation requirements, Aluminum Nitride (AlN) is one of the best solutions. An AlN has the higher thermal conductivity among DBC ceramics and lower CTE mismatch to semiconductor devices (3–5 ppm/°C) compared with Al_2O_3. ABB Ltd proposed HiPak IGBT power modules rating from 1.7 to 6.5 kV by employing AlN-insulated substrate and Aluminum Silicon Carbide (AlSiC) baseplate for high-power applications [15].

Although many studies have focused on DSC power modules, very limited research focused on organic-based DSC power modules with evaluation of thermal and mechanical performance at the same time. This study proposes a DSC 1.2 kV SiC half-bridge power module applying a highly thermally conductive Epoxy Resin Composite Dielectric (ERCD) substrate to prove the ruggedness under thermal cycling test and demonstrates the methodology of thermal-mechanical characterization. Moreover, it shows better thermal performance and much lower cost compared with Al_2O_3 ceramic substrate. Previous works proved the feasibility and performance of one-side cooled power modules using ERCD substrates [16-18].

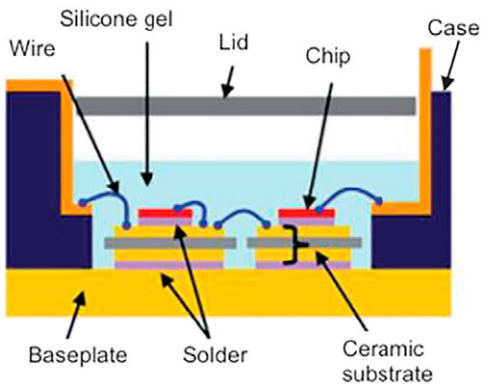

Fig. 1. A conventional power module using ceramic substrates [1].

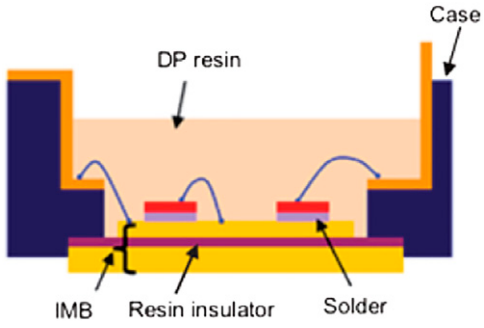

Fig. 2. A novel power module using an organic IMB and epoxy resin encapsulant [1].

A Double-Side Cooled 1.2 kV SiC BiDFET Half-Bridge Power Module Using ERCD Substrates

A. Bidirectional Field Effect Transistor (BiDFET)

The Bidirectional power switch performs identically in on and blocking states in two directions (forward and reverse). It can be used in matrix-converters or cyclo-converters and multistage inverters to facilitate high-frequency switching of AC-to-AC conversion [19]. A monolithic 1.2 kV/10A SiC BiDirectional Field Effect Transistor (BiDFET) with a dimension around 1×1 cm is proposed which contains two 4H-SiC power JBSFETs with a shared bottom drain. It can functionally work by four I/O pinouts (i.e., G1, T1, G2, and T2) on the top surface of the device as shown in Fig. 4 [20]. This article presents a BiDFET half-bridge power module by connecting the T2 of the first BiDFET to the T1 of the other one.

B. Epoxy Resin Composite Dielectric (ERCD)

The ERCD material proposed in this study is a mixture of epoxy resin, Al_2O_3, and AlN fillers developed by Risho Kogyo Co., Ltd (See Fig. 5). The epoxy resin is a low thermally conductive material. Adding the ceramic fillers greatly increases

Table I
Material Properties of Common Ceramic Materials for DBC [14]

Material	Thermal conductivity (W/mK)	CTE (ppm/°C)	Dielectric strength (kV/mm)
Al_2O_3	26-35	6.8-9	10-20
AlN	150-180	4.3-6.2	14-17
BN	20-60	0.1-6	40-200
Si_3N_4	20-30	2.6-3.6	10-14

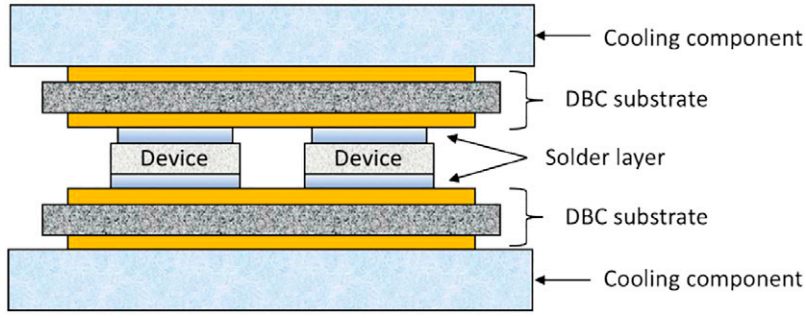

Fig. 3. The cross-sectional schematic of a DSC power module using dual DBC substrates.

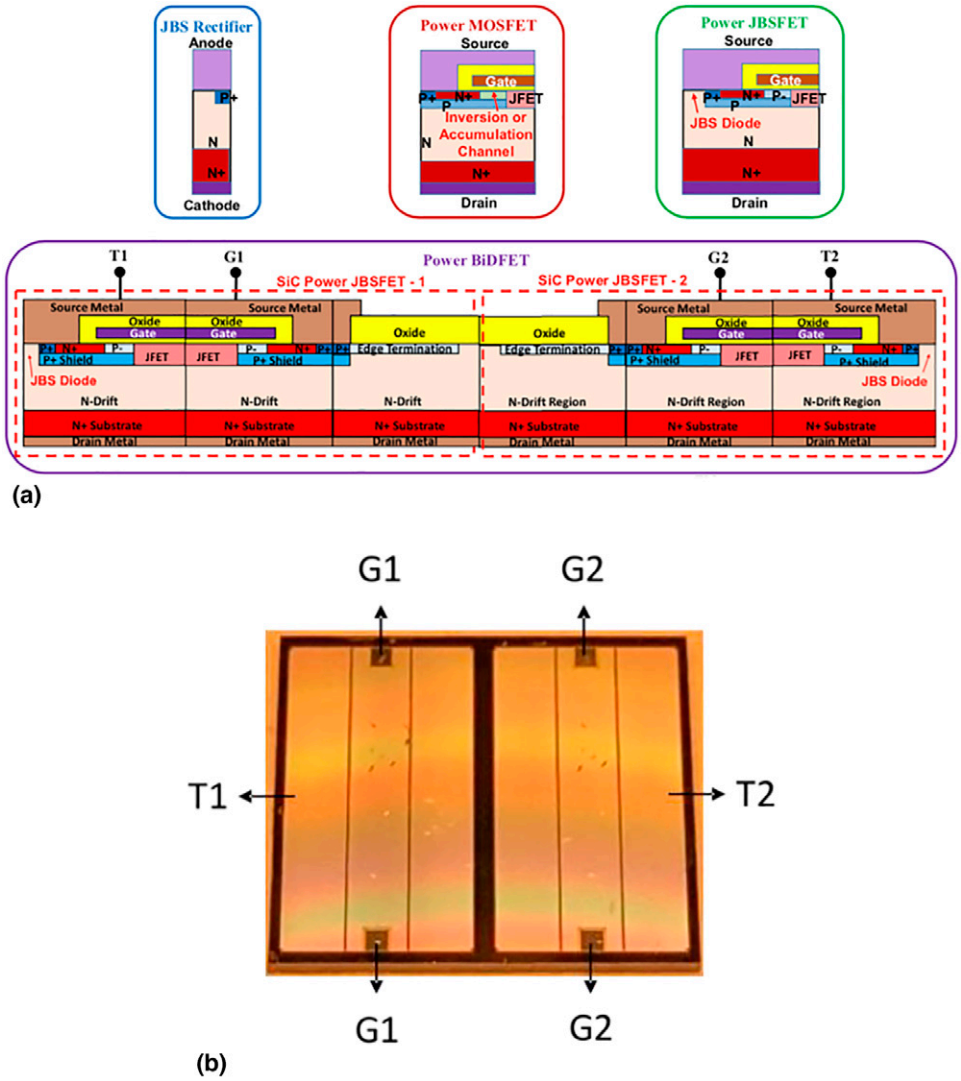

Fig. 4. A monolithic bidirectional field effect transistor: (a) schematic plot of the cross-sectional view, and (b) top view of the prototype [20].

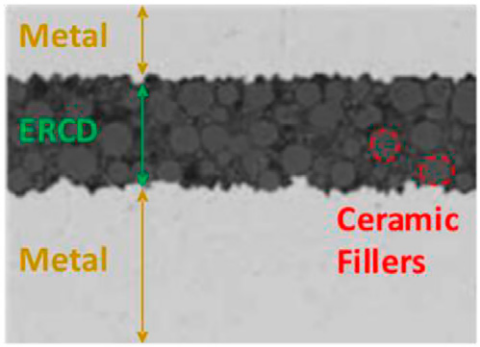

Fig. 5. The SEM image of a metal-clad ERCD substrate.

the equivalent thermal conductivity. Fig. 6 indicates the breakdown voltage (BV) test setup that is in accordance with IEC 60243-1 standard [21]. The test specimen is an IMS having 1oz top Cu layer, 120 μm ERCD, and 1 mm Al baseplate. The test results show an average BV of 5.1 kV with a standard deviation of 0.34 kV among 50 specimens, as shown in Fig. 7. For the long-term reliability testing, the ERCD substrate also shows good performance under the thermal aging test (175°C/3,000 h) and thermal cycling test (−40 to 125°C range with 30 mins dwell time for 3,000 cycles), as shown in Fig. 8.

In terms of the thermal characteristics, the Glass Transition Temperature (Tg) and thermal conductivity are 300°C and 10 W/mK, respectively. Since the standard single-layer thickness of ERCD is 120 μm, the thermal conductance of ERCD is similar to 15-mil 96% Al_2O_3 DBC. A more detailed comparison will be discussed in the next part. Its properties are shown in Table II showing excellent thermal/mechanical/electrical characteristics for wide-band gap (WBG) device packaging.

C. Physical Structure

In Fig. 9, two 10.5 × 11 × 0.36 mm SiC BiDFET devices are mounted on the bottom ERCD substrate. Spacers are mounted between the top ERCD substrate and the top surface of the

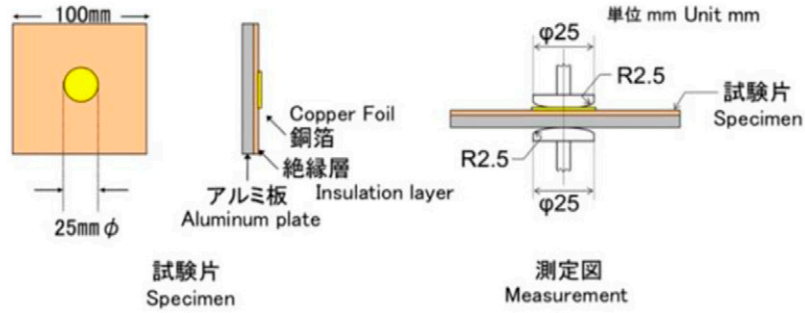

Fig. 6. Breakdown voltage test setup and test specimen.

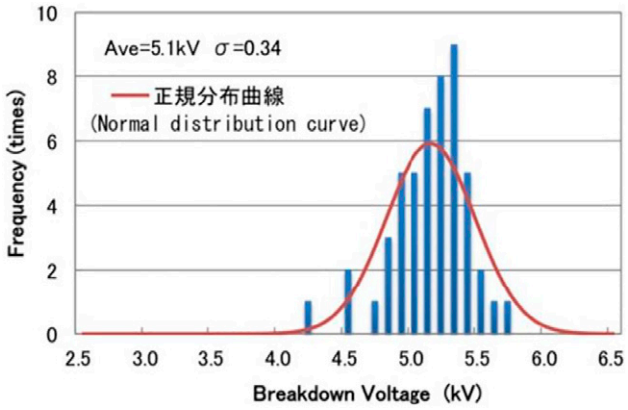

Fig. 7. Breakdown voltage distribution among 50 specimens

devices for enabling thermal and electrical paths. The function of the spacer is to create room for wire bonding on the gate pads and insulation distance between pin terminals and cooling components. The power and signal terminals are located at two opposite sides for lower crosstalk noise and easier next level packaging design. The size of the power module is 37 × 31.5 × 3.05 mm, not including terminals. Table III shows the thickness of each layer. The schematic fabrication process flowchart is shown in Fig. 10.

3-D Finite Element Modeling and Thermal Modeling Validation

A. Steady-State Thermal Modeling

To quantify the capability of power modules to dissipate the heat from die to outside, thermal resistance junction-to-case (R_{jc}) is extracted and it can be expressed as

$$R_{jc} = \frac{T_{j,max} - T_c}{P} \quad (1)$$

where the $T_{j,max}$ is the maximum junction temperature of the semiconductor device and T_c is the case temperature at the exposed thermal pad of the insulated substrate. The P is the power loss passing through the thermal path. Since there are two thermal paths in the DSC power module, both top and bottom R_{jc} will be characterized separately. Take top R_{jc} ($R_{jc,top}$) for instance, in the simulation, the exposed thermal pad of the top

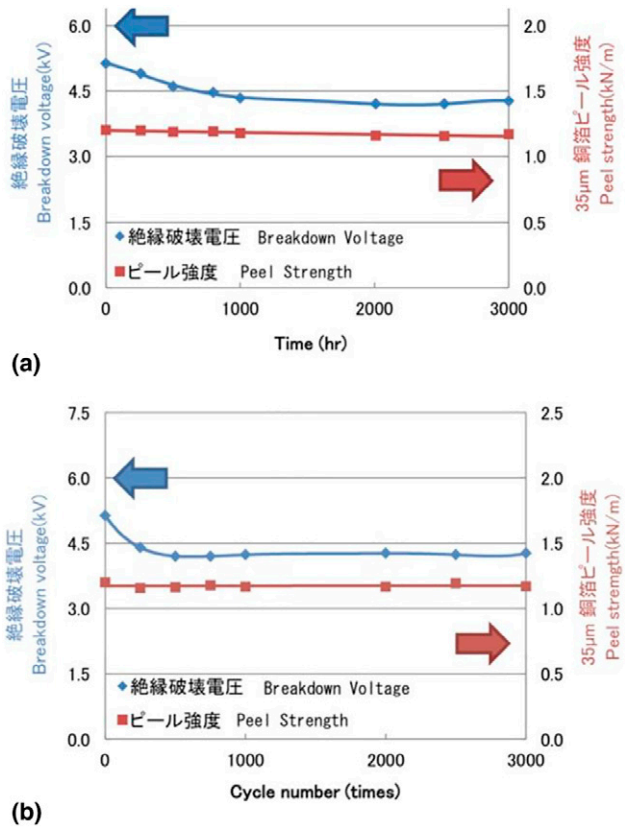

Fig. 8. Performance under long-term reliability tests: (a) thermal aging, and (b) thermal cycling.

Table II
Material Properties of the ERCD Material

Parameter	Unit	Value
Tg	°C	300
Thermal conductivity	W/mK	10
Young's modulus	GPa	53
CTE (α_1)	ppm/°C	15
Breakdown voltage	kVAC	5 @ 120 μm
Volume resistivity	Ω-m	1×10^{13}
Dk	–	6.8
Df	–	0.009

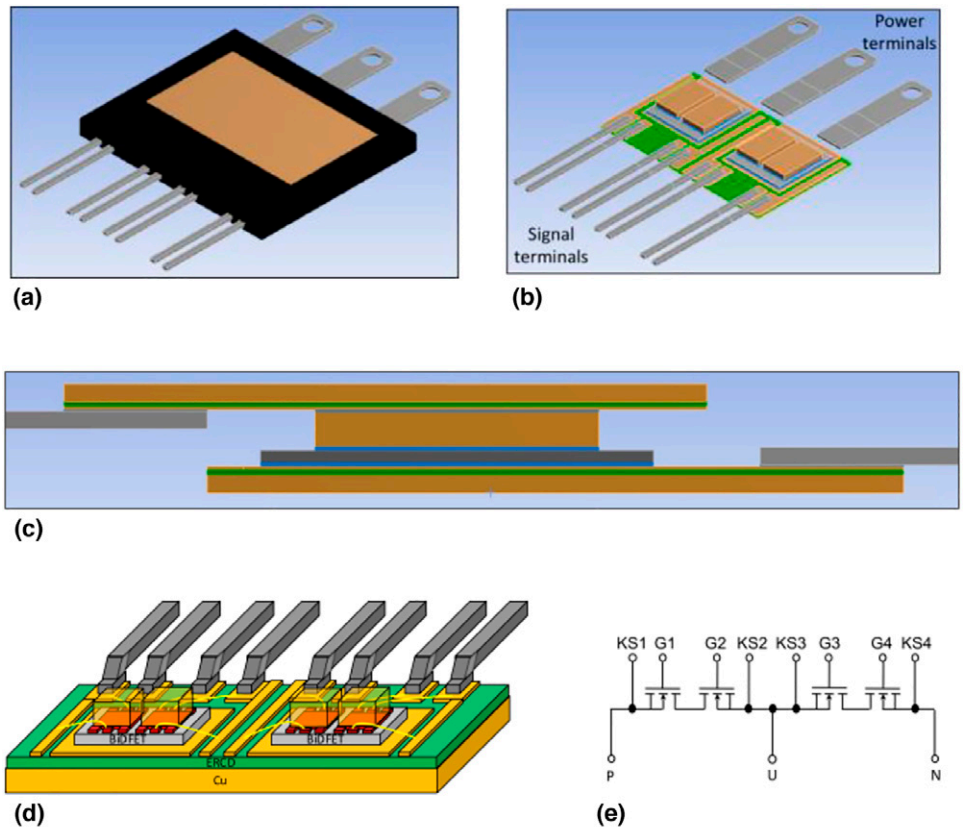

Fig. 9. 3-D models and schematics of the DSC power module: (a) 3-D model with encasement, (b) 3-D model without encasement, (c) cross-sectional view, (d) 3-D schematic, and (e) electrical circuit diagram.

Table III
Dimension of the DSC Power Module

Component	Thickness (mm)
4H-SiC Die	0.36
Cu spacer	1
ERCD substrate	Cu:3oz/ERCD:120 μm/ Cu baseplate:0.5 mm
Sn89/Sb10.5/Cu0.5 die attachment	0.1
SAC305 solder layer	0.1
Epoxy encapsulant	3.05

substrate was set to be 25°C uniformly and a known heat flow was applied on the top surface of the device. Thus, all the heat would only flow from the junction to the top case and the thermal resistance can be calculated by Eq. 1. Same method for characterizing the bottom R_{jc} ($R_{jc,\text{bottom}}$). In Fig. 11, the red dash line depicts the heat flow directions for top and bottom thermal paths. It is worth pointing out that the 25°C setting at the case is equivalent to an infinite convective heat transfer coefficient (h) applied at the case together with an ambient temperature (T_c) of 25°C. It considers the worst case when calculating the R_{jc} since the infinite h would result in a smallest spreading angle, leading to a smallest effective area along the heat path. Besides, there is no temperature gradient between case to ambient. It represents that the cooling component on the case is ideal and provide zero thermal resistance. To understand the maximum power dissipation capability of the DSC power module, an equivalent R_{jc} ($R_{jc,eq}$) is proposed and is expressed by

$$R_{jc,eq} = \frac{R_{jc,\text{top}} \times R_{jc,\text{bottom}}}{R_{jc,\text{top}} + R_{jc,\text{bottom}}} \tag{2}$$

It is crucial that the definition of $R_{jc,eq}$ is based on having both top and bottom case temperatures identical (e.g., 25°C). Hence, the $R_{jc,eq}$ can be calculated by parallel connection of $R_{jc,\text{top}}$ and $R_{jc,\text{bottom}}$. Moreover, the maximum power dissipation ($P_{d,max}$) can be further defined as

$$P_{d,max} = \frac{T_{j,\text{max allowed}} - T_c}{R_{jc,eq}} \tag{3}$$

where the $T_{j,\text{max allowed}}$ is the maximum allowed junction temperature of the semiconductor device. Typically, the values of $T_{j,\text{max allowed}}$ for Si and WBG (e.g., SiC and GaN) devices are 150°C and 175°C, respectively. T_c is 25°C for both top and bottom cases.

Due to the symmetrical structure, only half of the model was considered in the Finite Element (FE) modeling, as shown in Fig. 12. Considering interfacial thermal resistance between solder and its adjacent layer is critical in the thermal modeling. Research indicates that the interfacial thermal resistance of solder or die attachment strongly affects the power dissipation capability of electronic packages [22-24]. The interfacial thermal resistance can be

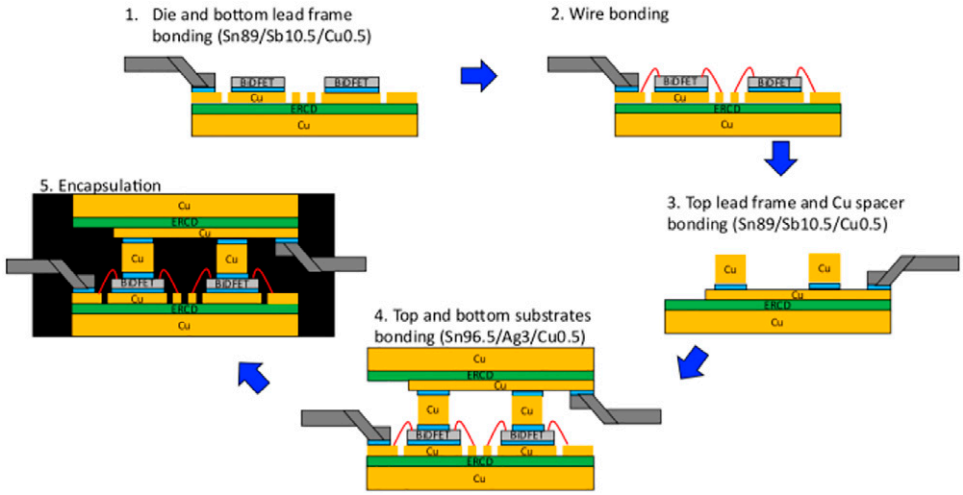

Fig. 10. Fabrication process of the DSC power module.

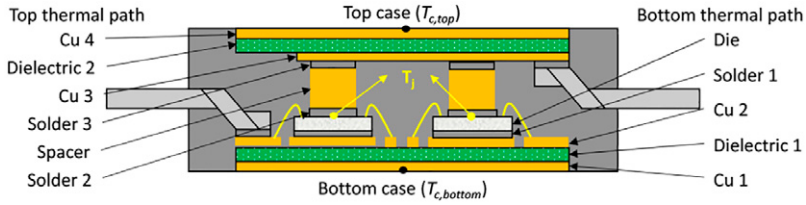

Fig. 11. The schematic plot of heat flow paths.

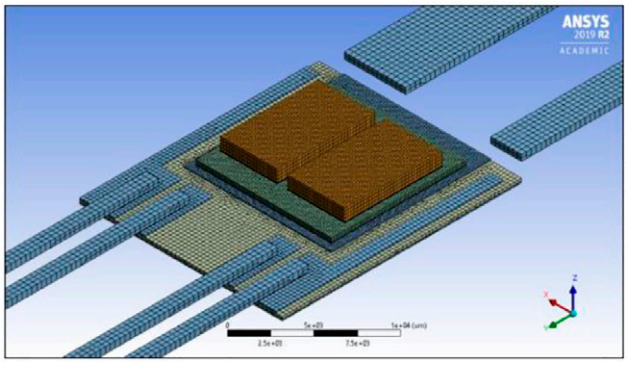

Fig. 12. Mesh arrangement of the half symmetry model.

extracted by transfer line method (TLM) and the *y*-intercepts represent the interfacial thermal resistance, as shown in Fig. 13. It's also worth pointing out that the interfacial thermal resistance can be several times of the bulk thermal resistance of the solder itself depending on the bond line thickness (BLT) and bulk thermal conductivity. Silver sintering materials are one of the solutions for minimizing interfacial thermal resistance due to excellent bonding quality between silver sintering die attachment and bonding pad with silver surface treatment. To simulate the thermal behavior accurately, the interfacial behavior can't be neglected and must be considered in the FE modeling. This study considered the interfacial thermal resistance at all the solder layer interfaces.

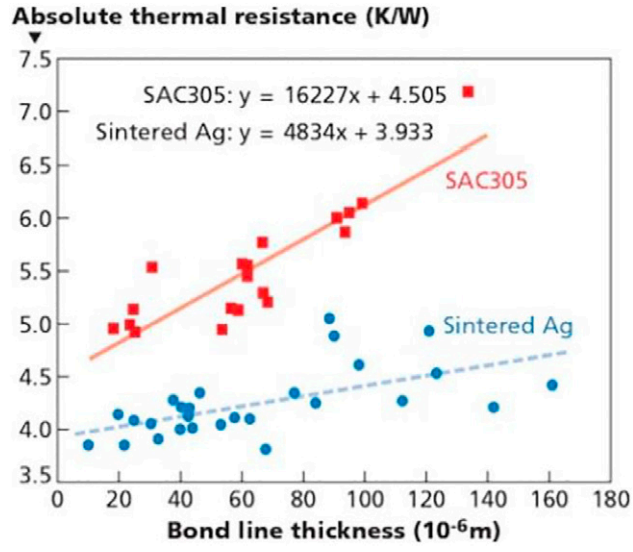

Fig. 13. Thermal resistance versus bond line thickness of die attachment materials [22].

B. *Thermal Performance Comparison of DSC Power Modules Using DBC and ERCD Substrates*

This study compared the thermal performance of DSC power modules using dual Cu-clad ERCD and Cu-clad ceramic (i.e.,

Table IV
Thermal Conductivity Parameters Used in the FE Modeling of DSC Power Module

Component	Material	Thermal conductivity (W/mK)
Pin terminal	Copper	390
Spacer		
Conductor layer		
Encapsulant	Epoxy molding compound	1
Solder 1 and 3	Sn89/Sb10.5/Cu0.5	60
Solder 2	Sn96.5/Ag3/Cu0.5	60
Die	4H-SiC	370
Dielectric layer	ERCD	10
	Al_2O_3	24
	AlN	170

Table V
Characteristics and Dimensions of Cu-clad Insulated Substrates for DSC Power Modules

Parameter	Al_2O_3 DBC	AlN DBC	ERCD IMS
Dielectric thickness (mm)	0.38	0.38	0.12
Cu thickness (mm)	Top: 0.127	Top: 0.127	Top: 0.1
	Bottom: 0.127	Bottom: 0.127	Bottom: 0.5
Breakdown voltage (kV)	5.7	5.9	5.1

Al_2O_3 and AlN) insulated substrates. The thermal property of each component in the module is shown in Table IV. To make a fair and practical comparison, 15-mil (0.38 mm) of Al_2O_3 and AlN DBCs were selected due to standard commercial thickness options and similar BV (based on the dielectric strength in Table I) to 120-μm ERCD IMS. Detailed characteristics and dimensions are shown in Table V.

To understand the most critical layers for R_{jc}, the breakdown chart by extracting the thermal resistance of each layer is provided in Fig. 14. Due to the low thermally conductive dielectric layer in ERCD and Al_2O_3 cases, as well as high interfacial thermal resistance, the "Solder 1" and "Dielectric 1" layers contribute around 90% of the $R_{jc,\text{bottom}}$, as shown in Fig. 14a. Thus, the power module designers should pay more attention to these two layers while thinking of improving the thermal conductance. Same concept for the top thermal path. In Fig. 14, it can be found that all the $R_{jc,\text{top}}$ is roughly twice the $R_{jc,\text{bottom}}$. Since the spacers only cover 60% of the die area and there is one more solder layer in the top thermal path, resulting in higher $R_{jc,\text{top}}$. Therefore, eliminating solder layers is one of the future trends, not only due to reducing thermal resistance, but also the failure probability and complexity of the manufacturing process. Fig. 15a indicates that the $R_{jc,eq}$ of ERCD case is 10% lower than Al_2O_3 one, leading to 9% higher on max. power dissipation ($P_{d,max}$) capability. It's because the Al_2O_3 is 3× thicker than ERCD, but the thermal conductivity is only 2.4× of the ERCD. In addition, though the $P_{d,max}$ of the AlN case is 68%

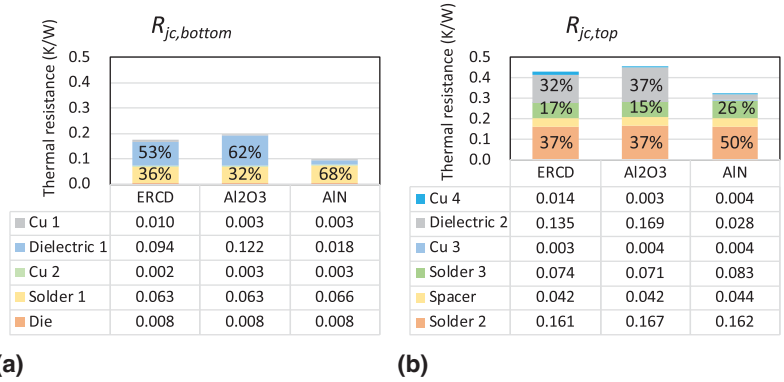

Fig. 14. Thermal resistance breakdown: (a) $R_{jc,bottom}$, and (b) $R_{jc,top}$.

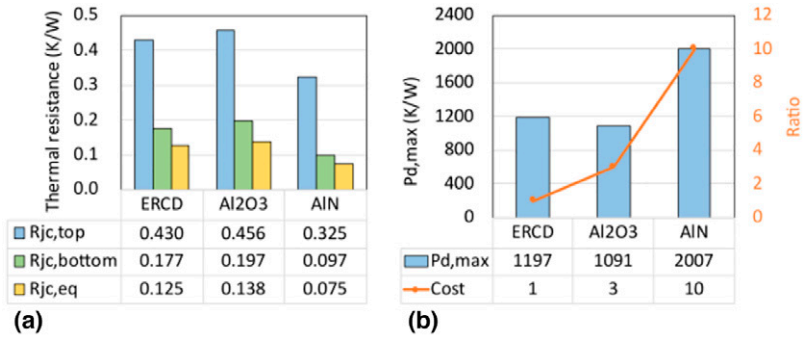

Fig. 15. Thermal characteristics and cost comparison: (a) thermal resistance, and (b) max. power dissipation and cost.

higher than the ERCD case, the cost is roughly 10 times higher than the ERCD substrate (see Fig. 15(b)).

C. *Validation of Thermal Modeling*

To validate the thermal modeling, a thermal dissipation test was carried. In the experiment, the module was self-heated by inputting a known DC current and the case temperature was captured by thermocouple (TC). Due to the unavailability of the dual-side solderable die and ERCD IMS with Cu baseplate, this study proposed a single-side cooled BiDFET half-bridge power module using wire bond version die and IMS with 1.5 mm-thick Al baseplate for validation, as shown in Fig. 16.

A fine gauge TC wire (36-40 gauge) and high thermally conductive attachment material (>5 W/mK) was used for minimizing the TC reading error [25, 26]. Thus, two 38-gauge (0.1 mm) K-type TCs were selected and mounted on the top case of the module by a small amount of 15.7 W/mK thermal paste. A 12V DC fan was mounted on the top of the top-side cooled module for cooling. Fig. 17 demonstrates the test setup and all the equipment.

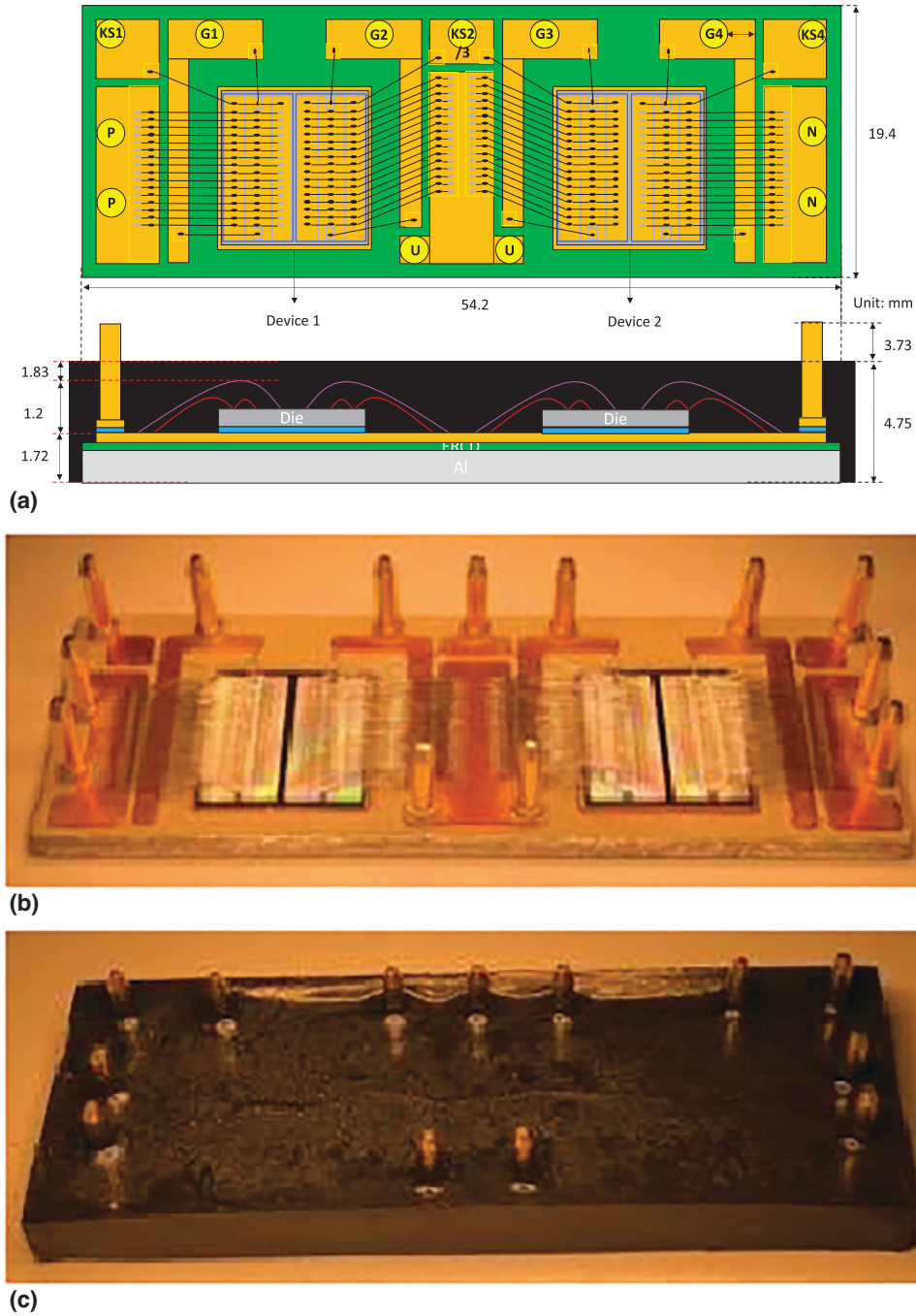

Fig. 16. Single-side cooled BiDFET half-bridge power module: (a) schematic plot, (b) unencapsulated module, and (c) encapsulated module.

Although difficult to physically measure the junction temperature (T_j), JESD51-1 proposed an electrical test method (ETM) for measuring the thermal characteristics of packaged semiconductor devices by using a temperature-sensitive parameter (TSP) [27]. The forward voltage drop (V_f) of a diode is one of the most common TSPs. The diode can be specifically designed into the die or it exists as a parasitic device (e.g., body diode of MOSFET). The concept is to capture the relationship of TSP versus temperature for correlating junction temperature. However, to measure the V_f of the MOSFET, the heating current (I_h) has to be turned off and then the V_f measurement needs to start within a few microseconds for preventing temperature drop. This requires high-speed sampling digital multimeters and fast high-compliance pulsed current sources for ensuring accurate measurement. Therefore, for a simpler and reliable measurement, this study adopts the on-state resistance (R_{on}) as TSP since the R_{on} can be measured without turning off the I_h and high-speed equipment. The R_{on} is defined as the terminal-to-terminal resistance between P and U pins (see Fig. 16(a)) and the relationship of R_{on} versus temperature is shown in Fig. 18.

In the thermal dissipation experiment, a known heating current was inputted into device 1 (left) and the voltage drop was in-situ monitored. The case temperatures and the voltage drop were recorded once those values were stable and the system reached thermal equilibrium. The R_{on} and generated power can be calculated by Ohm's law and Joule heating, respectively. In the simulation, the convection heat transfer coefficient (h) was obtained as 270 W/m^{2}K by aligning to the experimental T_j. The differences of T_c between experiment and simulation are only −3.1% and 1.8% for $T_{c,1}$ and $T_{c,2}$, respectively. The temperature distribution with an input current of 20A and Joule heat of 17.92W is shown in Fig. 19. Fig. 20 shows good agreement between experiment and simulation and validates the steady-state thermal modeling.

D. Thermal-Mechanical Modeling

This section discusses the mechanical reliability of the DSC power modules using different insulated substrates subjected to the thermal cycling test in accordance with JESD22-A104D condition M that the testing temperature range is −40 to 150°C and the dwell time is 10 min [28]. The common failure modes of power modules under active and passive thermal cycling load were well organized, such as wire degradation, solder fatigue, and die crack [29, 30]. In terms of the DSC power module with spacer interconnection, it was found that the failure mode occurred at the solder layer between the spacer and die due to a high CTE mismatch between silicon and metal [31]. In this study, several potential failure points were monitored, and the criteria are defined as (1) max. principal stress of SiC die <250 MPa, (2) max. principal stress <50 and 300 MPa for ERCD and ceramic dielectric (i.e., Al_2O_3 and AlN, respectively), (3) SAC305 fatigue life >1,000 cycles.

Coffin–Manson empirical equation [32] is widely used for evaluating the solder joint fatigue life under thermal cycling test in the electronic packaging field. Many researchers have modified the equation for better accuracy and made it easier to apply. For example, Lin et al. proposed a modified Coffin–Manson equation by using the range of equivalent plastic strain in one cycle to predict the solder fatigue life [33] and was applied in this study. This modified equation has been validated by some research [34, 35]. The equation can be expressed as

$$N_f = \theta\left(\Delta\varepsilon_{eq}^{pl}\right)^{\eta} \tag{4}$$

where N_f is the mean cycles to failure and $\Delta\varepsilon_{eq}^{pl}$ is the range of equivalent plastic strain. The θ and η are the constants determined by solder materials. The θ and η are 0.235 and −1.75 for SAC305, respectively [35].

In the numerical modeling, Anand viscoplastic constitutive model was applied since it can consider both elastoplastic and

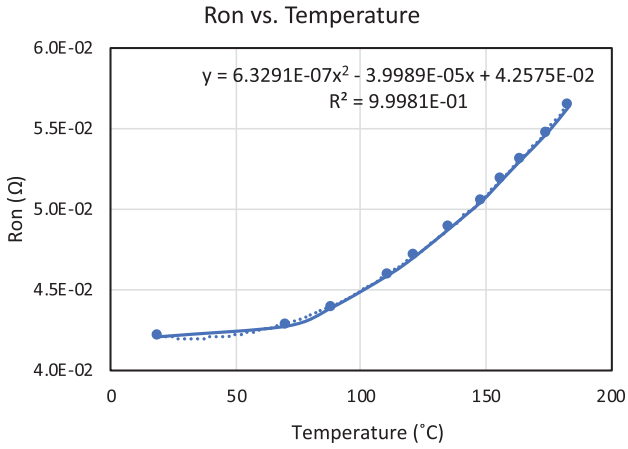

Fig. 18. Relationship of R_{on} versus temperature of Device 1.

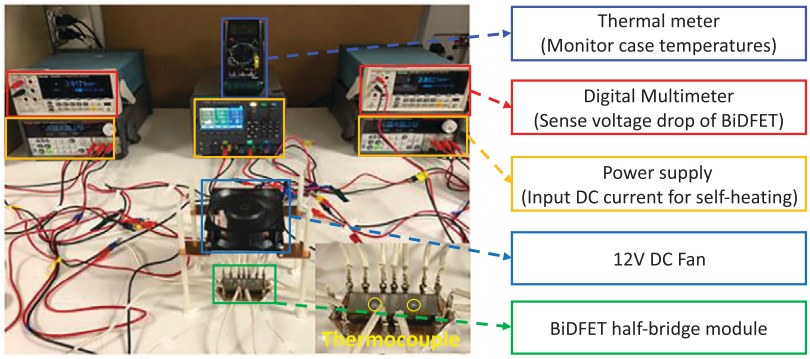

Fig. 17. Test setup of the thermal dissipation experiment.

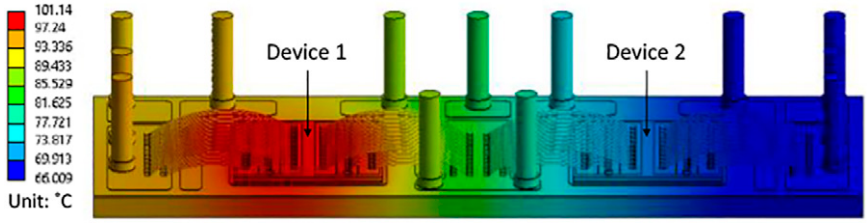

Fig. 19. Temperature distribution of the single-side cooled power module with an input current of 20A.

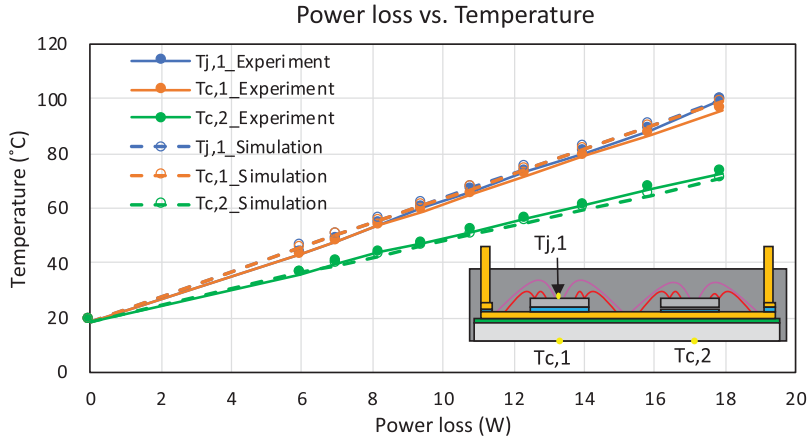

Fig. 20. Relationship of power loss versus temperature of the single-side cooled power module.

creep behaviors for SAC305 during the cyclic thermal load. The flow equation was described as [36]

$$\dot{\varepsilon}_p = A \exp\left(-\frac{Q}{RT}\right)\left[sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \quad (5)$$

where $\dot{\varepsilon}_p$ is the plastic strain rate, T is the absolute temperature, and s is the internal variable.

The evolution equation was described as

$$\dot{s} = \left\{h_0 |\ (B)\ |^a \frac{B}{|\ B\ |}\right\}\dot{\varepsilon}_p \quad (6)$$

where

$$s^* = s\left[\frac{\dot{\varepsilon}_p}{A} exp\left(\frac{Q}{RT}\right)\right]^n \quad (7)$$

and,

$$B = 1 - \frac{s}{s^*} \quad (8)$$

All the material parameters of the Anand model for SAC305 and mechanical properties are shown in Table VI and Table VII, respectively.

It is critical to select the encapsulant material with optimal mechanical properties for maximizing reliability. Thus, this study sets the ranges of modulus and CTE of commonly seen commercial epoxy encapsulants for 25 cases of Design of Experiment (DoE), as shown in Table VII. Due to the higher CTE mismatch between die and organic substrate compared with the ceramic substrate, the encapsulant is more important for organic power modules to balance CTEs and manage reliability. The traditional silicone gel that primary function is to provide electrical insulation is no longer capable of stress management due to low modulus or weak mechanical support.

Table VI
The Parameters of Anand Model for SAC305 [37]

Description	Symbol	Value
Initial value of deformation resistance	*s0*	45.9 MPa
Activation energy	*Q/R*	7460 K^{-1}
Pre-exponential factor	*A*	5.87×10^6 s^{-1}
Stress multiplier	ξ	2
Strain rate sensitivity of stress	*m*	0.00942
Hardening/softening constant	*h0*	9350 MPa
Coefficient for saturatio*N* value of deformation resistance	$\hat{s}$	58.3 MPa
Strain rate sensitivity of the saturatio *N* value	*n*	0.015
Strain rate sensitivity of the hardening/softening	*a*	1.5

The mechanical behaviors in the DSC power module can be attributed to two mechanisms, including (1) local CTE mismatch between adjacent materials, and (2) global CTE mismatch between spacer and encapsulant. The first mechanism can occur at any two bonded materials with different CTEs, and a higher modulus would exaggerate the thermal stress. The global CTE mismatch can result in tensile or compressive stress on dice based on the polarity of the CTE mismatch between spacer and

Table VII
The Mechanical Properties in FE Modeling

Component	Material	Young's modulus (GPa)	Poisson ratio	CTE (ppm/°C)
Lead frame Spacer Conductor layer	Copper	110	0.35	17.6
Encapsulant	Epoxy molding compound	10-30	0.3	10-30
Solder 1	Sn95Sb5	50	0.38	22.8
Solder 2	SAC305	45.7 @ −40°C 42.2 @ −20°C 31.7 @ 40°C 24.6 @ 80°C 16.7 @ 125°C 12.3 @ 150°C	0.35	21
Die	4H-SiC	347	0.23	4.5
Dielectric	ERCD	53	0.22	15
	Al_2O_3	340	0.22	6.8
	AlN	320	0.23	4.7

encapsulant. It can bring opposite mechanical behaviors when the CTE of the encapsulant is higher or lower than Cu spacer. In addition, the fatigue life of solder and the stress of the top and bottom insulated substrates would also be affected by the extent of global CTE mismatch.

In addition to CTE, Young's modulus is another key factor for reliability. A higher modulus can mitigate the deformation as a result higher stiffness. However, it can also yield higher stress directly at adjacent materials due to local CTE mismatch. Since the mechanical interaction can be very complicated, this study parameterizes CTE and modulus of encapsulant for a sophisticated evaluation of the reliability.

The most commonly seen failure points in power modules are monitored and the criteria are defined. The failure theory can be categorized into two types: brittle failure and ductile failure. The brittle failure usually occurs when the max. normal stress in any direction reaches the max. tensile or compressive strength of the material. Thus, the principal stress, which is corresponding to the max. normal stress at a certain angle, is a proper failure indicator for brittle materials (e.g., SiC, ceramics, and ERCD). Due to the ductile or malleable feature, the ductile materials usually fail in a certain cyclic force or load in electronic packaging, leading to fatigue failure. For assessing solder fatigue lifetime, there are many empirical theories been developed, including stress-based, strain energy-based, and strain-based prediction models. This study adopted an equivalent plastic strain-based model for evaluating SAC305 solder fatigue life subjected to thermal cycling test.

Aforementioned, there is a huge CTE mismatch between die and ERCD IMS, resulting in a higher max. principal stress of die of the ERCD type compared with ceramic substrate configuration, as shown in Fig. 21. However, there is minimal die stress when the encapsulant has a CTE of 15 ppm/°C and modulus of 30 GPa. This indicates that the global CTE mismatch mechanism dominates the die stress in the ERCD type and the encapsulant material has to be carefully optimized. The lower CTE mismatch to Cu spacer (CTE = 17.6 ppm/°C) and the harder encapsulant, the better improvement on the die reliability. On the other hand, it

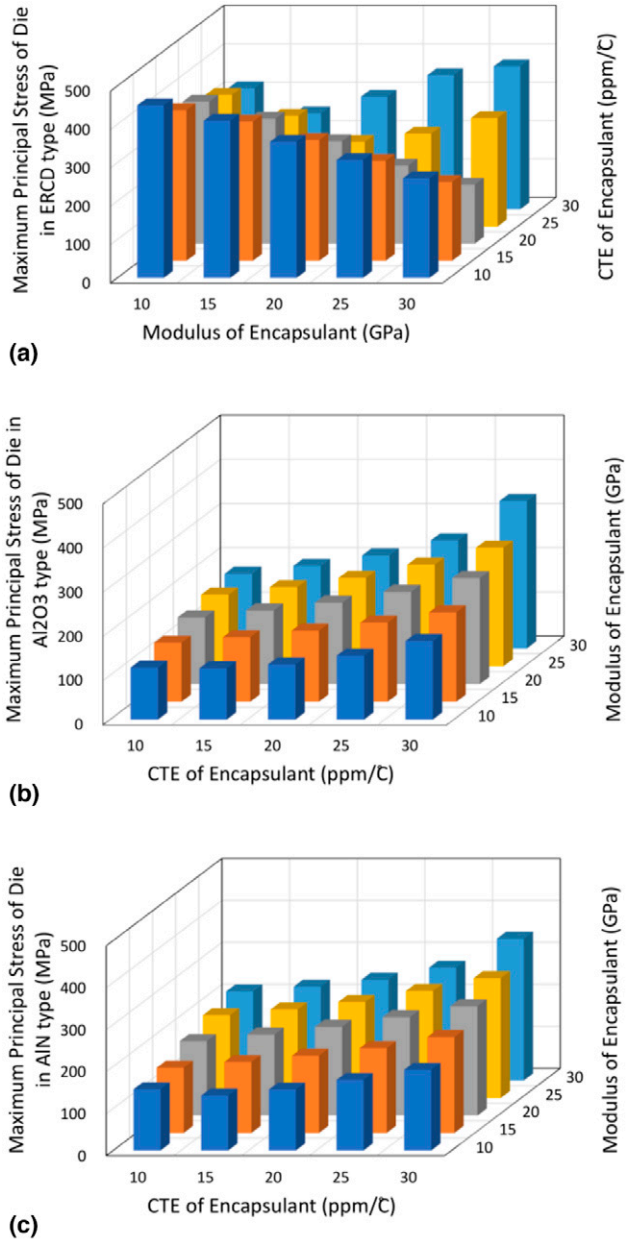

Fig. 21. Max. principal stress of SiC die: (a) ERCD type, (b) Al_2O_3 type, and (c) AlN type.

shows that the local CTE mismatch dominates the die stress in ceramic types. Higher CTE and modulus of encapsulant would only deteriorate the reliability of SiC die. Therefore, the design experience of ceramic-based DSC power modules cannot be applied to organic-based approaches.

In terms of the stress on the dielectric layer of the metal-clad insulated substrates (e.g., Al_2O_3 or AlN in DBC, and ERCD in IMS), it can be found that the optimal points are located in the range of 15–20 ppm/°C of encapsulant, as shown in Fig. 22. With similar CTEs, the Cu spacer and encapsulant would expand or contract evenly in the vertical direction, leading to small warpage on both top and bottom substrates. This is exactly the global effect. However, the local effect still affects the AlN type since

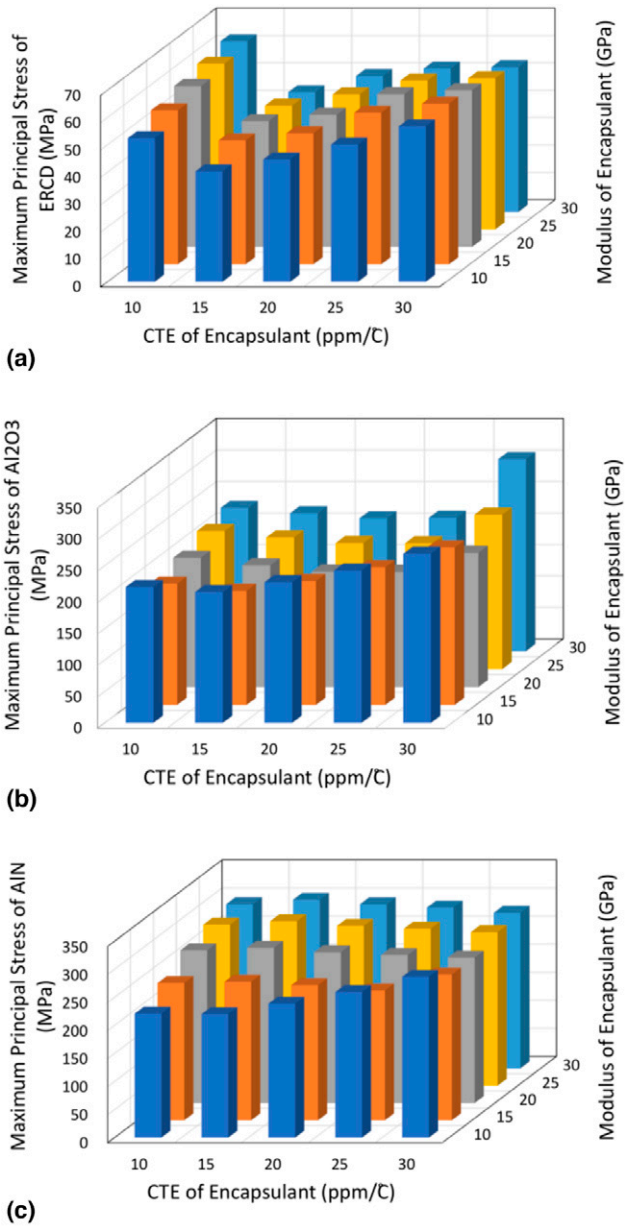

Fig. 22. Max. principal stress of dielectric substrate layer: (a) ERCD type, (b) Al_2O_3 type, and (c) AlN type.

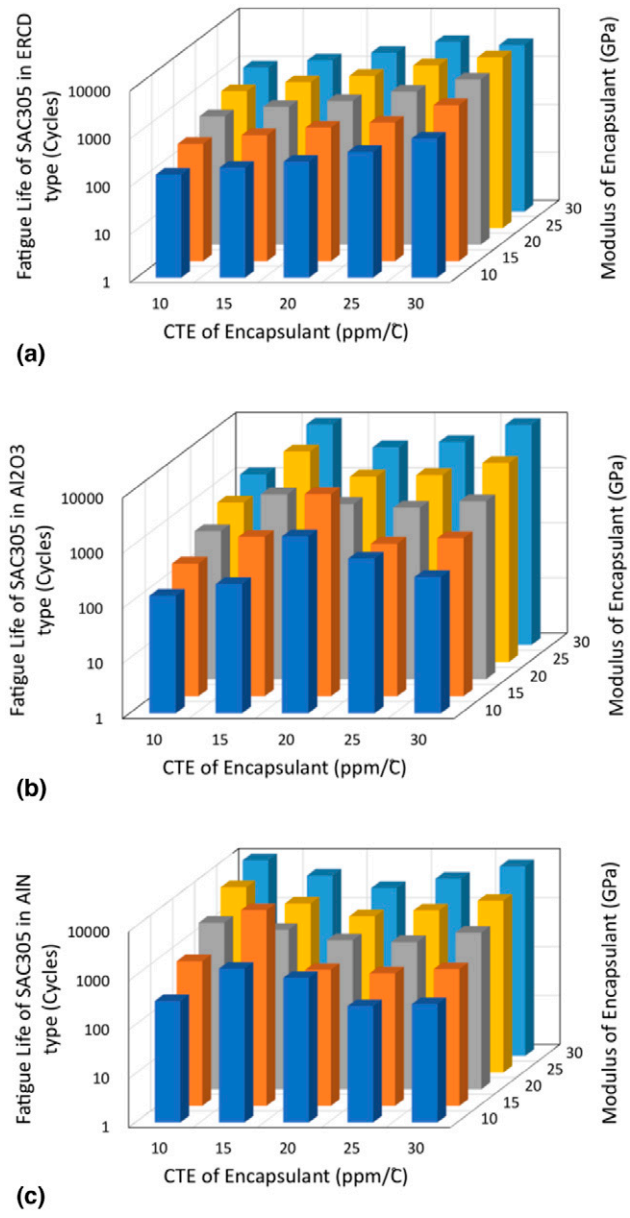

Fig. 23. Fatigue life of SAC305: (a) ERCD type, (b) Al_2O_3 type, and (c) AlN type.

the minimal stress occurs at the bar with a CTE of 10 ppm/°C and modulus of 10 GPa.

The SAC305 is located between the die and the bottom substrate (see "solder 2" in Fig. 11). It is subjected to a large CTE mismatch between those parts. Thus, in Fig. 23, it can be observed that higher CTE of encapsulant can increase the equivalent CTE surrounding the die for minimizing the CTE mismatch or maximizing the solder lifetime. In addition, the higher modulus can magnify this effect. It is worth noting that the global effect still has an influence on ceramic types. Some peaks occur at the range of 15-20 ppm/°C of encapsulant due to low CTE mismatch to Cu spacer.

Each type of power module contains 25 cases of DoE. After the filtering process based on the criteria established, the optimal properties of encapsulant and its corresponding stresses and fatigue life among the DoE are shown in Table VIII. The first step of the filtering process is to screen out the points by the criteria for die, dielectric layer, and solder. Then, for considering the minimum mechanical effect on the semiconductor device, the optimal cases are selected based on the lowest max. principal stress of die from the passed cases. Although the ERCD type has higher stress on the die, the solder fatigue life is higher than ceramic types. It can be found that the optimal mechanical properties of encapsulant for the organic and ceramic-based power modules are quite different. The encapsulant material has to be separately optimized based on the different configurations. Also, the CTE of commercial epoxy molding compounds

Table VIII
Optimal Properties of Encapsulants and the Corresponding Stresses and Fatigue Life

	ERCD	Al_2O_3	AlN
CTE of encapsulant (ppm/°C)	20	20	15
Modulus of encapsulant (GPa)	30	10	10
Max. principal stress of die (MPa)	154	125	131
Max. principal stress of dielectric layer (MPa)	41	224	220
Solder fatigue life (cycles)	2,078	1,624	1,396

(EMCs) is usually inversely proportional to its modulus since the EMC is a mixture of epoxy resin and hardener. More hardener results in higher modulus but lower CTE. Therefore, it is difficult to find a high CTE and high-modulus EMC for the ERCD-type power module. This study points out the potential demand for high CTE and high modulus encapsulants and provides insights for material scientists to explore epoxy encapsulants.

Conclusion

Thermal performance and mechanical reliability of DSC power modules are characterized by three-dimensional (3-D) FE modeling. The thermal modeling is validated through a thermal dissipation test on a single-side cooled power module that uses an ERCD. The DSC ERCD power module shows a 10% reduction on equivalent thermal resistance junction-to-case ($R_{jc,eq}$) compared with an Al_2O_3 DBC power module. In addition, the ERCD material cost is only 1/3 of the 96% Al_2O_3 DBC. In the thermal–mechanical modeling, a methodology for evaluation of DSC power module reliability is proposed. For selecting optimized encapsulants, a set of DOE and reliability criteria are created for three types of DSC power modules. This study proposes local and global CTE mismatch mechanisms to elucidate the mechanical behaviors on die, dielectric substrate layer, and solder. The ERCD type power module passes the established criteria by applying optimized properties of the encapsulant. In summary, the organic-based insulated substrate is a replacement for Al_2O_3 DBC substrate in advanced DSC power modules.

Acknowledgments

The authors thank the Solar Energy Technologies Office (SETO) of U.S. Department of Energy (DOE) for funding this work. This work was supported by the Risho Kogyo Co., LTD. and TechDream, Inc.

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