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Chip-Last (RDL-First) Fan-Out Panel-Level Packaging (FOPLP) for Heterogeneous Integration

John H. Lau,* Cheng-Ta Ko, Chia-Yu Peng, Kai-Ming Yang, Tim Xia, Puru Bruce Lin, Jean-Jou Chen, Po-Chun Huang, Tzvy-Jang Tseng, Eagle Lin, Leo Chang, Curry Lin, and Winnie Lu

***Abstract*—In this investigation, the chip-last, redistribution-layer (RDL)–first, fan-out panel-level packaging (FOPLP) for heterogeneous integration is studied. Emphasis is placed on the materials, process, fabrication, and reliability of a heterogeneous integration of one large chip (10 × 10 mm^2) and two small chips (7 × 5 mm^2) by an FOPLP method on a 20 × 20-mm^2 RDL-first substrate fabricated on a 515 × 510 mm^2 temporary glass panel. Reliability test such as the drop test of the heterogeneous integration package on a printed circuit board (PCB) is performed, and test results including failure analysis are presented. Some recommendations are also provided.**

***Keywords*—Fan-out packaging, RDL-first, chip-last, panel-level packaging, heterogeneous integration, drop test**

Introduction

In [1], the design, materials, process, and assembly of a heterogeneous integration of multiple chips on a redistribution-layer (RDL)–first substrate with fan-out panel-level packaging (FOPLP) have been reported. The RDL-first substrate [1] is fabricated on a temporary glass carrier and consists of three RDLs with the metal layer linewidth and spacing (L/S) equal to 2/2, 5/5, and 10/10 μm. Because of the process order (2/2 μm metal L/S first, 5/5 μm second, and 10/10 μm third) in fabricating the RDL-first substrate, there is a need to transfer (bond) the RDL-first substrate to another temporary carrier. Then, the first temporary glass carrier was debonded and the chips-to-substrate bonding was performed, so that the chips can be connected directly to the 2/2-μm metal L/S RDL. However, because of the large warpage due to the bonding of the second carrier and the debonding of the first carrier, the yield of the solder mass reflow of the chips on the RDL substrate is very low. Thus, in [1] thermocompression bonding, one chip at a time, has been used.

In this study, a new process order in fabricating the RDL substrate is presented (10/10 μm metal L/S first, 5/5 μm second, and 2/2 μm third). In this case, there is no need to transfer the RDL substrate to another carrier before chips-to-RDL-substrate bonding by a small-force thermocompression first and then solder mass reflow of all the chips at once.

The reliability of the printed circuit board (PCB) assembly of the heterogeneous integration package is demonstrated by a drop test. The results and failure analysis are discussed.

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Unimicron Technology Corporation, No. 179, Shanying Road, Taoyuan City 33341, Taiwan

*Corresponding author; email: John_Lau@unimicron.com

A brief literature review of chip-last (RDL-first) FOPLP has been given in [1-3]. A brief literature review of heterogeneous integration has been given in [4] and [5]. Defense advanced research projects agency (DARPA) has been making very good progress on heterogeneous integration in more than 15 y with more than 30 first-tire companies such as Intel, Micron, Cadence, Synopsys, Lockheed Martin, Northrop Grumman, MI University, and Georgia Institute of Technology, and their key programs in heterogeneous integration are briefly mentioned.

DARPA's first effort on heterogeneous integration is the COSMOS (compound semiconductor materials on silicon) program [6] which started in May 2007. COSMOS developed three unique approaches to the heterogeneous integration of (indium phosphide) (heterojunction bipolar transistors) with deep submicron Si (complementary metal-oxide semiconductor). COSMOS is now a diverse accessible heterogeneous integration (DAHI) program [7] thrust. The DAHI program is developing the following key technical challenges: (1) heterogeneous integration process development, (2) high-yield manufacturing and foundry establishment, and (3) circuit design and architecture innovation.

DARPA started the CHIPS (common heterogeneous integration and IP (Intellectual Property) reuse strategies) program [8] in 2017. The aim of the CHIPS program is to make modular computers out of chiplets. The CHIPS program is addressing integration standards, IP blocks, and design tools. Intel is providing a royalty-free license for their advanced interface bus technology to CHIPS program participants.

Navy proposed a state-of-the-art heterogeneous integrated packaging (SHIP) program [9] in the mid-2019. The primary objective of the SHIP project will be to demonstrate a novel approach to a secure, assessable, and cost-effective state-of-the-art integrated, design, assembly, and test leveraging the expertise of commercial industry. Designs must also adhere to the interface standards developed under the DARPA CHIPS program to ensure proper insertion and testability of the final product.

In the past couple years; there are many heterogeneous integration articles. Some of those are listed in [4, 5, 10-26].

In this study, the materials, process, fabrication, and reliability of the heterogeneous integration of three chips (one large and two small) on a three-layer RDL substrate (with the minimum L/S of the metal layers (MLs) equal to 2/2 μm) fabricated on a 515 × 510-mm^2 panel are investigated. The physical meaning of this structure could be for an application processor chipset; the large chip could be the processor and the smaller chips could be the memories.

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Test Chips and Test Package

A. Test Chips

The test chips are the same as those in [1]. The dimensions of the large chip (chip 1) are 10 × 10 mm^2 and of the small chip (chip 2) are 7 × 5 mm^2 (Fig. 1. It can be seen that there are 3,760 pads on 90-μm pitch for the large chip and 1,512 pads on 60-μm pitch for the small chip. The micro bump of both chips is the same: (1) the diameter and height of the Cu pillar are, respectively, 35 μm and 37 μm, (2) the Ni barrier layer is 3 μm, and (3) the SnAg solder cap is 15 μm.

B. Test Package

The cross section view and top view of the test package is shown in Fig. 2. It can be seen that there are three chips (one large and two small) on a 20 × 20-mm^2 substrate. The substrate consists of three RDLs and the L/S of the first metal layer (ML1) of RDL1 are 2/2 μm, of the second metal layer (ML2) of RDL2 are 5/5 μm, and of the third metal layer (ML3) of RDL3 are 10/10 μm. The thickness of ML1, ML2, and ML3 are, respectively, 2.5, 2.5, and 8 μm. The thickness of the dielectric layers (DLs) DL01 (DL between the Cu pad and ML1), DL12 (DL between ML1 and ML2), and DL23 (DL between ML2 and ML3) are, respectively, 5, 6.5, and 6.5 μm as shown in Fig. 3a. The solder resist (mask) opening and thickness are, respectively, 245 μm and 5 μm.

The top side of the RDL substrate for those three chips is shown in Fig. 3b and its bottom side for the solder balls on the PCB is shown in Fig. 3c. It can be seen that there are 6,784 pads with 90-μm and 60-μm pitches on the top side and 2,780 pads with .35-mm pitch on the bottom side.

The 20 × 20 mm^2-RDL substrate is fabricated on a large temporary glass panel with dimensions of 515 × 510 mm^2 as shown in Fig. 4. It can be seen that, at one shot, 396 (20 × 20 mm^2) RDL substrates can be made. After the RDL substrate fabrication is completed, the panel is then cut into 12 strips (240 × 74 mm^2) and each strip is with 33 (20 × 20 mm^2) package substrates. All the remaining assembly and process steps are performed on the strip.

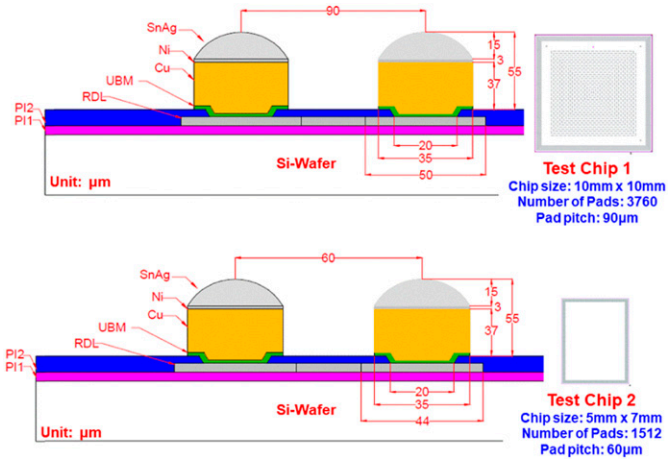

Fig. 1. Cross sections of test chips (chip 1 and chip 2).

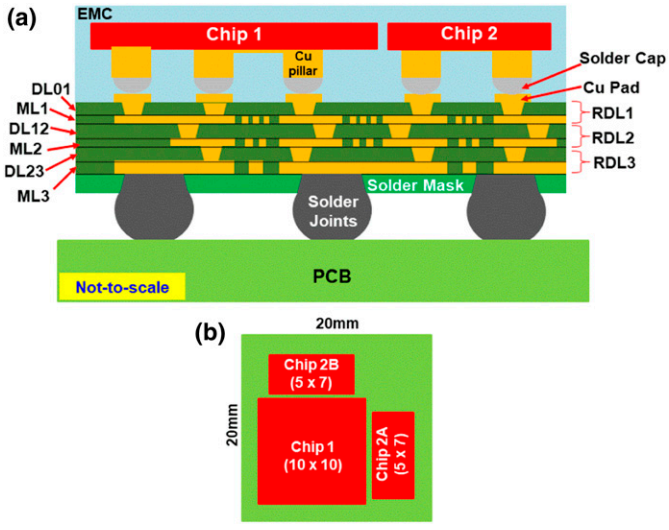

Fig. 2. (a) Cross section of heterogeneous integration test package with three RDLs. (b) Top-view of the package.

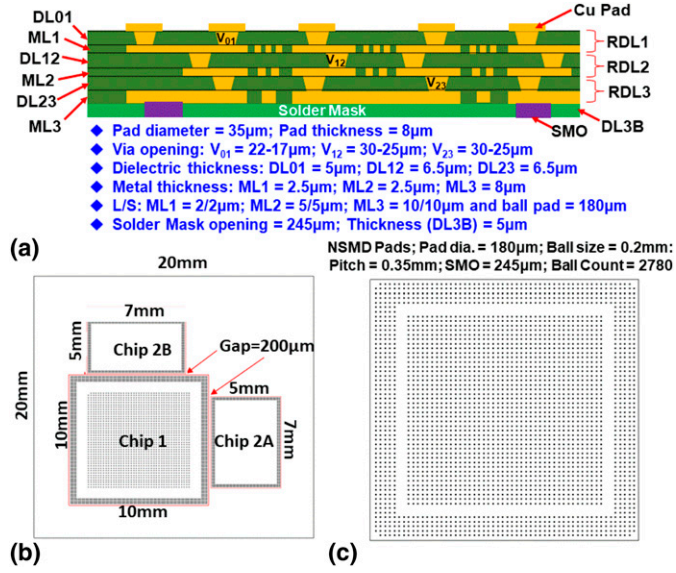

Fig. 3. (a) RDL substrate. (b) Top-view of the RDL substrate. (c) Bottom-view of the RDL substrate.

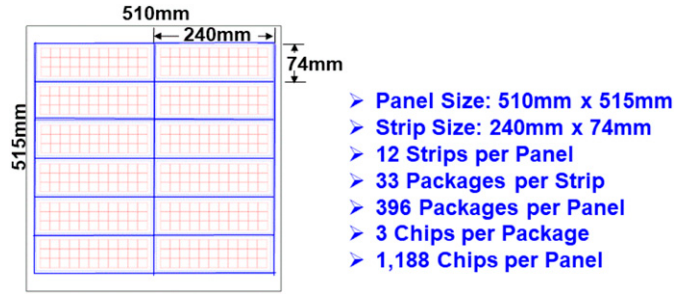

Fig. 4. Temporary glass panel for fabricating the RDL substrate.

Redistribution-Layer–First Fan-Out Panel-Level Packaging for Heterogeneous Integration

The key process flow steps for fabricating the RDL-first substrate, surface finishing, chip-to-substrate bonding, underfilling, epoxy molding compound (EMC) molding, solder resist opening (SRO) and solder ball mounting, and dicing are shown in Figs. 5a and b. Comparing with those process steps in making the RDL substrate in Figs. 6a and b of [1], it can be seen that they are very different. The key difference is that in [1], the RDLs are

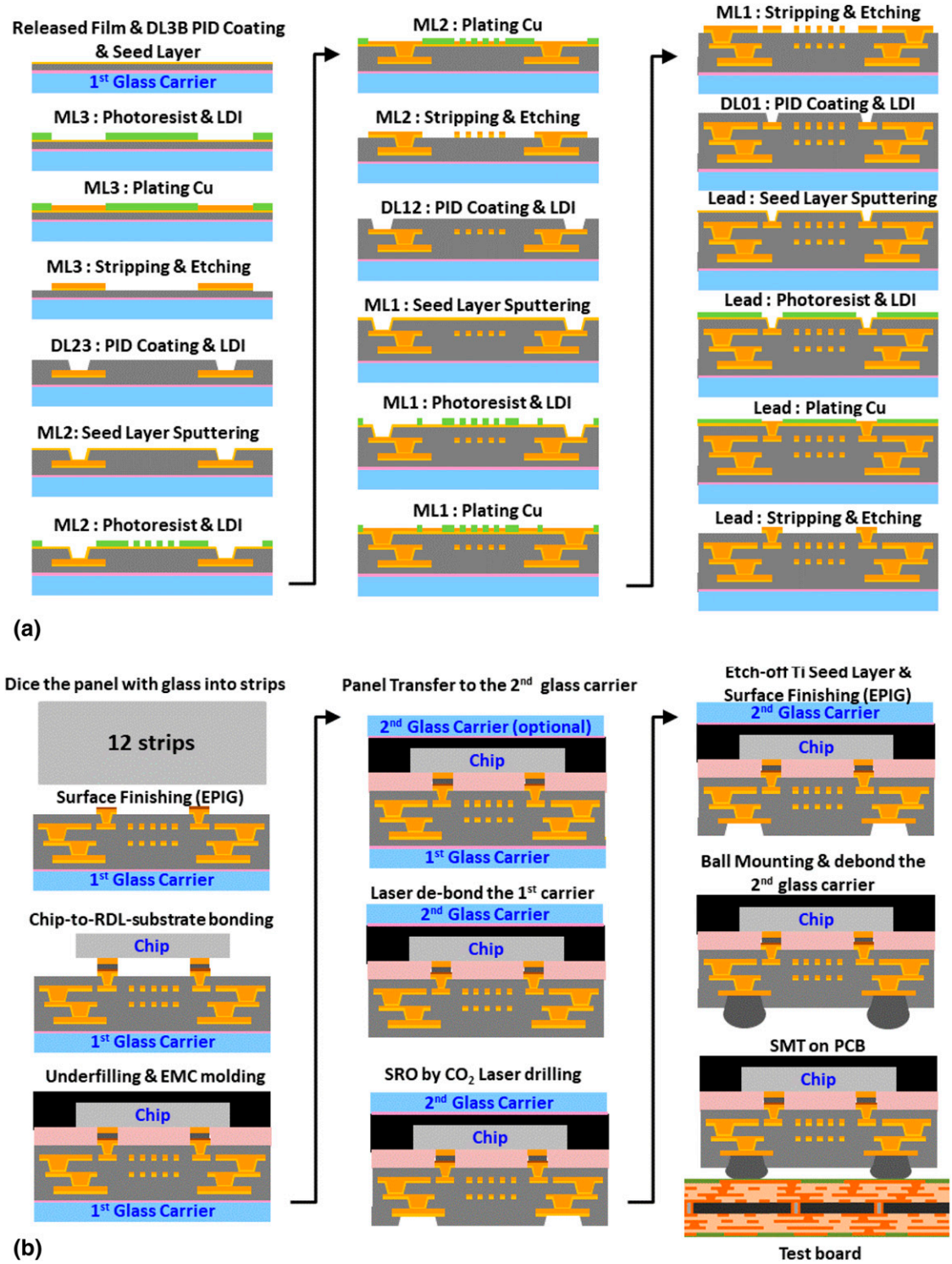

Fig. 5. (a) Key process steps in fabricating the RDL substrate, flip chip assembly, underfilling, EMC molding, solder ball mounting, and SMT assembly. (b) Key process steps in fabricating the RDL substrate, flip chip assembly, underfilling, EMC molding, solder ball mounting, and SMT assembly (continue).

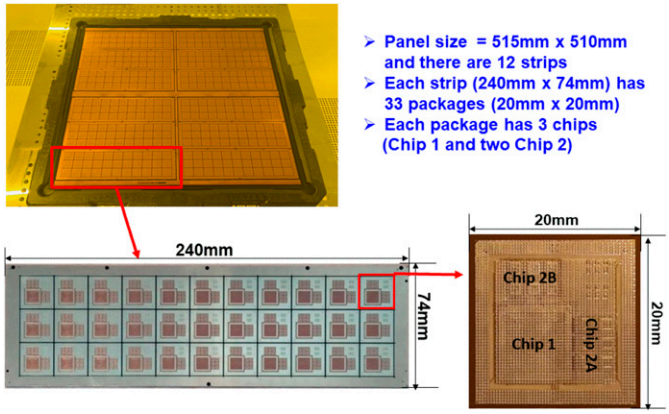

Fig. 6. The 396 (20×20 mm^2) RDL substrates are all fabricated at once on the 515×510 mm^2 glass panel. Then, the panel is cut into 12 strips and each strip is with 33 RDL substrates. Each 20×20-mm^2 RDL substrate is to support three chips (one large and two small).

built from the 2/2 μm metal L/S, whereas in this study, the RDLs are going to be built from the 10/10 μm metal L/S. Consequently, the vias connecting the MLs are different. Also, there is no need to transfer the RDL substrate to another temporary carrier before the chip-to-substrate bonding.

A. Fabrication of Redistribution-Layer Substrate

First, a released film (sacrificial layer) is slit coated on a temporary glass carrier (515×510 mm^2) and it is followed by slit coating a photoimageable dielectric (PID) for the solder mask (or passivation layer) DL3B as shown in Fig. 3a and Fig. 5a. Then, a Ti/Cu seed layer is formed by physical vapor deposition. It is followed by photoresist, laser direct imaging (LDI), and development. Then, electrochemical deposition (ECD) Cu and strip off the photoresist and etch off the Ti/Cu to obtain the ML (ML3) of RDL3.

It is followed by slit coating a PID and LDI to get the DL (DL23) of RDL3. Then, sputter the Ti/Cu seed layer, slit coat the photoresist, LDI and develop, and ECD the Cu. It is followed by stripping off the photoresist and etching off the TiCu seed layer to get the ML (ML2) of RDL2. It is followed by slit coating a PID and LDI to get the DL (DL12) of RDL2. Repeat the same process steps to obtain the ML (ML1) and DL (DL01) of RDL1. Then, sputter the Ti/Cu, slit coat the photoresist, LDI and develop, and ECD the Cu. It is followed by stripping off the photoresist and etching off the TiCu to get the bonding pad (lead) for the chips, which is shown in the last step of Fig. 5a.

Next, the glass panel (515×510 mm^2) with the fabricated 396 three-layer RDL substrates is cut into 12 strips. The dimensions of each strip are 240×74 mm^2, and each strip has 33 (20×20 mm^2) RDL substrates. Fig. 6 shows the panel, the strip, and the individual RDL substrate.

Fig. 7 shows the SEM images of a typical cross section of the RDL substrate. This cross section is showing (including) all three MLs (ML1, ML2, and ML3) of RDL1, RDL2, and RDL3. A closer look at the bottom SEM image, it can be seen that for RDL1, the linewidth does not meet the 2-μm target but equals 2.15 μm, 2.24 μm..., the line spacing does not meet the 2-μm target but equals 1.4 μm, 1.49 μm..., and the thickness also does

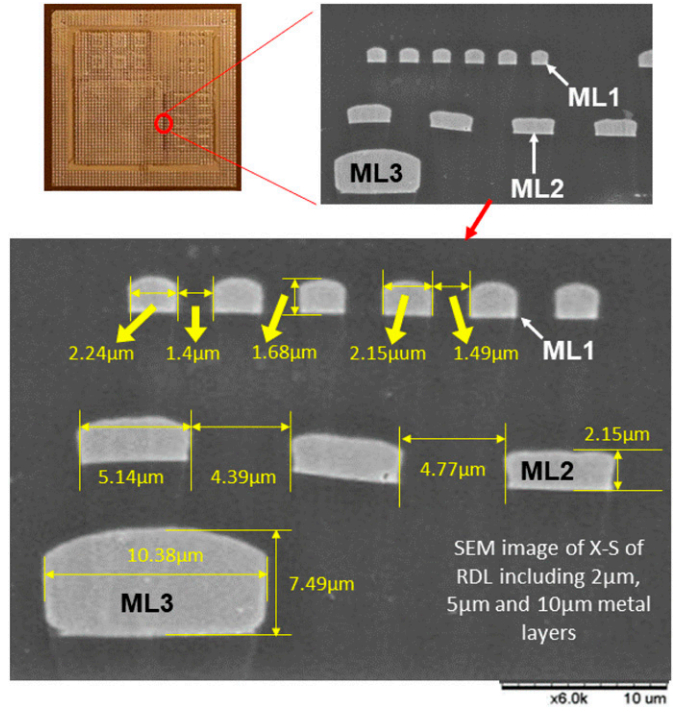

Fig. 7. SEM images of the RDL substrate showing the L/S of ML1, ML2, and ML3.

not meet the 2.5 μm target but equals 1.68 μm… Thus, there are rooms for improvements (such as use higher resolution LDI or a stepper). The linewidth, spacing, and thickness of ML2 are much better, and they are, respectively, 5.14, 4.77, and 2.15 μm, and the targets are 5, 5, and 2.5 μm. The linewidth and thickness of ML3 are, respectively, 10.38 μm and 7.49 μm, which are very close to the target values of 10 μm and 8 μm. This is understandable because the smaller the L/S, the larger the error.

The last step on the fabrication of the RDL substrate right before the chips-to-substrate bonding is the surface finishing of the Cu bonding pads. In this study, electroless palladium and immersion gold (EPIG) surface finishing is used. Fig. 8 shows the results at a few locations of the RDL substrate.

B. Wafer Bumping

In parallel, the test wafers are bumped with the C2 (chip connection) bumps [27] as shown in Fig. 1. After wafer bumping, the wafer is diced into individual chips. For all the bumped test chips, the bump consists of the Cu pillar, Ni barrier, and SnAg cap.

C. Chip-to-Substrate Bonding

Now, it is ready for chips-to-substrate bonding. Because of the support of the temporary glass carrier, the strip is very stiff and flat for bonding, Fig. 5b. Also, because the 2/2-μm ML1 of RDL1 is facing upward, there is no need to transfer the RDL substrate strip to another temporary carrier before chip bonding. This is the biggest difference between the current process and the one from [1].

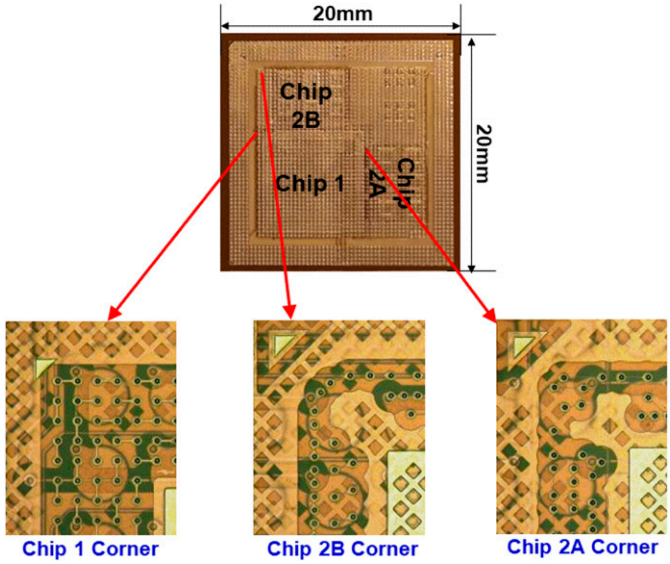

Fig. 8. The surface finishing (EPIG) of the bonding pad (of the RDL substrate) for the chips.

First, pick and place (P&P) all the chips on the strip, which is at room temperature. The P&P head condition for the large chip (chip 1) is shown in Fig. 9. It can be seen that the temperature rises very fast from 75°C to 250°C and then 275°C and stays there for 2.5 s, then drops very fast to 75°C. The applied force is small (10 N). The P&P head condition for the small chips (chip 2A and chip 2B) is also shown in Fig. 9. It can be seen that the temperature rises very fast from 75°C to 225°C and then 260°C and stay there for 1 s, then drops very fast to 75°C. The applied force is very small (5 N).

After the P&P of all the ($3 \times 33 = 99$) chips on the RDL substrate strip, it is put into a reflow oven for a solder mass reflow of all the chips. The reflow temperature profile is shown in Fig. 9. It can be seen that the maximum temperature is 250°C for the SnAg solder cap. Fig. 10a shows a strip with 33 RDL

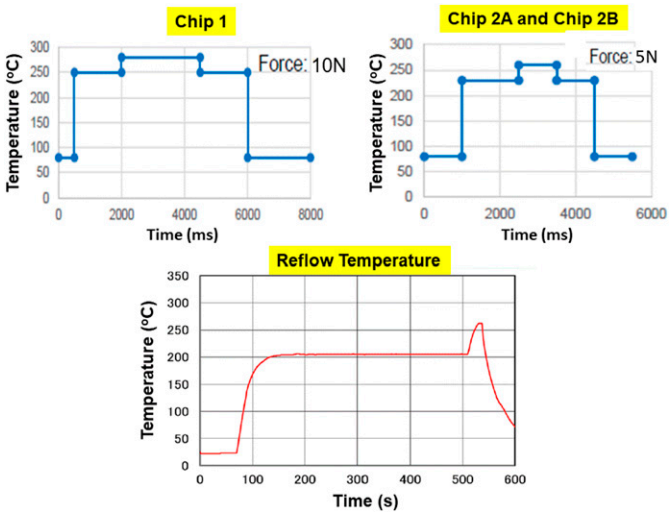

Fig. 9. Chip-to-substrate (temperature vs. time) bonding conditions for the large chip and small chips. Solder mass reflow condition for all the chips.

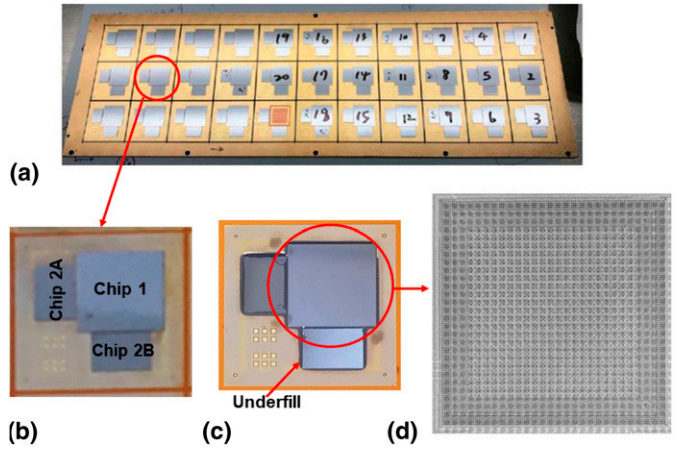

Fig. 10. (a) A strip with 33 heterogeneous integration packages after mass reflows. (b) A close-up. (c) After underfill. (d) X-ray for one of the large chips.

substrates and each with 3 chips as shown in Fig. 10b. Unlike the process in [1], the chip-to-substrate bonding is by thermo-compression (one chip at a time); the current process is very high throughout.

D. Underfilling and Epoxy Molding Compound Molding

After chips-to-substrate strip bonding, it is time for underfill dispensing and curing as shown in Fig. 5b. The underfill curing condition is 165°C for 2 h. A typical example is shown in Fig. 10c.

After underfilling all the packages on the strip, the whole strip is laminated with an EMC (400 μm-thick). The temperature and pressure conditions for the lamination are (1) first stage: 120°C/vacuum for 30 s and press = .68 MPa for 30 s and (2) second stage: 100°C and press = .58 MPs for 60 s. Fig. 10d shows the X-ray image of one of the large chips.

Fig. 11 shows a cross section of the chip bonded to the RDL substrate. The Cu pillar and solder cap of the chip, the underfill, and the ML1, ML2, and ML3 of the RDL substrate are clearly seen.

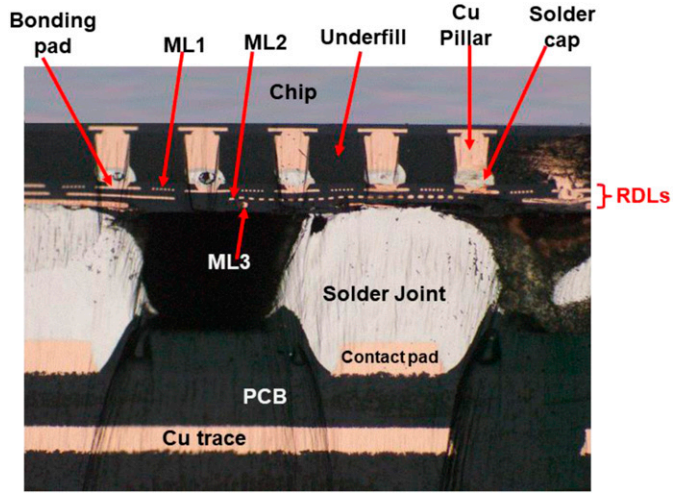

Fig. 11. Cross section image showing the chip-to-RDL-substrate bonding, solder ball mounting, and then SMT reflow on a PCB.

E. Strip Transfer

Depending on the thickness of the EMC, the strip transfer is optional. If the EMC thickness is thick enough (>500 μm), i.e., the stiffness of the strip with EMC embedded heterogeneous integration packages is strong enough to resist large (>1 mm) warpage after the original temporary glass carrier is removed, then there is no need to transfer the strip to another temporary carrier. Otherwise, the strip transfer to another glass carrier is necessary for the remaining process steps such as solder ball mounting. In this study, the strip was transferred to another temporary glass carrier and then the original temporary glass carrier was removed so that we can make SRO and surface finishing on the Cu contact pads as shown in Fig. 5b.

In this study, to save the EMC materials and have a lower profile heterogeneous integration package, the thickness of the EMC is only 400 μm, thus the transfer of the strip to another temporary glass carrier is necessary. Fig. 12 shows the case of strip transfer to another glass carrier and then remove the first temporary glass carrier. The warpage is .7 mm.

F. Solder Resist Opening and Surface Finishing

After the removal of the first temporary glass carrier by a laser, it is time to make the SRO and surface finishing as shown in 5(b). The 245-μm-diameter SRO is made by a CO_2 laser with four times of pulse. Then, it is followed by plasma etching the PID for 460 s and chemical etching the Ti for 270 s as shown in Fig. 13. The surface finishing is by EPIG with the thickness of Pd and Au, respectively, equal to .056 μm and .069 μm. The target values are .05 μm for both Pd and Au.

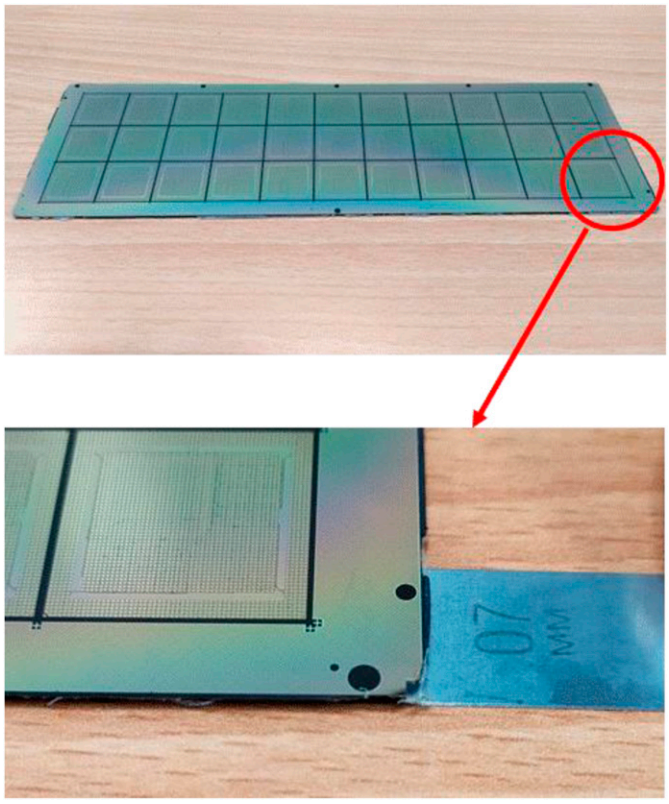

Fig. 12. After chip-to-substrate bonding, underfilling, and EMC molding, transfer the strip to another glass carrier and debond the original glass carrier.

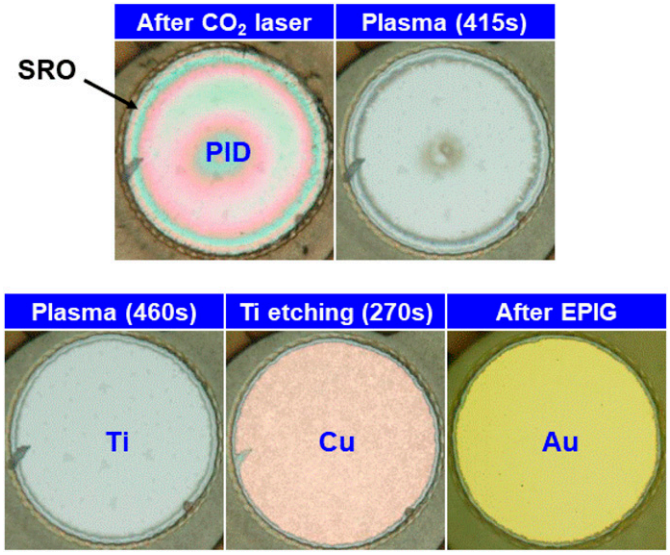

Fig. 13. Solder resist opening, plasma etching, Ti etching, and EPIG surface finishing.

G. Solder Ball Mounting, Debonding, and Strip Dicing

After the SRO and EPIG surface finishing, it is time for solder ball mounting. The equipment for solder ball mounting is exactly the same as those in [1]. Fig. 14 shows the solder balls mounted on a strip (the average solder ball height equals to 154.7 μm) and the size of an individual solder ball. The alloy of the solder ball is Sn_3Ag .5 Cu.

After solder ball mounting, it is time to remove the second temporary glass carrier from the strip. Finally, the strip was diced into individual heterogeneous integration packages.

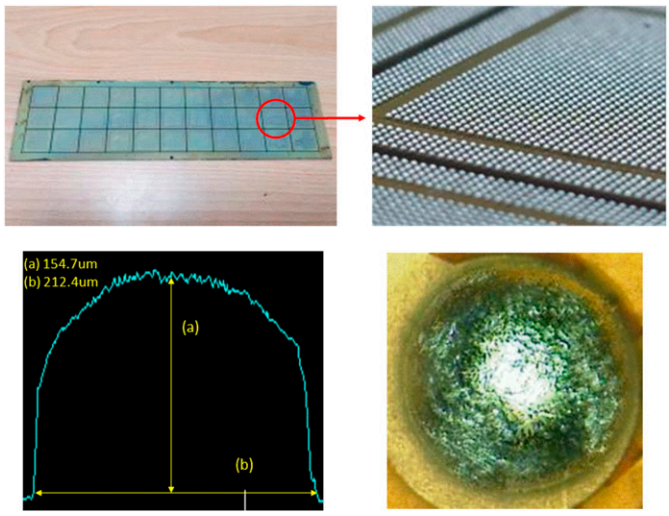

Fig. 14. Solder ball mounting after strip transferred to another temporary glass carrier.

Reliability Assessment

The reliability assessment of the present heterogeneous integration package is performed by the drop test.

A. Printed Circuit Board

The PCB for the heterogeneous integration package is made of FR-4 and is shown in Fig. 15. It can be seen that there are eight package sites on the board. The dimensions of the PCB are 132 × 77 × .992 mm^3, and there are eight layers. There are 2,780 pads (with a pitch = .35 mm) for each package. The pad with a diameter of .2 mm is nonsolder mask defined, and its surface finish is an organic solderability preservative. The solder mask opening diameter is .245 mm and the ball pad diameter is .18 mm.

B. SMT (Surface Mount Technology) Assembly of the Package

The SMT [28] assembly of the heterogeneous integration package on PCB is shown in Fig. 16. Fig. 16a shows the reflow temperature profile, and it can be seen that the maximum temperature is 245°C. Fig. 16b shows the assembled PCB with eight heterogeneous integration packages. Figs. 11 and 16c show a typical cross section of the PCB assembly where the chip, Cu pillar and solder cap, EMC, MLs of RDLs, solder joints, and PCB are clearly seen.

C. Drop Test

The shock (drop) test setup is according to JEDEC Standard ESD22-B111, as shown in Fig. 17. It consists of a drop tower, a drop table for the PCB with samples. There are 22 channels plus one common and a data acquisition system (DAS).

The drop spectrum with 1,500 G/ms (1,500-Gs, .5-ms half-sine pulse) is shown in Fig. 18. The drop condition is 30 drops. The failure criterion is when the measured resistance during the drop test reaches 1,000 Ω as shown in Fig. 19a. Less than that, it is considered no failure, as shown in Fig. 19b.

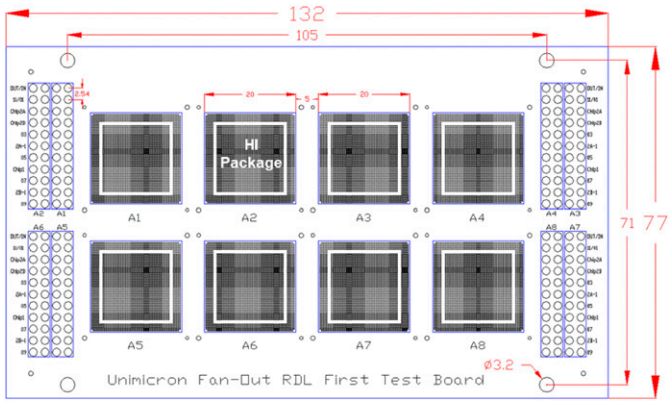

Fig. 15. Reliability test PCB with eight 20 × 20 mm^2 heterogeneous integration packages.

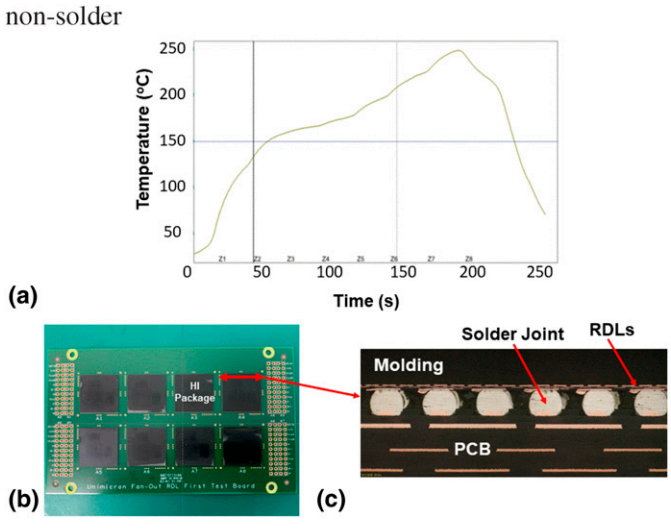

Fig. 16. (a) SMT reflow temperature profile. (b) The assembled test board. (c) Typical cross section of the PCB assembly.

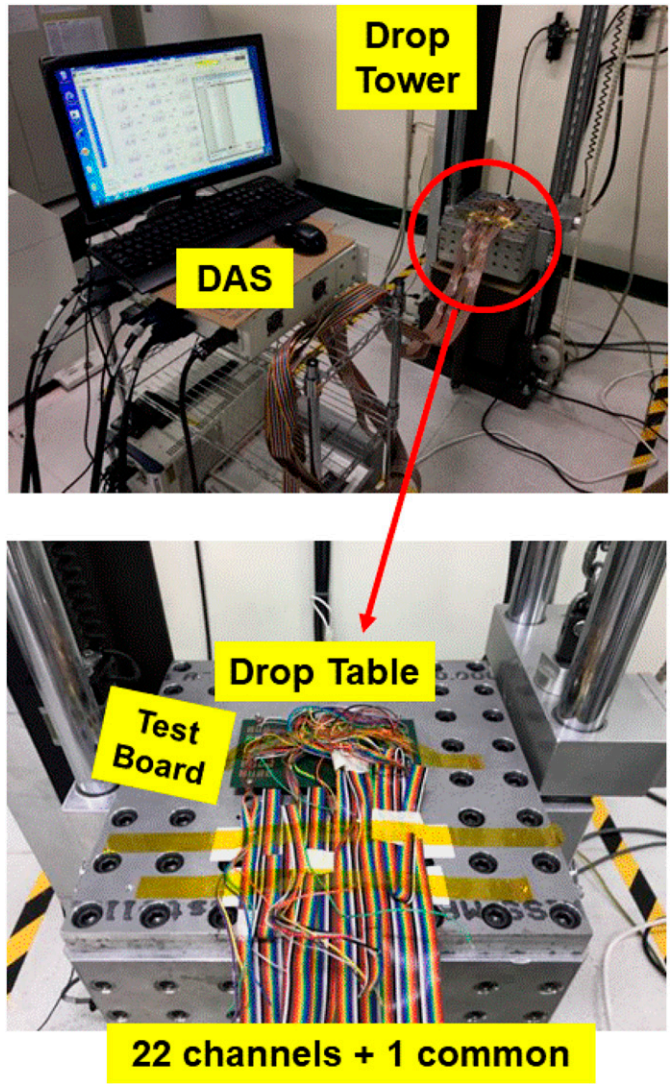

Fig. 17. Drop test setup, DAS, and samples.

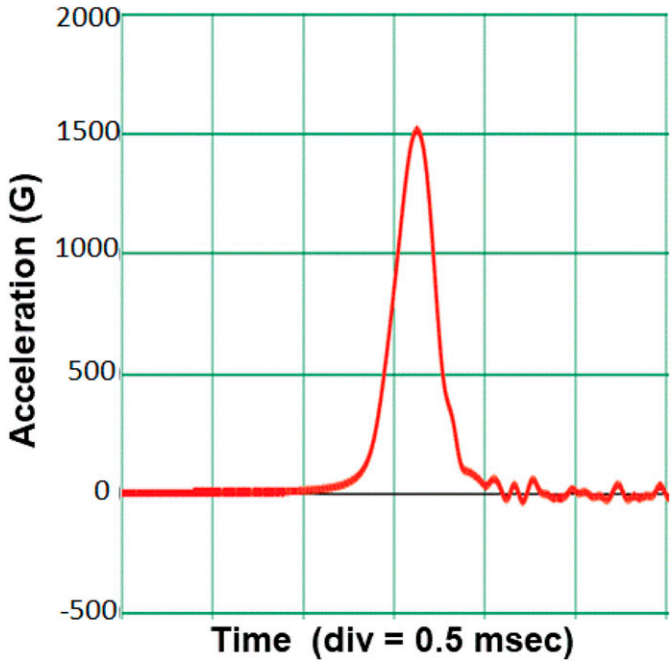

Fig. 18. The drop spectrum.

D. Drop Test Results and Failure Analysis

After 30 drops, there is only one failure which occurs after 23 drops. The DAS shows that the second package has failed (Fig. 20). Failure analysis by X-ray and cross sections indicates that the failure location of this package occurs near the corner solder joints and the edge near the middle of the PCB as shown in Fig. 20. However, this particular solder joint is bad to begin with. It is a head-in-pillow [28] solder joint. Before the drop test, the DAS cannot detect it and think it is a good solder joint. After 23 drops, the head is separated from the pillow, i.e., the solder joint is totally cracked. Thus, this sample should not be counted, and the heterogeneous integration package PCB assembly should be considered passing the drop test.

On the other hand, failure analysis on some nonfailure samples (the measured resistance is far less than 1,000 Ω as shown in Fig. 21b) indicates that there are some small cracks in the solder joint as shown in Fig. 21.

Conclusions

Some important results and recommendations are summarized as follows.

1. The feasibility of materials, process, fabrication, and assembly of the heterogeneous integration of three chips (one 10×10 mm^2 and two 7×5 mm^2) on an RDL substrate by an FOPLP method has been demonstrated.
2. The present RDL-first FOPLP gives high throughput. At one shot, all the 396 (20×20 mm^2) RDL substrates can be made at once on a 515×510-mm^2 temporary glass carrier.
3. The present RDL substrate consists of three RDLs. The targets of the L/S and thickness of ML1 of RDL1 are, respectively, 2/2 μm and 2.5 μm. Unfortunately, the fabricated linewidth of ML1 is 2.15, 2.24 μm…, the spacing of ML1 is 1.4, 1.49 μm…, and the thickness of ML1 is 1.68 μm. Thus, there are rooms for improvements, such as use high-resolution LDI or a stepper. The fabricated L/S and thickness of ML2 of RDL2 are much better in comparing with their target values. As expected, the fabricated linewidth and thickness of ML3 of RDL3 compared very well with the target values.

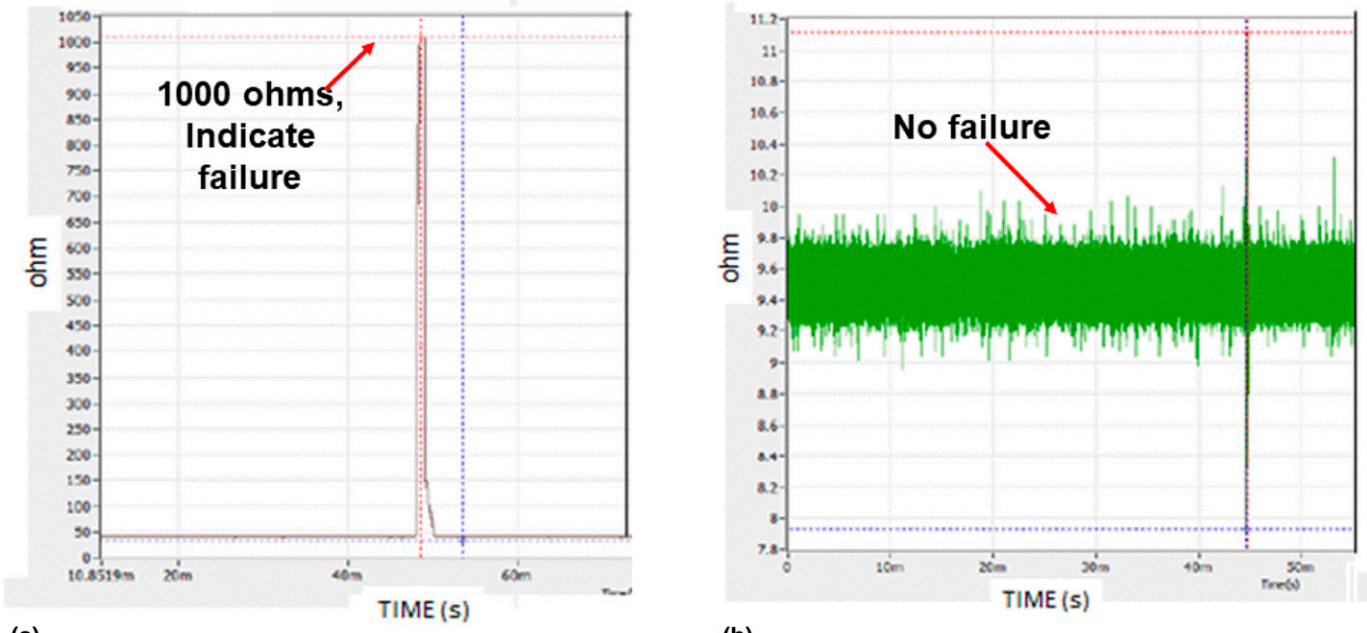

Fig. 19. Failure criterion. (a) When the resistance ≥1,000 Ω, it indicates failure. (b) No failure.

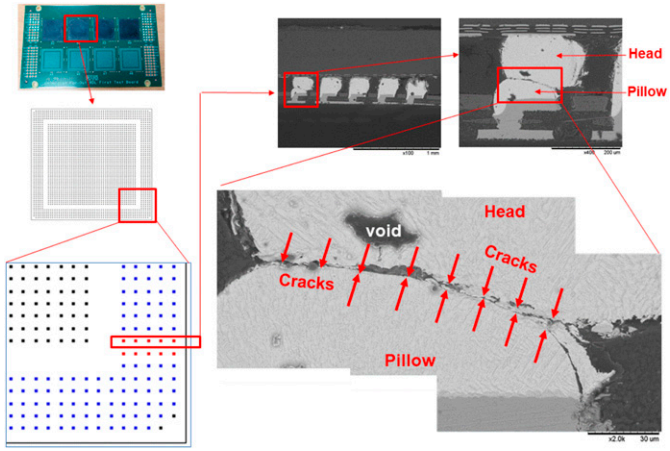

Fig. 20. The failure location and failure mode of the only failure sample under drop test. It turns out the failure sample to be bad (head-in-pillow) to begin with.

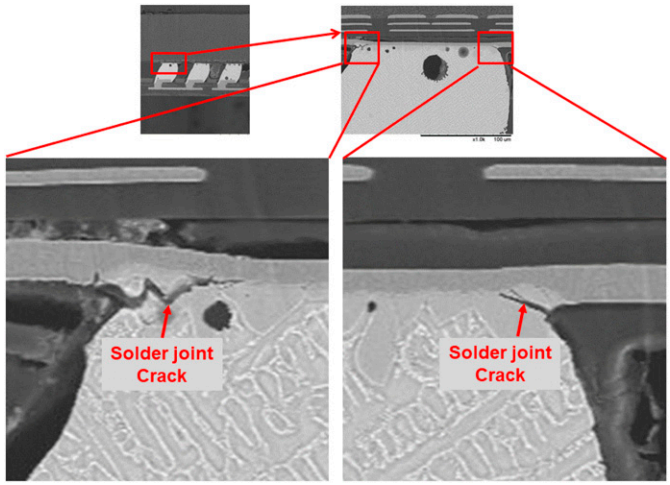

Fig. 21. No failure sample showing small cracks after drop test.

4. Because of the new process order (10 μm metal L/S first), there is no needed to transfer the fabricated RDL-strip substrate to another temporary carrier and then debond the original temporary glass carrier for chips-to-strip substrate bonding.
5. Chips-to-RDL-substrate bonding (with mass solder reflow of all the chips on the strip) can be performed with the original temporary glass carrier. This is another high throughput assembly feature in addition to the high throughput in making the RDL substrate on the large panel.
6. Reliability assessment of the heterogeneous integration of three chips on the RDL-first substrate package on PCB has been demonstrated (passed) through the shock (drop) test.

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