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Recent Advances and Trends in Heterogeneous Integrations

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***Abstract*—The recent advances and trends in heterogeneous integrations are presented in this study. Emphasis is placed on: (A) the definition of heterogeneous integrations, (B) the classifications of heterogeneous integrations such as heterogeneous integrations on (a) organic substrates, (b) silicon substrates (through-silicon via interposers), (c) silicon substrates (bridges), (d) fan-out RDL (redistribution-layer) substrates, and (e) ceramic substrates, and (C) the examples of heterogeneous integrations of chip-to-chip, chip-to-wafer, memory stacks, package-on-package, light-emitting diode, CMOS image sensors, micro-electro-mechanical systems, vertical-cavity surface-emitting laser, and photodetector. The trends of heterogeneous integrations are also presented.**

***Keywords*—Heterogeneous integrations, system-in-package, substrates, multichip module, through-silicon via, fan-out wafer-level packaging**

Introduction

Multichip module (MCM), system-in-package (SiP), and heterogeneous integration use packaging technology to integrate dissimilar chips, optical devices, and/or packaged chips with different materials and functions, from different fabless houses, foundries, wafer sizes, and feature sizes into a system or subsystem on different substrates or stand alone. What is the difference between MCM, SiP, and heterogeneous integration? The traditional MCM is mainly a 2D integration. The SiP can also be a 3D integration or called vertical-MCM or 3D-MCM. Heterogeneous integration is very similar to SiP, except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance applications. Actually, SiP can be considered a big subset of heterogeneous integration [1-99]. In this article, recent advances and trends in heterogeneous integrations will be presented. The MCM and SiP will be briefly mentioned first.

Multichip Module

MCM integrates different chips and discrete components side-by-side on a common substrate such as ceramic, silicon, or organic to form a system or subsystem for high-end networking, telecommunication, servers, and computer applications. Basically, there are three different kinds of MCM, namely, MCM-ceramic (MCM-C), MCM-deposited (MCM-D), and MCM-laminates (MCM-L).

A. Multichip Module-Ceramic

MCM-C are multichip modules that use thick-film technology such as fireable metals to form the conductive patterns and are constructed entirely from ceramic or glass-ceramic materials, or possibly, other materials having a dielectric constant above five. In short, an MCM-C is constructed on ceramic (C) or glass-ceramic substrates [100].

B. Multichip Module-Deposited

MCM-D are multichip modules on which the multilayered signal conductors are formed by the deposition of thin-film metals on unreinforced dielectric materials with a dielectric constant below five over a support structure of silicon, ceramic, or metal. In short, MCM-D uses deposited (D) metals and unreinforced dielectrics on a variety of rigid bases [100].

C. Multichip Module-Laminates

MCM-L are multichip modules which use laminate structures and use printed circuit board (PCB) technology to form predominantly copper conductors and vias. These structures may sometimes contain thermal expansion controlling metal layers. In short, MCM-L uses PCB technology of reinforced organic laminates (L) [100].

There was much research performed on MCMs during the 1990s. Unfortunately, at that time, because of the high cost of ceramic and silicon substrates and the limitation of linewidth and spacing of the laminate substrate, compounded with business models such as difficulty in getting the bare chips, the high-volume manufacturing (HVM) of MCMs never materialized, except some niche applications. Actually, since then, MCM has been a "dirty" word in semiconductor packaging.

System-in-Package

A. Intention of System-In-Package

SiP integrates different chips and discrete components, as well as 3D chip stacking of either packaged chips or bare chips (e.g., wide-bandwidth memory cubes and memory on logic with through-silicon vias [TSVs]) side-by-side on a common (either silicon, ceramic, or organic) substrate to form a system or subsystem for smartphones, tablets, high-end networking, telecommunication, server, and computer applications. SiP technology performs horizontal as well as vertical integrations. Some people also called SiP vertical-MCM or 3D-MCM.

B. Actual Applications of System-In-Package

Unfortunately, because of the high cost of TSV technology [101, 102] for smartphones and tablets, it never materialized. Most SiPs that went into HVM in the past 10 y are actually MCM-L for low-end applications such as smartphones, tablets, smart watches, medical, wearable electronics, gaming systems, consumer products, and internet of things–related products [103] such as smart homes, smart energy, and smart industrial automation. Most actual applications of SiPs by outsourced

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semiconductor assembly and tests (OSATs) integrate two or more dissimilar chips, components, and some discrete components on a common laminated substrate.

C. Potential Applications of System-In-Package

The applications of SiP for the high-price, high-margin, and high-end products are, e.g., dual-lens camera modules. However, right now, this SiP cannot be all performed by the OSAT, but also involves optical design, testing, lenses, micromotors, flexible substrate, and system integration capabilities which still need to be strengthened.

System-on-Chip

Moore's law [104] has been driving the system-on-chip (SoC) [105-107] platform. Especially, in the past 10 y, SoCs have been very popular for smartphones, tablets, etc. SoCs integrate different-function ICs into a single chip for a system or subsystem. Three typical SoC examples are shown in the following paragraphs.

A. Apple Application Processor (A10)

The application processor (AP) A10 is designed by Apple and manufactured by TSMC using its 16-nm process technology. It consists of a six-core graphics processor unit (GPU), two dual-core central processing unit (CPUs), two blocks of static random-access memories, etc. The chip area (11.6 × 10.8 mm) is 125 mm^2 (Fig. 1a).

B. Apple Application Processor (A11)

The AP A11 is also designed by Apple and manufactured using TSMC's 10-nm process technology. The A11 consists of more functions, including a tricore Apple-designed GPU, neural engine for face ID, etc. However, the chip area (89.23 mm^2) is about 30% smaller than that of the A10 because of Moore's law, i.e., the feature size is from 16 nm down to 10 nm (Fig. 1b).

C. Apple Application Processor (A12)

The AP A12, Fig. 1c, is also designed by Apple and manufactured using TSMC's 7-nm process technology. The A12 consists of much more functions, including an eight-core neural engine with artificial intelligence capabilities, four-core GPU which can run faster, six-core CPU which can performance better, etc. However, the chip area (83.27 mm^2) is about the same as that of A11.

Heterogeneous Integration

Some of the early researches in heterogeneous integration have been provided by Georgia Institute of Technology [108-110], where they reported a differential Si complementary metal-oxide semiconductor (CMOS) receiver IC (operating at 1

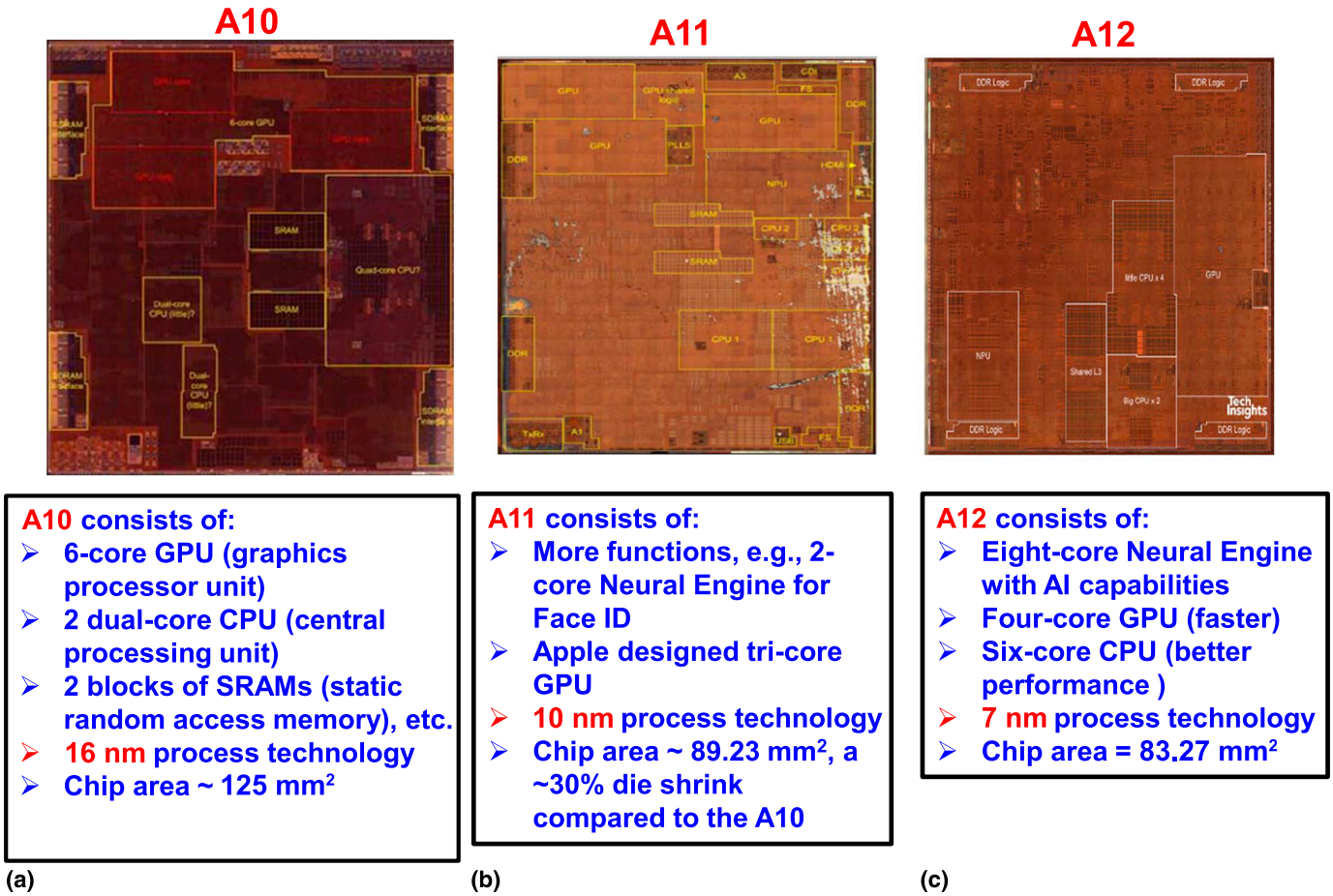


Fig. 1. SoC platforms for the A10, A11, and A12 APs.

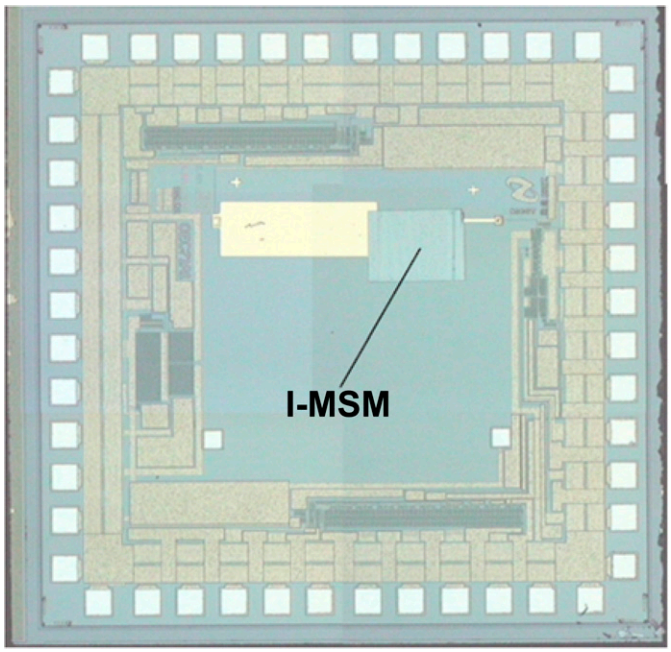


Fig. 2. InGaAs/InP I-MSM integrated onto differential Si CMOS receiver IC.

Gbps) integrated with a large-area thin-film InGaAs/InP I-metal-semiconductor-metal (MSM) photodetector (Fig. 2). Today, most heterogeneous integrations focus on higher density, finer pitch, and more complex system.

A. Heterogeneous Integration Versus System-On-Chip

Why is the heterogeneous integration of such great interest? One of the key reasons is because the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make SoCs. Heterogeneous integration contrasts with SoCs as follows. The heterogeneous integration uses packaging technology to integrate dissimilar chips (either side-by-side or stack) or components with different materials and functions, and from different fabless houses, foundries, wafer sizes, and feature sizes (as shown in Fig. 3) into a system or subsystem on different (e.g., organic, silicon, or redistribution layer [RDL]) substrates or stand alone, rather than integrating most of the functions into a single chip and going for a finer feature size.

B. Advantages of Heterogeneous Integration

For the next few years, we will see more of a higher level of heterogeneous integrations, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, or cost. Heterogeneous integration is going to take some of the

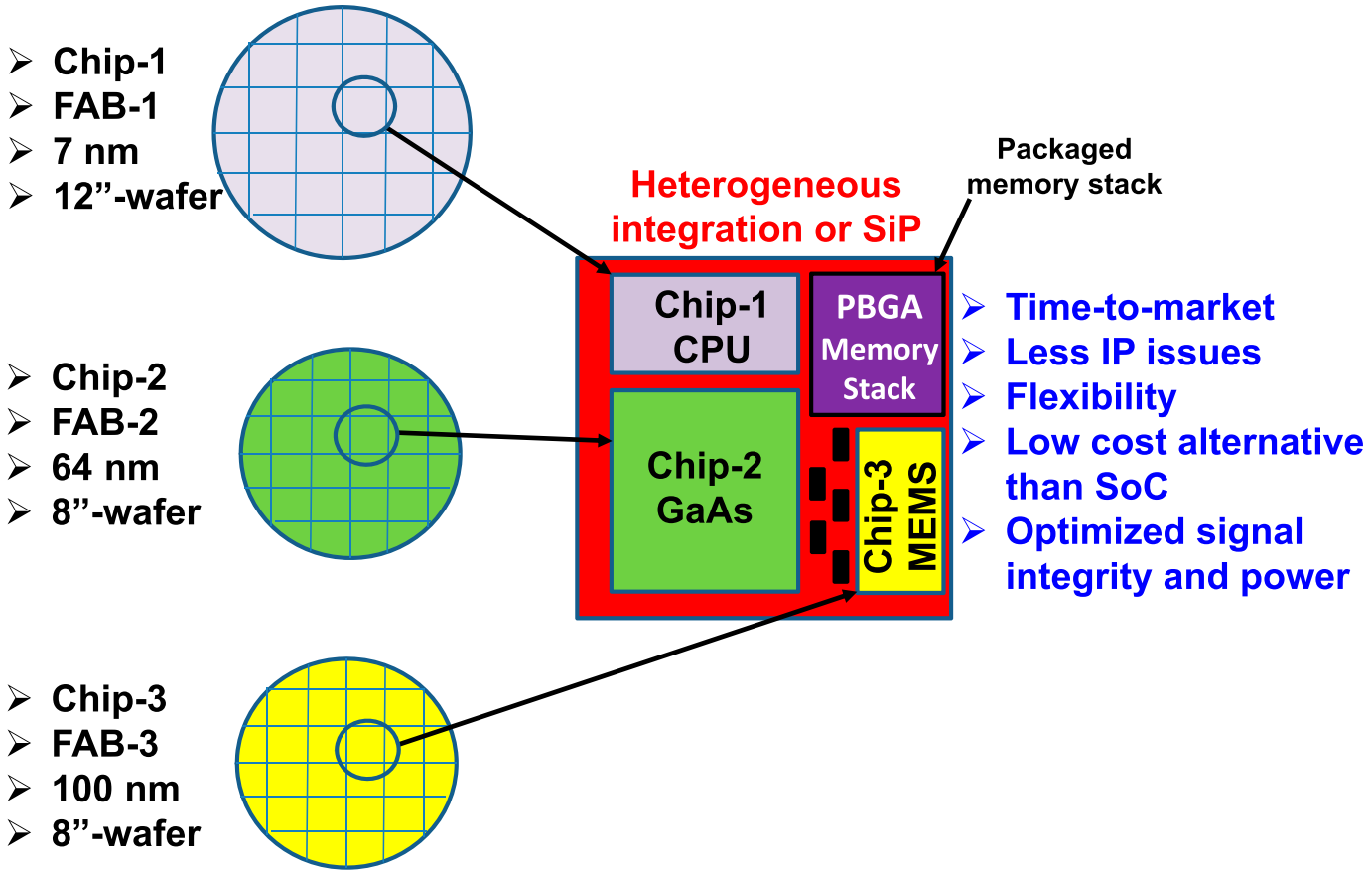


Fig. 3. Heterogeneous integration or SiP.

market shares away from SoCs on high-end applications such as high-end smartphones, tablets, wearable, networking, telecommunication, and computing devices. How should these dissimilar chips talk to each other, however? The answer is RDLs [111, 112]! In this article, the RDLs for heterogeneous integrations on organic substrates, silicon substrates (TSV interposers), silicon substrates (bridges), and fan-out substrates will be discussed. (RDLs for heterogeneous integrations on ceramic substrates such as the thermal conduction module will not be discussed.) Also, various applications of heterogeneous integrations of package-on-package (PoP), memory stacks, chip-to-chip stacks, light-emitting diode (LED), CMOS image sensors (CIS), microelectro-mechanical systems (MEMS), and vertical-cavity surface-emitting laser (VCSEL) will be briefly mentioned. SiP [37-99] is very similar to heterogeneous integration [1-36], except SiP is for coarser pitches, less I/Os, lower density, and lower performance applications.

Heterogeneous Integration on Organic Substrates

Today, the most common applications of heterogeneous integration are on organic substrates, or the so-called SiP. The assembly methods are usually surface mount technology including solder-bumped flip chips with mass reflow and wire bonding chips on board. In general, this is for low-end to middle-end applications.

A. Amkor's System-In-Package for Automobiles

Amkor's SiP for automobiles focuses on autonomous driving, infotainment, and advanced drive assist systems, and computer in a car. Figs. 4a and 4b, show a couple of examples of Amkor's SiP for automobiles. It can be seen from Fig. 4a that the 42.5 × 42.5-mm infotainment organic substrate is supporting the processor and double data rate memories, whereas from Fig. 4b, the 55 × 72-mm organic substrate is supporting the network switch, application-specific integrated circuit (ASIC), and memories.

B. Apple Watch III (System-In-Package) Assembled by Advanced Semiconductor Engineering (ASE) and iPhone XS and XS Max Assembled by Foxconn

Through Universal Scientific Industrial, ASE is a sole back end provider for Apple's custom-designed S3 SiP modules (Fig. 5a) for use in the Apple Watch III. It can be seen from Fig.

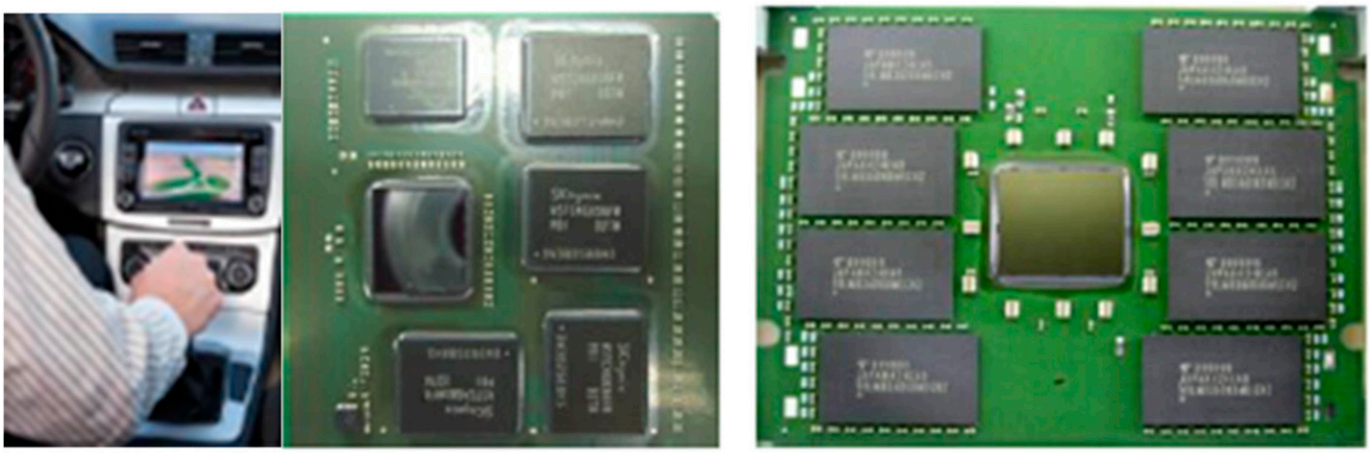


Fig. 4. Amkor's SiP for automobiles. (a) 42.5 × 42.5 mm infotainment. (b) 55 × 72 mm organic substrate.

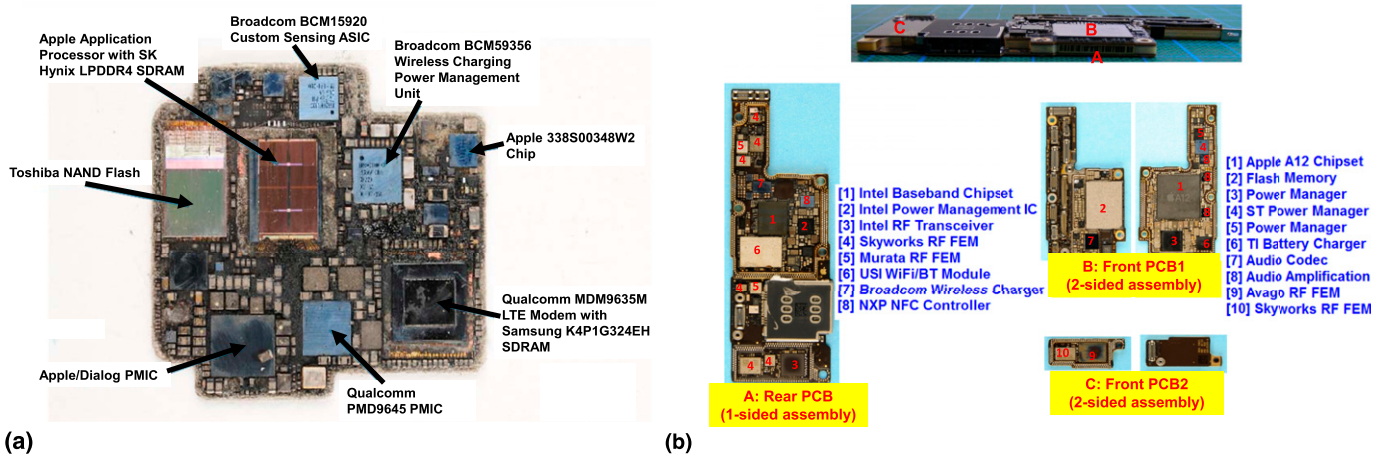


Fig. 5. (a) Apple's smart watch SIII assembled by ASE. (b) Apple's iPhones XS and XS Max assembled by Foxconn.

5a that there are >40 chips and are on an organic substrate. Some of these chips are discrete passive components such as capacitors and resistors, ASIC, processors, controller, converter, dynamic random access memory (DRAM), NAND, Wi-Fi, near-field communication, global positioning system, sensors, etc.

Fig. 5b shows the 3 SiPs in iPhone XS and XS Max assembled by Foxconn. The rear SiP is a single-side PCB which consists of the baseband chipset, PMIC, etc. The large SiP on top is a two-side PCB assembly which consists of the A12 chipset, flash memory, etc. The small SiP on top is also a two-side PCB assembly which consists of the RF FEMs (front-end modeles).

C. Cisco's Application-Specific Integrated Circuit and High-Bandwidth Memory on Organic Substrate

Fig. 6 shows a 3D SiP designed and manufactured with a large organic interposer (substrate) with fine-pitch and fine-line interconnections by Cisco [55]. The organic interposer has a size of 38 × 30 × 0.4 mm. The linewidth, spacing, and thickness of the front-side and backside of the organic interposer are the same and are, respectively, 6, 6, and 10 μm. A high-performance ASIC die measured at 19.1 × 24 × .75 mm is attached on top of the organic interposer along with four high-bandwidth memory (HBM) DRAM die stacks. The 3D HBM die stack with a size of 5.5 × 7.7 × .48 mm includes one base buffer die and four DRAM core dice, which are interconnected with TSVs and fine-pitch micro pillars with solder caps. This is for the high-end application.

D. Intel's Central Processing Unit and Micron's Hybrid Memory Cube on Organic Substrate

Fig. 7 shows Intel's Knights Landing CPU with Micron's hybrid memory cube (HMC), which have been shipping to Intel's favorite customers since the second-half of 2016. It can be seen that the 72-core processor is supported by eight multichannel DRAMs based on Micron's HMC technology. Each HMC consists of four DRAMs and a logic controller (with

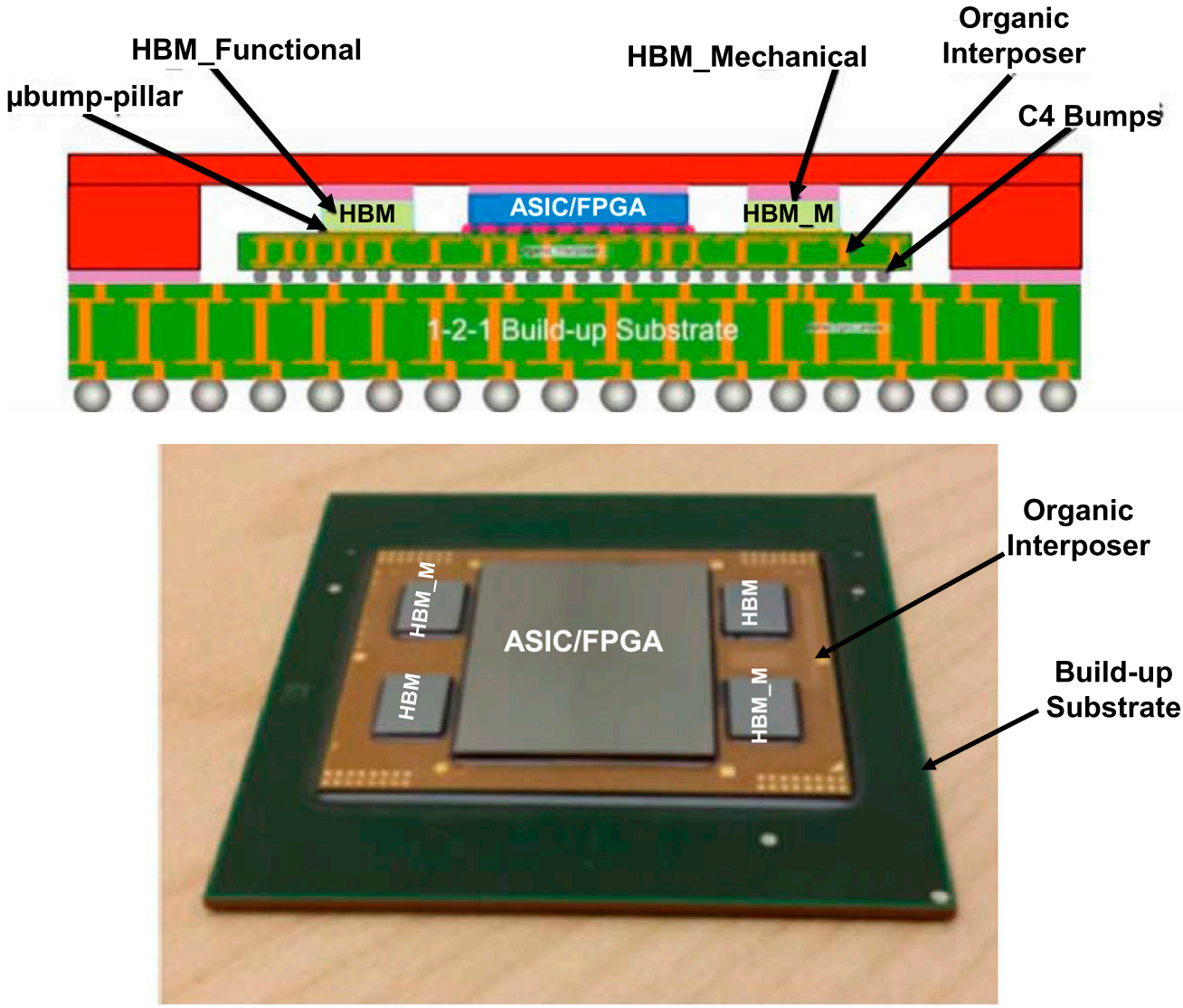


Fig. 6. Cisco's networking system with organic interposer.

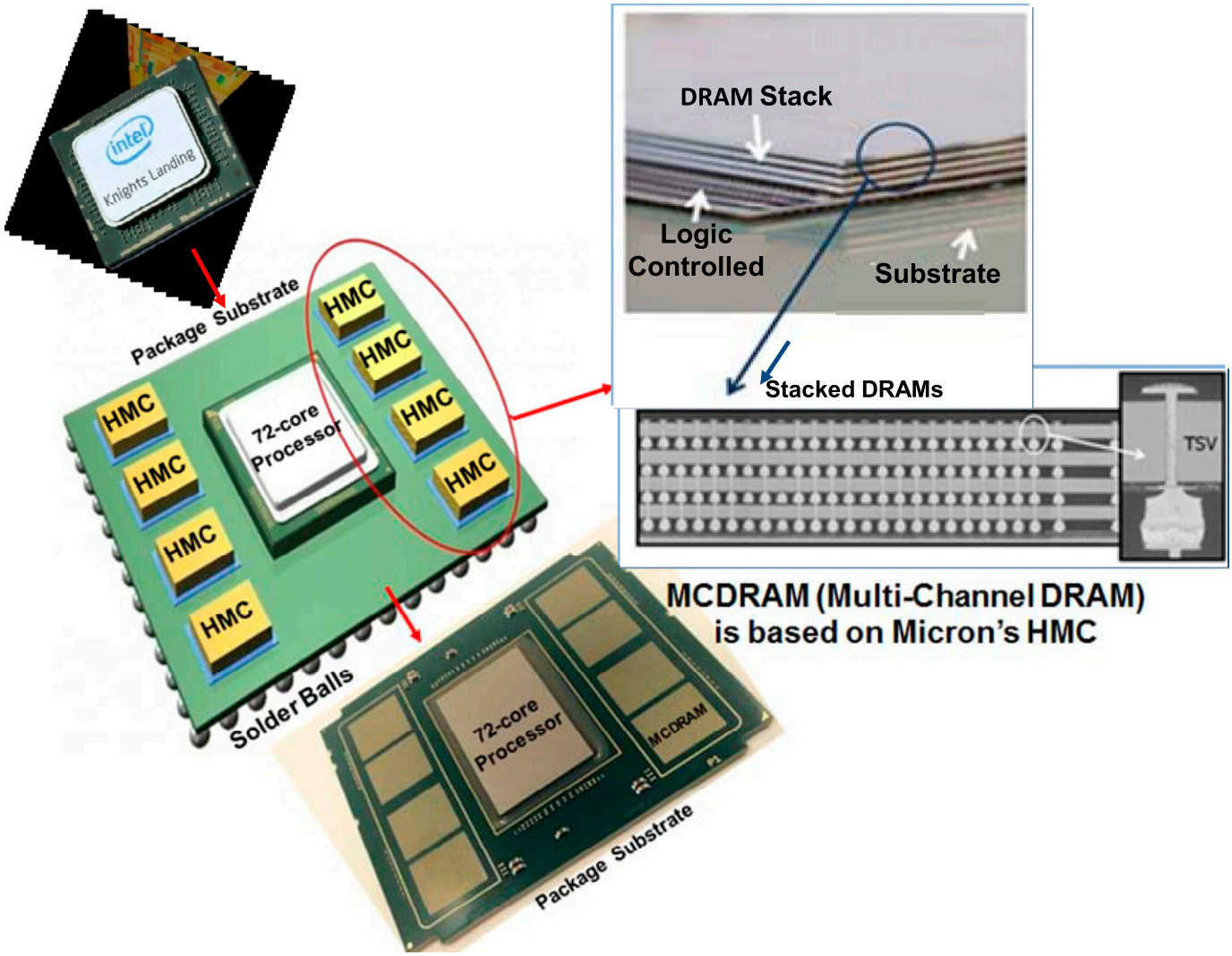


Fig. 7. Intel's Knights Landing and Micron's HMC on organic substrate.

TSVs), and each DRAM has >2,000 TSVs with Cu pillar bump with solder cap. The CPU and the DRAM + logic controller stacks are attached to an organic package substrate. This is for the high-end application.

Heterogeneous Integration on Silicon Substrates (Through-Silicon Via Interposer)

In general, heterogeneous integrations on silicon substrates are for multichip on silicon wafer or system-on-wafer (SoW). The assembly methods are usually flip chips-on-wafers (CoW) with TSVs with mass reflow or with thermocompression bonding for very fine pitches. In general, this is for high-end applications.

A. Leti's System-On-Wafer

One of the early applications of SoW is given by Leti [35, 36] as shown in Fig. 8. It can be seen that a system of chips such as ASIC and memories, power management IC (PMIC) and MEMS are on a silicon wafer with TSVs. After dicing, the individual unit becomes a system or subsystem and can be attached on an organic substrate or stand alone.

B. Institute of Microelectronics (IME's)System-On-Wafer

Mobile electronic products demand multifunctional module comprising digital, Radio-frequency (RF), and memory

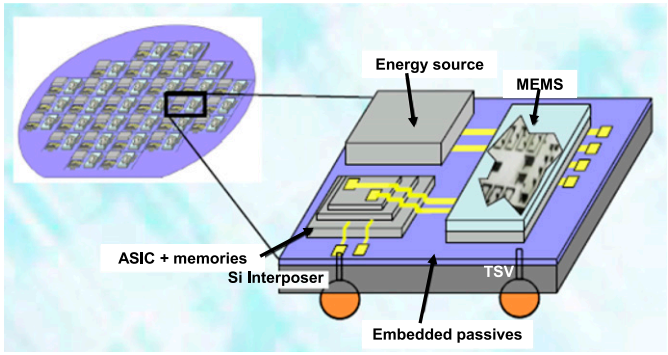


Fig. 8. Leti's heterogeneous integration (SoW).

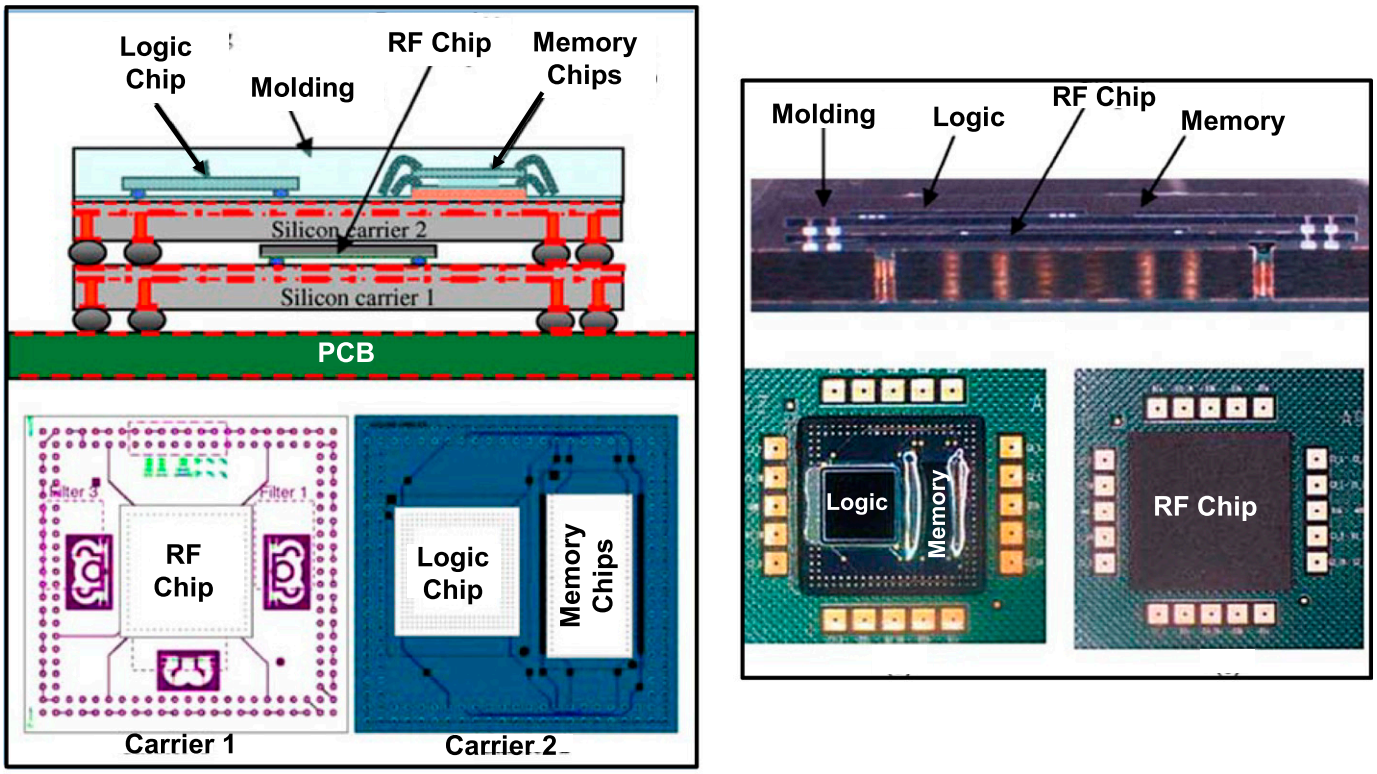


Fig. 9. IME's heterogeneous integration of RF chip, logic chip, and memory chips.

functions. TSV technology provides a means of implementing complex, multifunctional integration with a higher packing density for a heterogeneous integration. Fig. 9 shows a 3D module with silicon carrier [37]. The package consists of two stacks assembled with three chips. The module dimensions are 12 × 12 × 1.3 mm. The silicon carrier size is 12 × 12 mm with 168 peripherally populated via. Carrier 1 is assembled with a 5 × 5-mm flip chip. The carrier 2 is assembled with a 5 × 5 mm flip chip and two 3 × 6 mm wirebond-chip. The carrier 2 is overmolded to protect the wire bonds. The silicon carrier has been fabricated with two metal layers with SiO_2 as dielectric/passivation layer. Electrical connections through the carrier are formed by TSVs. The right-hand side of Fig. 9 shows the assembled structure.

C. Industrial Technology Research Institute (ITRI's) Heterogeneous Integrations

Fig. 10 shows a heterogeneous integration of various chips on a TSV interposer [38, 39]. It can be seen that the interposer (with 15 μm-vias) supports four memory chips (with 10 μm-vias) stacked, one thermal chip and one mechanical chip. It is overmolded for pick-and-place purpose as well as protecting the chips from harsh environments. There are RDLs on both top and bottom sides of the interposer. Also, stress sensors are implanted on the top side and integrated passive devices are fabricated through the thickness (100 μm) of the interposer (12.3 × 12.2 mm). This test vehicle can be degenerated to the case of (1) wide I/O DRAM if there are not mechanical and thermal chips and the interposer is an ASIC chip; (2) wide I/O memory if there is not the memory chip stacking nor the TSVs in the mechanical/thermal chips and the interposer is either an ASIC or microprocessor; and (3) wide I/O interface if there is not the memory chip stacking and there is not any TSV in the thermal/mechanical chips. Thus, the enabling technologies developed with this test vehicle can have very broad applications.

D. Xilinx/TSMC's Chip-On-Wafer-On-Substrate

In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced field-programmable gate array (FPGA), even a 12-buildup-layer (6-2-6) organic package substrate is not enough to support the chips and a TSV interposer is needed [42-54]. For example, Fig. 11 shows the Xilinx/TSMC's sliced FPBG CoW-on-substrate (CoWoS) [50-53]. It can be seen that the TSV (10 μm-diameter) interposer (100 μm-deep) has four top RDLs: three Cu damascene layers and one aluminum layer. The 10,000 + of lateral interconnections between the sliced FPGA chips are connected mainly by the .4-μm pitch (minimum) RDLs of the interposer. The minimum thickness of the RDLs and passivation is <1 μm. Each FPGA has more than 50,000 microbumps (200,000 + microbumps on the interposer) at 45 μm pitch as shown in Fig. 11.

E. Through-Silicon Via/Redistribution Layer Interposer with Chips on Both Sides

Fig. 12 shows the 3D IC heterogeneous integration of an interposer that supported one CPU or ASIC chip on its top side and two memory chips on its bottom side [55-59]. TSVs are embedded in the interposer uniformly and the sizes are 25 μm

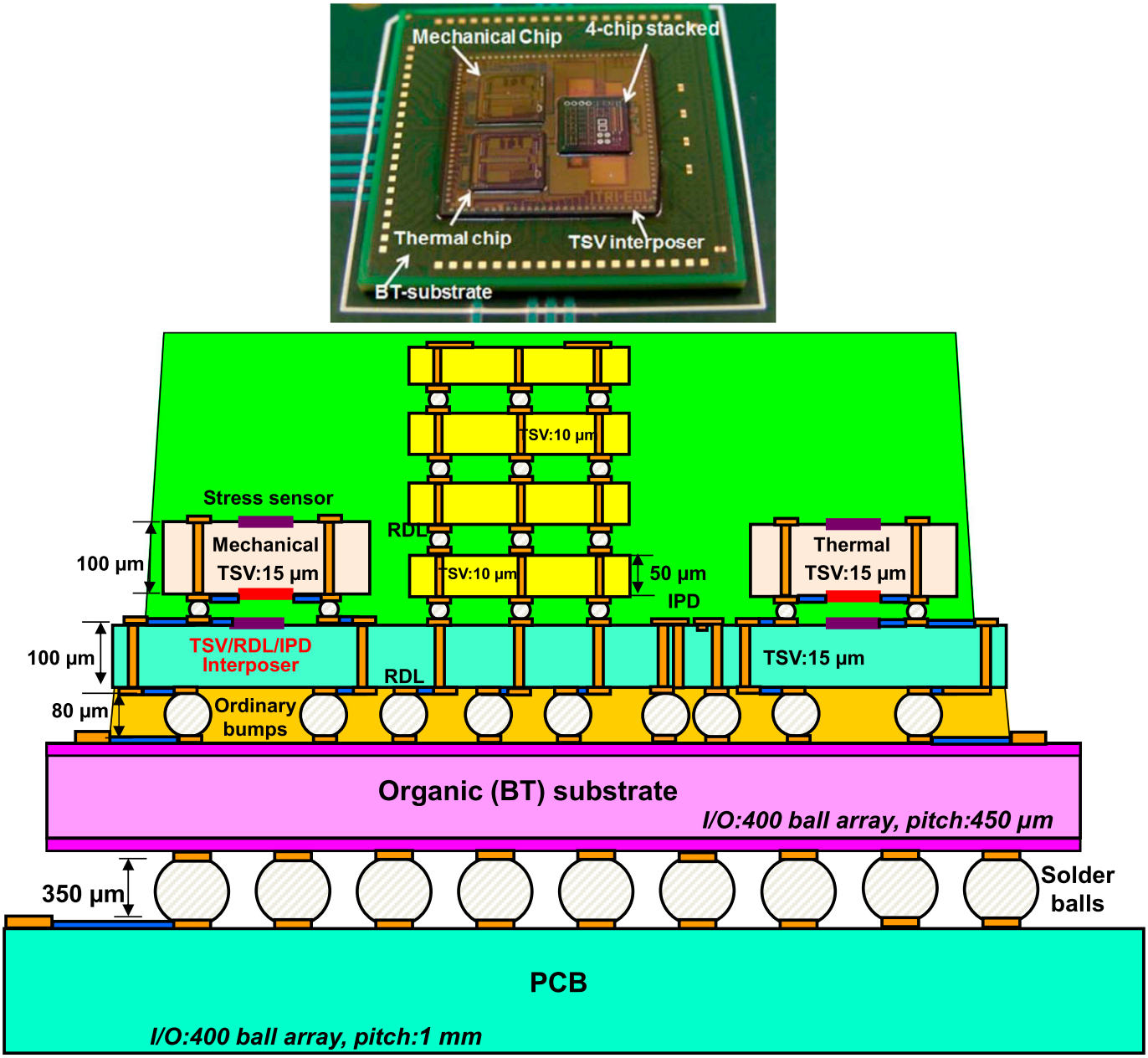


Fig. 10. ITRI's heterogeneous integration of memory cube, mechanical chip, and electrical chip.

in diameter, 150 μm in depth, and 150 μm in pitch; the thickness of passivation layer (SiO_2) on TSV sidewall is .5 μm. The interposer is attached to an organic substrate with ordinary bumps and the substrate is attached to a PCB with solder balls. The interposer is 28 mm × 28 mm × 150 μm, the CPU/ASIC is 22 mm × 18 mm × 400 μm, and the DRAM is 10 mm × 10 mm × 100 μm. The package substrate is 40 mm × 40 mm × 950 μm and the PCB is 114.3 mm × 101.6 mm × 1,600 μm.

The diameter of micro solder bumps between all the chips and the interposer is 25 μm and on 250 μm pitch. The diameter of the ordinary solder bumps is 150 μm and on 250 μm pitch. The diameter of the solder balls is 600 μm and on 1,000 μm pitch. The scanning electron microscope (SEM) image of a cross section of the 3D IC heterogeneous integration assembly is shown in Fig. 12. It can be seen that there is a larger and thicker chip on the top side of the passive interposer and a smaller and thinner chip on its bottom side. The micro solder joint between the top chip and the interposer is also enlarged and shown in Fig. 12. It can be seen that (1) the under bump metallurgy (UBM) on the interposer is Cu and Ni; (2) the solder becomes the intermetallic compound, Cu_6Sn_5; and (3) the Cu UBM from the larger chip. Similarly, the micro solder joint between the interposer with a TSV and the smaller chip is enlarged and shown in Fig. 12.

F. Interposer with Double-Sided Chip Attachments

The upper drawing of Fig. 13 shows the double-sided interposer for 3D IC heterogeneous integration of two chips on top

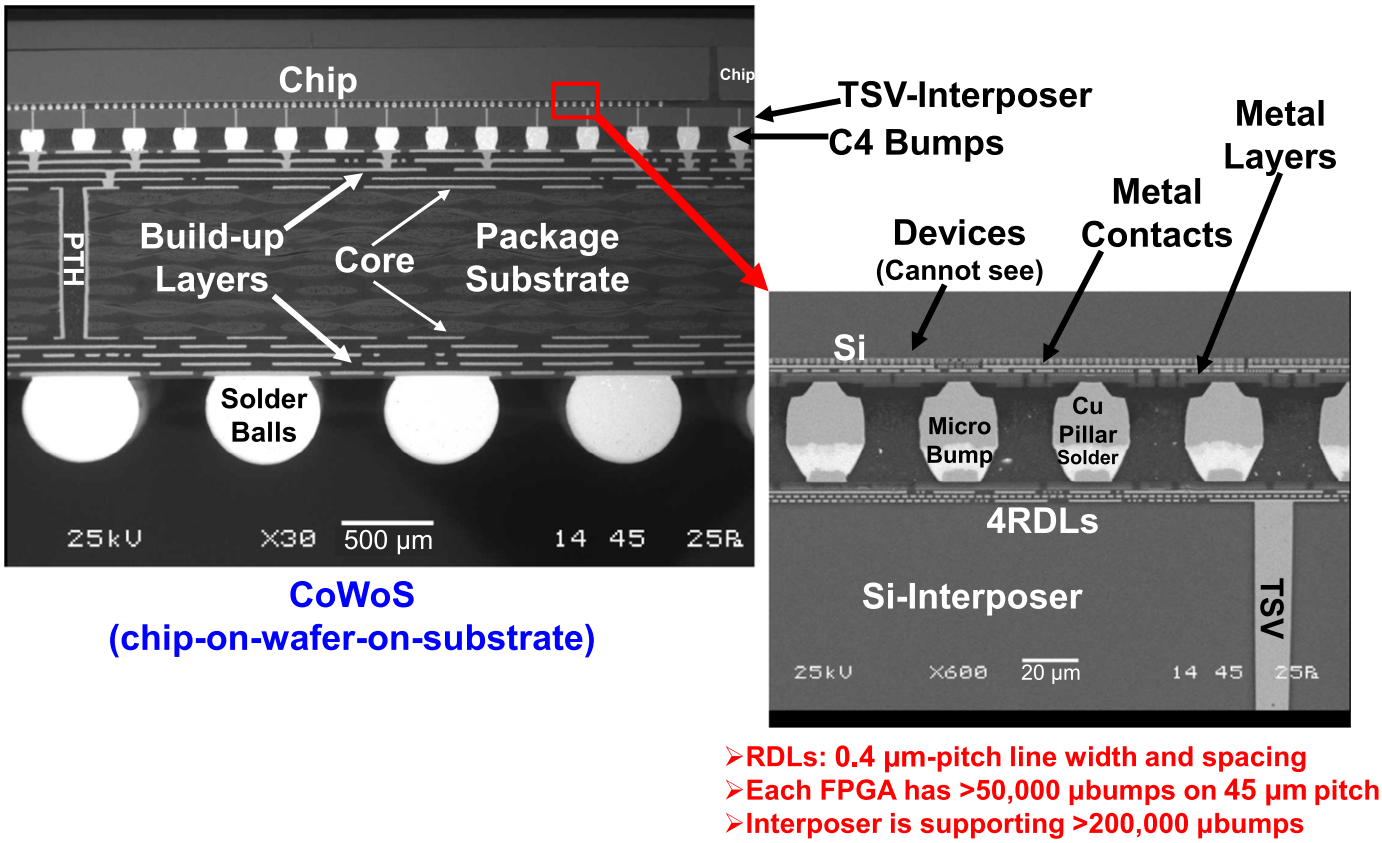


Fig. 11. Xilinx/TSMC's CoWoS.

and one chip at bottom [60-62]. The size of the package substrate is 35 mm × 35 mm × 970 µm. Underfills are used between the chips and interposer and the interposer and package substrate. The TSVs' diameter is 10 µm and on 150 µm pitch. The diameter of the solder bumps between the chips and interposer and between the interposer and package substrate is 90 µm and on 125 µm pitch. The diameter of the solder balls between the package substrate and the PCB is 600 µm and on 1,000 µm pitch. The bottom images of Fig. 13 show the cross sections of the full assembly module. It can be seen that the interposer is properly supporting the three chips with underfill. This interposer is soldered (with underfill) to a 4-2-4 package substrate.

G. Advanced Micro Devices (AMD's) Graphics Processor Unit and Hynix's High-Bandwidth Memory on UMC's Through-Silicon Via Interposer

Fig. 14 shows AMD's Radeon R9 Fury X GPU shipped in the second half of 2015. The GPU is built on TSMC's 28-nm process technology and is supported by four HBM cubes manufactured by Hynix. Each HBM consists of four DRAMs with Cu pillar + solder cap bumps and a logic base with TSVs straight through them. Each DRAM chip has >1,000 TSVs. The GPU and HBM cubes are on top of a TSV interposer (28 × 35 mm), which is fabricated by UMC with a 64-nm process technology. The final assembly of the TSV interposer with C4 (controlled collapse chip connection) bumps on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

H. NVidia's Graphics Processor Unit and Samsung's High-Bandwidth Memory2 on TSMC's Through-Silicon Via Interposer

Fig. 15 shows NVidia's Pascal 100 GPU, which was shipped in the second half of 2016 [41]. The GPU is built on TSMC's 16-nm process technology and is supported by four HBM2 (16 GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with Cu pillar + solder cap bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1,000 TSVs. The GPU and HBM2s are on top of a TSV interposer (1,200 mm^2), which is fabricated by TSMC with a 64-nm process technology. The TSV interposer is attached to a 5-2-5 organic package substrate with C4 bumps.

I. IME's MEMS Based Tunable Laser Source on Si-Substrate

In 2007, IME proposed a MEMS based tunable laser source with Si-modulator, polymer couplers, and III-IV gain chip on a silicon optical bench (w/o TSVs), which is cooled by a thermoelectric cooler as shown schematically in Fig. 16. The key features of the MEMS actuator are: driving voltage = 30 V@30µm displacement, resonant frequency = 2.559kHz, crosstalk < −60dB, polarization dependent loss < 0.1dB, wavelength-dependent loss < 0.05dB, rising time=75.6µs, falling time=63.4µm, and reliability > 1 × 107 times. The key features of the Si-modulator are: total length = 3500µm, splitter = 30µm, combiner = 30µm, modulator length ~3440µm, cross section ~0.4µm × 0.35µm, designed maximum frequency > 20 GHz, and designed propagation loss < 20dB/cm.

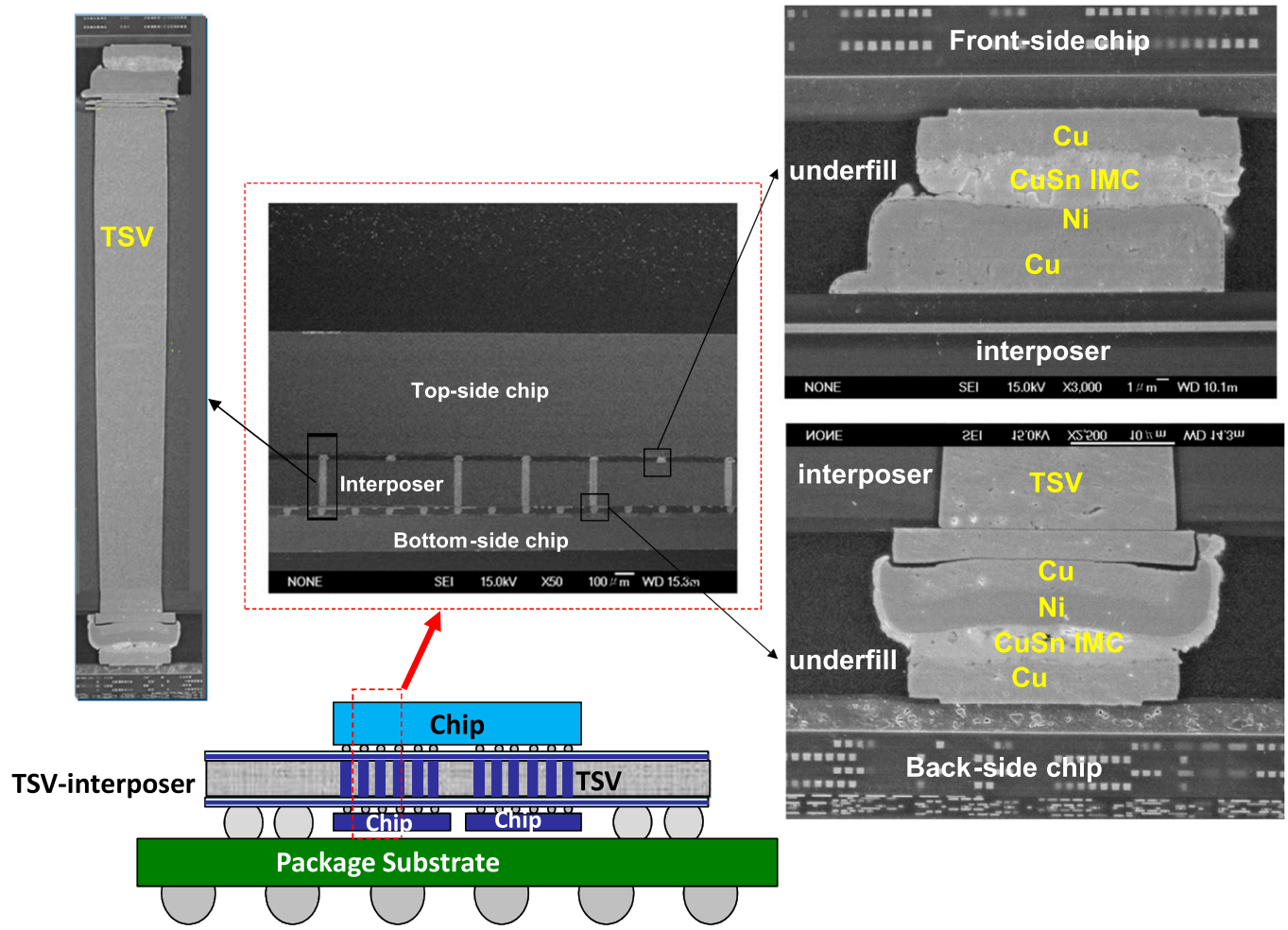


Fig. 12. TSV/RDL interposer with chips on both sides.

J. University of California at Santa Barbara (UCSB)/AMD's chiplets on Through-Silicon Via interposers

Excited by the Defense Advanced Research Projects Agency (DARPA) program called Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS), UCSB and AMD [63] proposed a future very high-performance system shown in Fig. 17. This system comprises a CPU chiplet and several GPU chiplets, as well as HBMs on a passive TSV interposer and/or on an active TSV interposer with RDLs.

Heterogeneous Integration on Silicon Substrates (Bridges)

Basically, a bridge is a piece of dummy silicon with RDLs and contact pads, but without TSVs. Usually, the RDLs and contact pads are fabricated on a dummy silicon wafer and then diced into individual bridges.

A. Intel's Embedded Multidie Interconnect Bridge for heterogeneous integration

Intel proposed embedded multidie interconnect bridge (EMIB) [30, 31] RDLs to replace the TSV interposer in heterogeneous integration systems. The lateral communication between the chips will be taken care of by the silicon-embedded bridge with RDLs, and the power/ground and some signals will go through the organic package substrate (or PCB) as shown in Fig. 18. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB, and the other is to make the substrate with EMIB. To make the EMIB, one must first build the RDLs (including the contact pads on a Si wafer). Finally, attach the non-RDL side of the Si wafer to a die-attach film (DAF), and then singulate the Si wafer into individual bridges. To make the organic substrate with an EMIB, first place the singulated EMIB with the DAF on top of the Cu foil in the cavity of the organic substrate. That step is followed by the standard organic package substrate build-up process all the way to the Cu-contact pads. The organic package substrate with the EMIB is ready for bonding of the chips such as the GPU and HBM cube, as shown in Fig. 19.

B. Imec's Bridges for Heterogeneous Integrations

Ever since Intel's proposal of using EMIB to serve as the high-density interconnects between chips in a heterogeneous integration system was put forth, the "bridge" has been very popular. For example, recently, IMEC proposed [33] the use of the

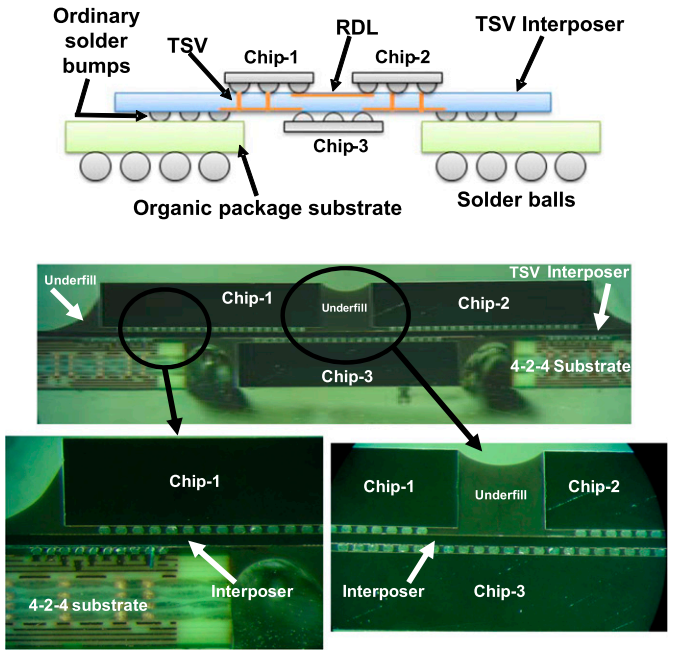


Fig. 13. Silicon interposer with double-sided chip attachments.

bridges + fan-out wafer-level packaging (FOWLP) technology to interconnect the logic chip, wide I/O DRAM, and the flash memory as shown in Fig. 20. Their objective is not to use TSVs for all the device chips.

C. ITRI's Bridge for Heterogeneous Integrations

Fig. 21 shows a heterogeneous integration with a through-silicon hole (TSH) interposer (a bridge) supporting a few chips on its top and bottom side [34]. The key feature of TSH interposers is that there is no metallization in the holes. Thus, dielectric layer, barrier and seed layers, via filling, Chemical-Mechanical Polishing (CMP) for removing overburden copper, and Cu revealing are not necessary. Comparing with the TSV interposers, TSH interposers only need to make holes (by either laser or deep reactive-ion etching (DRIE)) on a piece of silicon wafer. Just like the TSV interposers, RDLs are needed by the TSH interposers. The TSH interposers can be used to support the chips on its top side and bottom side. The holes can let the signals of the chips on the bottom side transmit to the chip on the top side (or vice versa) through the Cu pillars and solders. The chips on the same side can communicate to each other with the RDLs of the TSH interposer. Physically, the top chips and bottom chips are connected through Cu pillars and micro solder joints. Also, the peripherals of all the chips are soldered to the TSH interposer for structural integrity to resist shock and thermal conditions. In addition, the peripherals of the bottom side of the TSH interposer have ordinary solder bumps which are attached to a package substrate. Fig. 21 shows the SEM image of a cross section of a SiP [34], which includes all the key elements such as the top chip, TSH interposer, bottom chip, package substrate, PCB, microbumps, solder bumps, solder ball, TSH, and Cu pillars. It can be seen through the x-ray and SEM images that the key elements of SiP structure are properly fabricated.

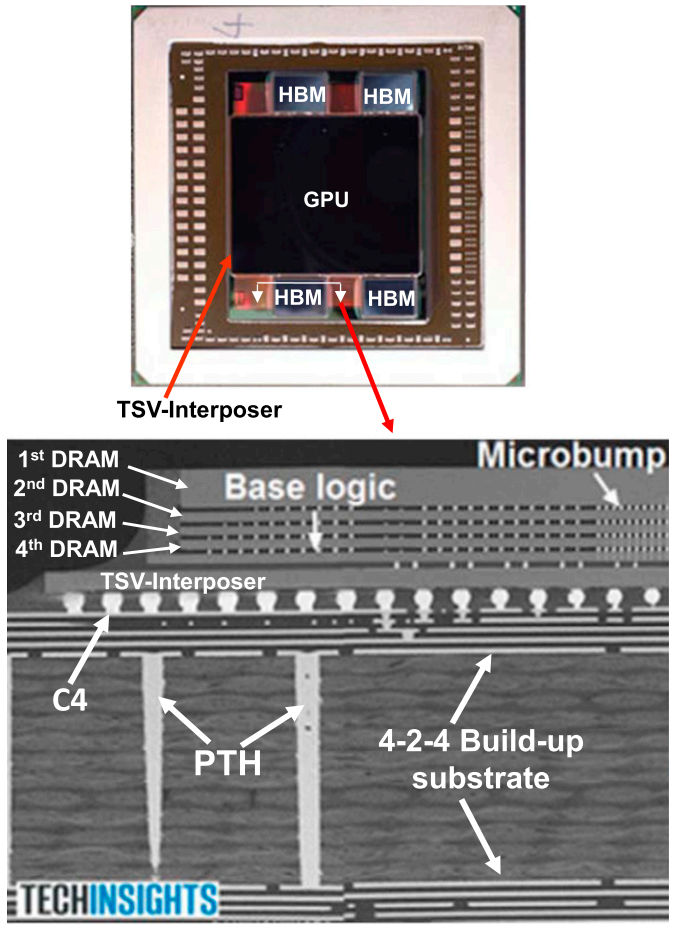


Fig. 14. AMD's heterogeneous integration of GPU and HBM.

Fan-Out Wafer/Panel-Level Packaging for Heterogeneous Integrations

Fan-out wafer/panel-level packaging [113-133] is very suitable for heterogeneous integrations. Two examples, one for FOWLP and the other for fan-out panel-level packaging (FOPLP) are briefly mentioned.

A. Fan-Out Wafer-Level Packaging for Heterogeneous Integrations

Fig. 22 shows a reconstituted wafer which consists of 629 (10 × 10 mm) packages [7,21]. Each package has four (one 5 × 5 mm and three 3 × 3 mm) chips and four (0402) capacitors. The spacing between the large chip and the small chip is 100 μm. There are two RDLs for each package. It should be emphasized that FOWLP is a very high-throughput process. In this case, in one shot, it can produce 629 10 × 10 mm packages. Fig. 23 shows the cross section of the package. It can be seen that there are two RDLs, and the thickness of the metal layer of RDL1 is 3 μm and that of RDL2 is 7.5 μm. The linewidth and spacing of RDL1 are 10 μm and those of RDL2 are 15 μm. The dielectric layer thickness of DL1 and DL2 is 5 μm and DL3 is 10 μm. The opening of the passivation (DL3) is 180 μm. The solder ball size is 200 μm and the ball pitch is .4 mm.

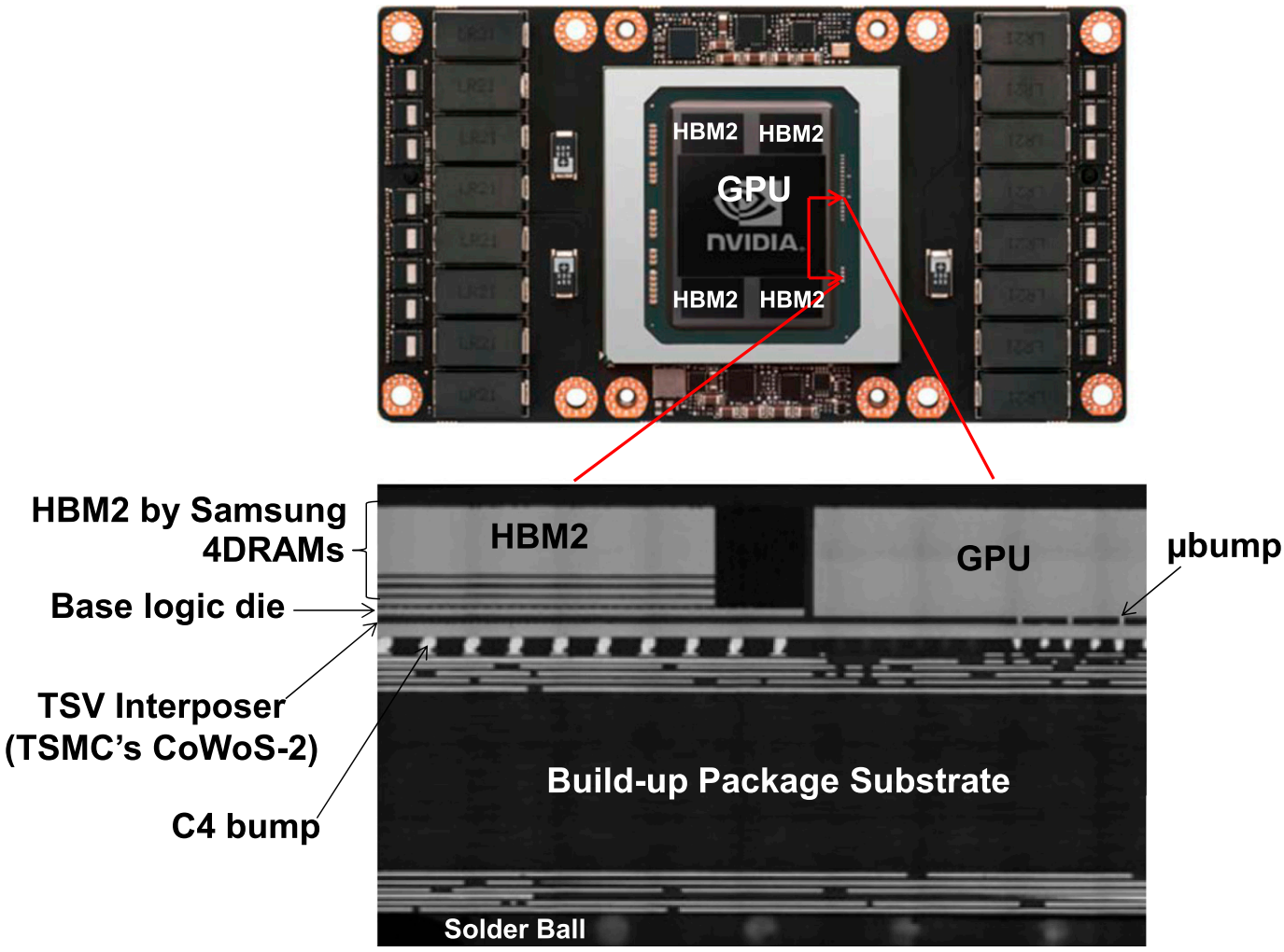


Fig. 15. NVidia's heterogeneous integration of GPU and HBM2.

B. FOPLP for Heterogeneous Integrations

Fig. 24 shows a reconstituted panel which consists of 1,512 (10 × 10 mm) packages [3, 22]. Again, each package has four (one 5 × 5 mm and three 3 × 3 mm) chips. Fig. 25 shows the x-ray image and the cross section of the package. It can be seen that there are two RDLs and the thickness of the metal layer of RDL1 and RDL2 is 10 μm. The linewidth and spacing of RDL1 are 20 μm and those of RDL2 are 25 μm. The dielectric layer thickness of DL1, DL2, and DL3 is 20 μm. The opening of the passivation (DL3) is 180 μm. The solder ball size is 200 μm and the ball pitch is .4 mm.

Heterogeneous Integrations on Fan-Out Redistribution Layer Substrates

Recently, to lower the package profile, enhance the performance, and lower the cost, the heterogeneous integration on RDLs by fan-out have been very popular, especially with the FOWLP technology. In general, this is for middle-end to high-end applications.

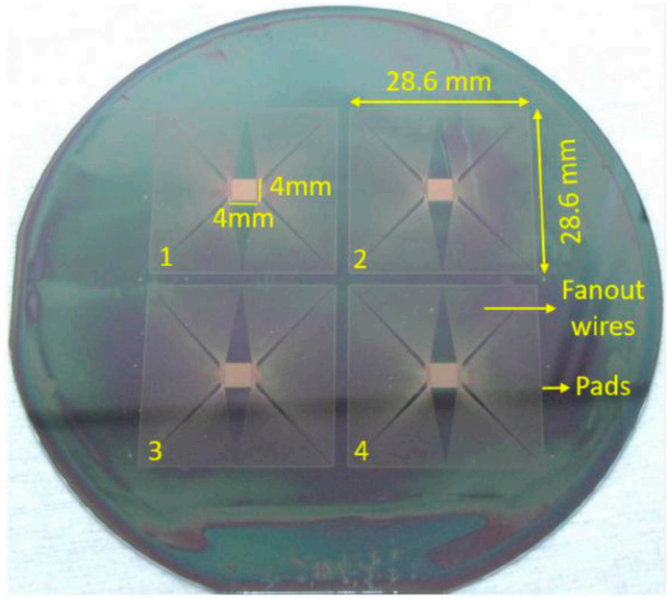


Fig. 16. IME's MEMS based tunable laser source on Si-substrate.

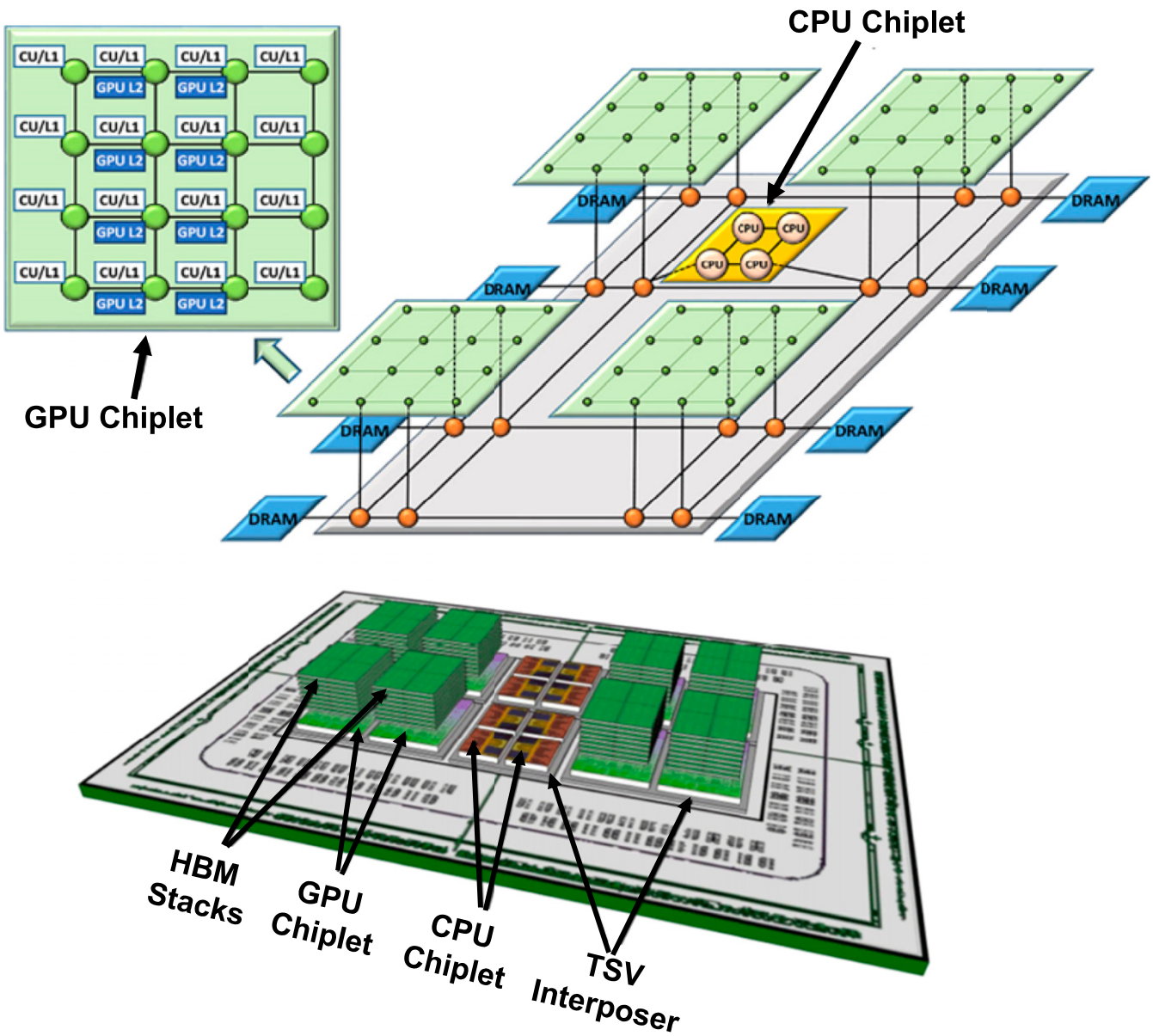


Fig. 17. UCSB/AMD's heterogeneous integration of GPU chiplets and CPU chiplet on TSV interposers.

A. STATSChipPAC's Fan-Out Flip Chip-Embedded Wafer Level Ball Grid Array (eWLB)

At ECTC2013, STATSChipPAC proposed [26, 134] using the fan-out flip chip (FOFC)-eWLB to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 26. It can be seen that the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated.

B. ASE's Fan-Out Wafer-Level Chip-On-Substrate

In 2016, ASE [27] proposed using the FOWLP technology (chip-first and die-down on a temporary wafer carrier and then overmolded by the compression method) to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 27; the technology is called fan-out wafer-level chip-on-substrate (FOCoS). The TSV interposer, wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected to the package substrate using UBM and the C4 bump as shown in Fig. 27.

C. MediaTek's Redistribution Layers by Fan-Out Wafer-Level Packaging

In 2016, MediaTek [135] proposed similar TSV-less interposer RDLs fabricated with FOWLP technology as shown in Fig. 28. Instead of the C4 bump, they used a microbump (Cu pillar + solder cap) to connect the bottom RDL to the 6-2-6 package substrate.

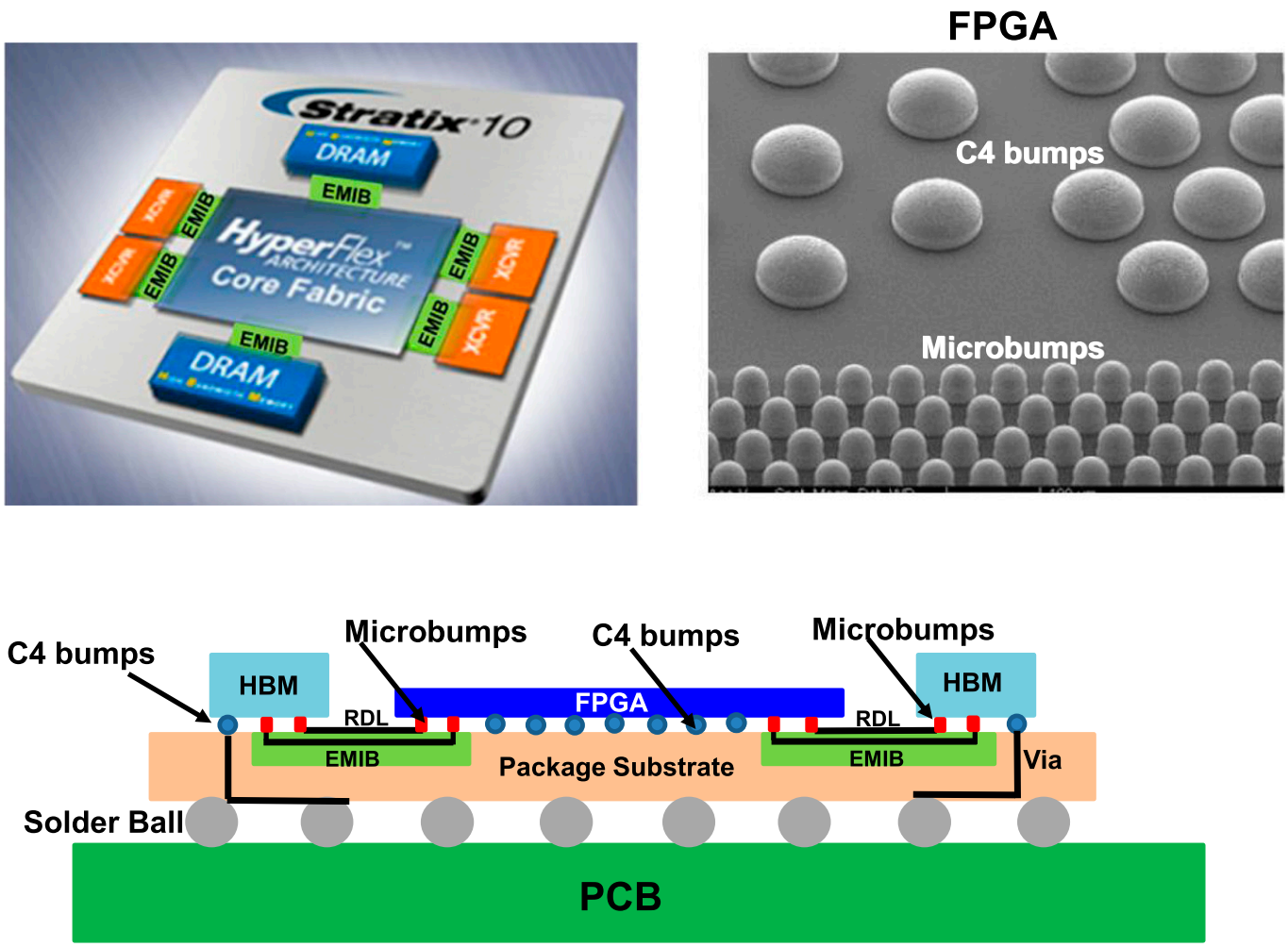


Fig. 18. Heterogeneous integration using Intel's EMIB and FPGA technology.

D. Samsung's Si-Less Redistribution Layer Interposer

Recently, Samsung [32] proposed using chip-last or RDL-first FOWLP to eliminate the TSV interposer as shown in Fig. 29. First of all, they build the RDL on a silicon or glass wafer or panel and in parallel, wafer bumping of the logic and HBM. They then performed fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing. It was followed by epoxy molding compound (EMC) compression molding and then by backgrinding the EMC, remove the carrier, and C4 wafer bumping. It was followed by attaching the whole module on the package substrate. Finally, they performed solder ball mounting and lid attachment.

E. TSMC's Integrated Fan-Out on Substrate

Fig. 30 shows the schematic of TSMC's integrated fan-out on substrate (InFO_oS) [136]. The RDLs are fabricated by TSMC's InFO chip-first and die face-up technology. This InFO_oS is for high-performance applications but not as high as those with CoWoS technology.

Heterogeneous Integration of Antenna-in-Package and Baseband Chipset

Two examples of heterogeneous integration of antenna-in-package (AiP) by FOWLP are briefly mentioned. One is by TSMC and the other is a new proposal.

A. TSMC's Antenna-in-Package with Fan-Out Wafer-Level Packaging

TSMC [137] demonstrated that the InFO_AiP for high-performance and compact 5G millimeter wave system integration is superior than that of solder-bumped flip chip AiP on substrate as shown in Fig. 31. It can be seen that (1) in the 28-GHz frequency range, InFO RDLs transmission loss (.175 dB/mm) is 65% less than that on flip chip substrate trace (.288 db/mm) and (2) in the 38-GHz frequency range, the transmission loss for InFO RDLs (.225 dB/mm) is 53% less than that (.377 dB/mm) on flip chip substrate trace.

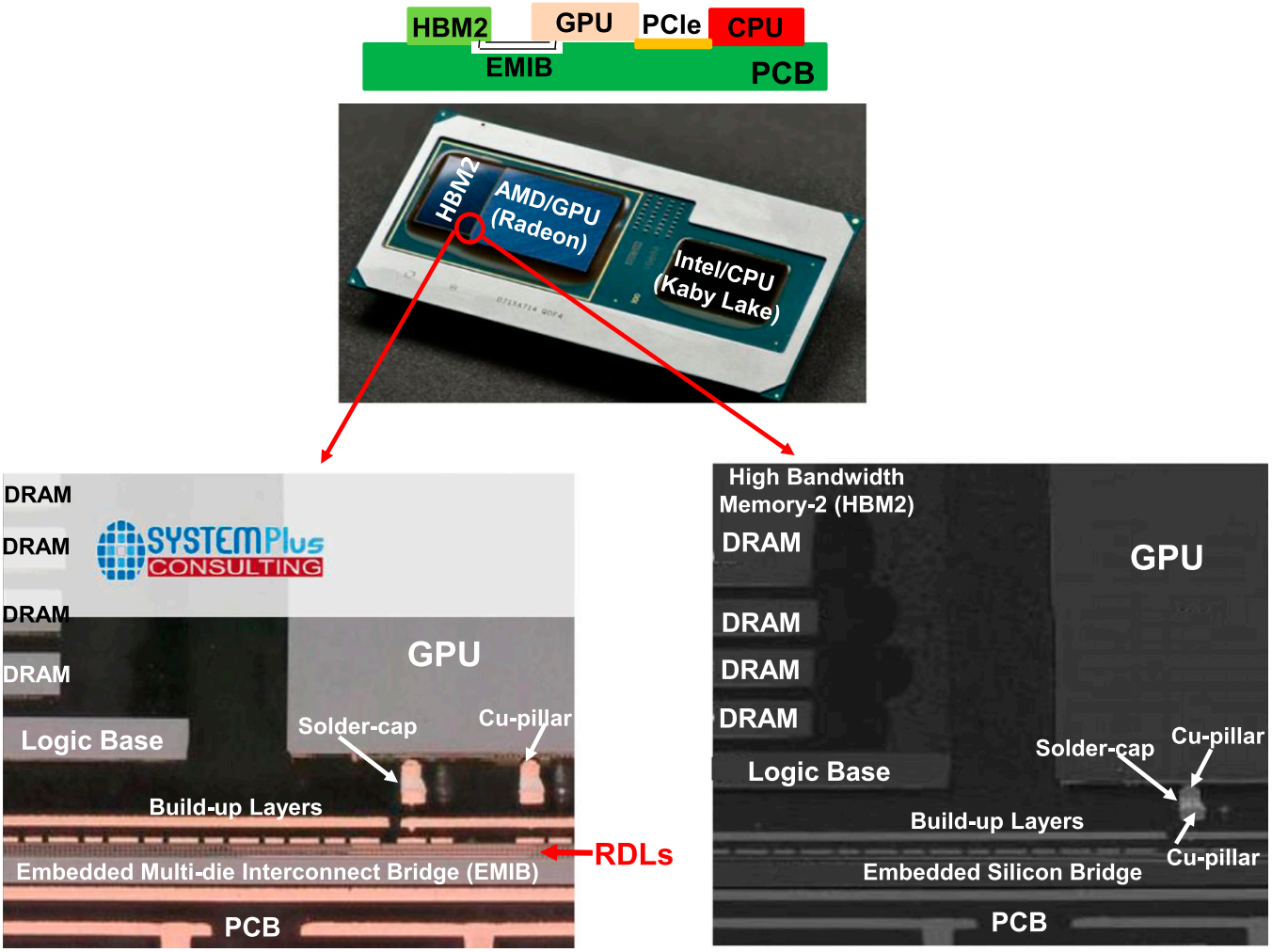


Fig. 19. Heterogeneous integration of Intel's CPU, AMD's GPU, and HBM with EMIB.

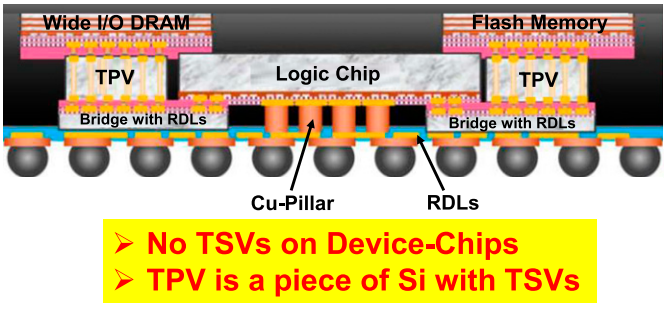


Fig. 20. Imec's heterogeneous integration system with silicon bridges.

B. Heterogeneous Integration of Antenna-in-Package and Baseband Chipset

Fig. 32 schematically shows a heterogeneous integration of AiP and baseband chipset by FOWLP. It can be seen that the RF Chip and the baseband chipset (modem AP and the DRAM) are placed side-by-side with RDLs and coupled with the antenna patches.

Heterogeneous Integration of Package-On-Package

PoP is one of the heterogeneous integrations. A few heterogeneous integrations of PoPs are briefly mentioned in this section.

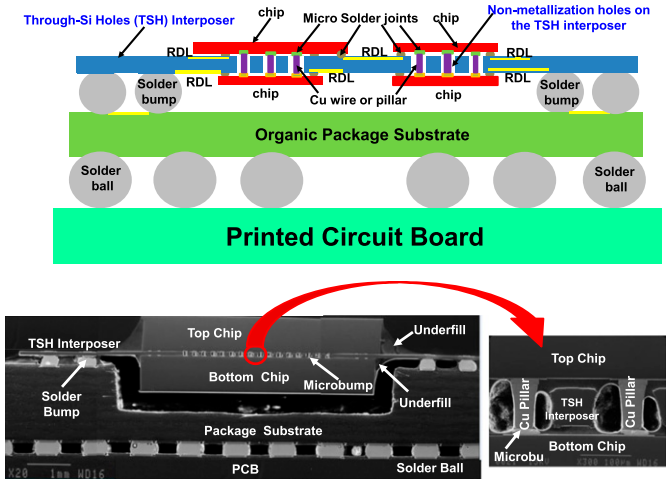


Fig. 21. ITRI's bridge (TSH-interposer) for heterogeneous integrations.

A. Amkor/Qualcomm/Shinko's Package-On-Package

High bonding force thermocompression of the Cu pillar + solder cap bumps with nonconductive paste (TC-NCP) underfill on the substrate was first studied by Amkor [138] and has been

used to assemble Qualcomm's SNAPDRAGON AP for Samsung's Galaxy smartphone for the bottom package of a PoP as shown in Fig. 33. The NCP underfills can be spun on, dispensed by a needle, or vacuum-assisted. The molded core-embedded package substrate was manufactured by Shinko.

B. Apple/TSMC's Package-on-Package for Application Processor A10

Fig. 34 shows the cross section of iPhone 6 Plus. It can be seen that the A9 AP is housed in a PoP format and the solder-bumped flip chip is mass-reflowed on a 2-2-2 organic package substrate and then underfilled. Fig. 35 shows the cross section of iPhone 7. Fig. 35 shows the schematic and SEM images of the cross section of the PoP that houses the Apple A10 AP and mobile dynamic random-access memories (DRAMs) of the iPhone 7/7+. This PoP is fabricated by TSMC with its InFO WLP technology [96-98]. It can be seen from the bottom package that

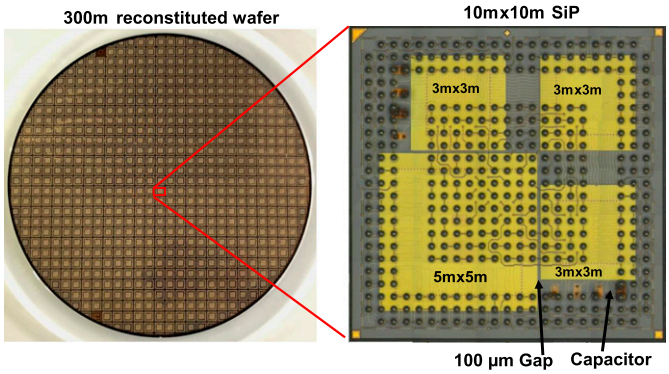


Fig. 22. Heterogeneous integration of four chips by FOWLP.

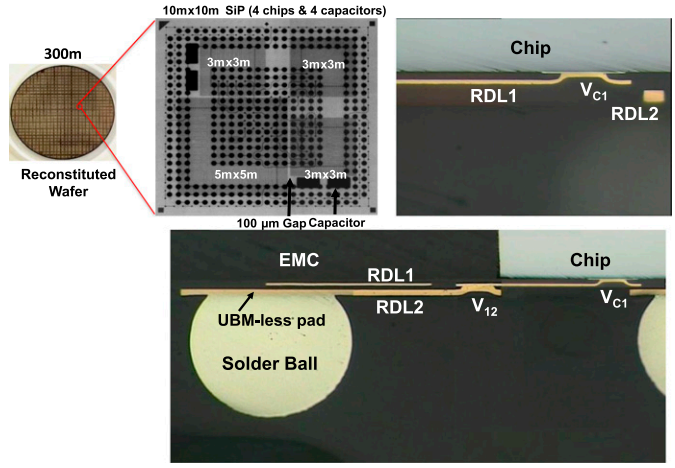


Fig. 23. Cross section of the heterogeneous integration package (by FOWLP) showing the RDLs.

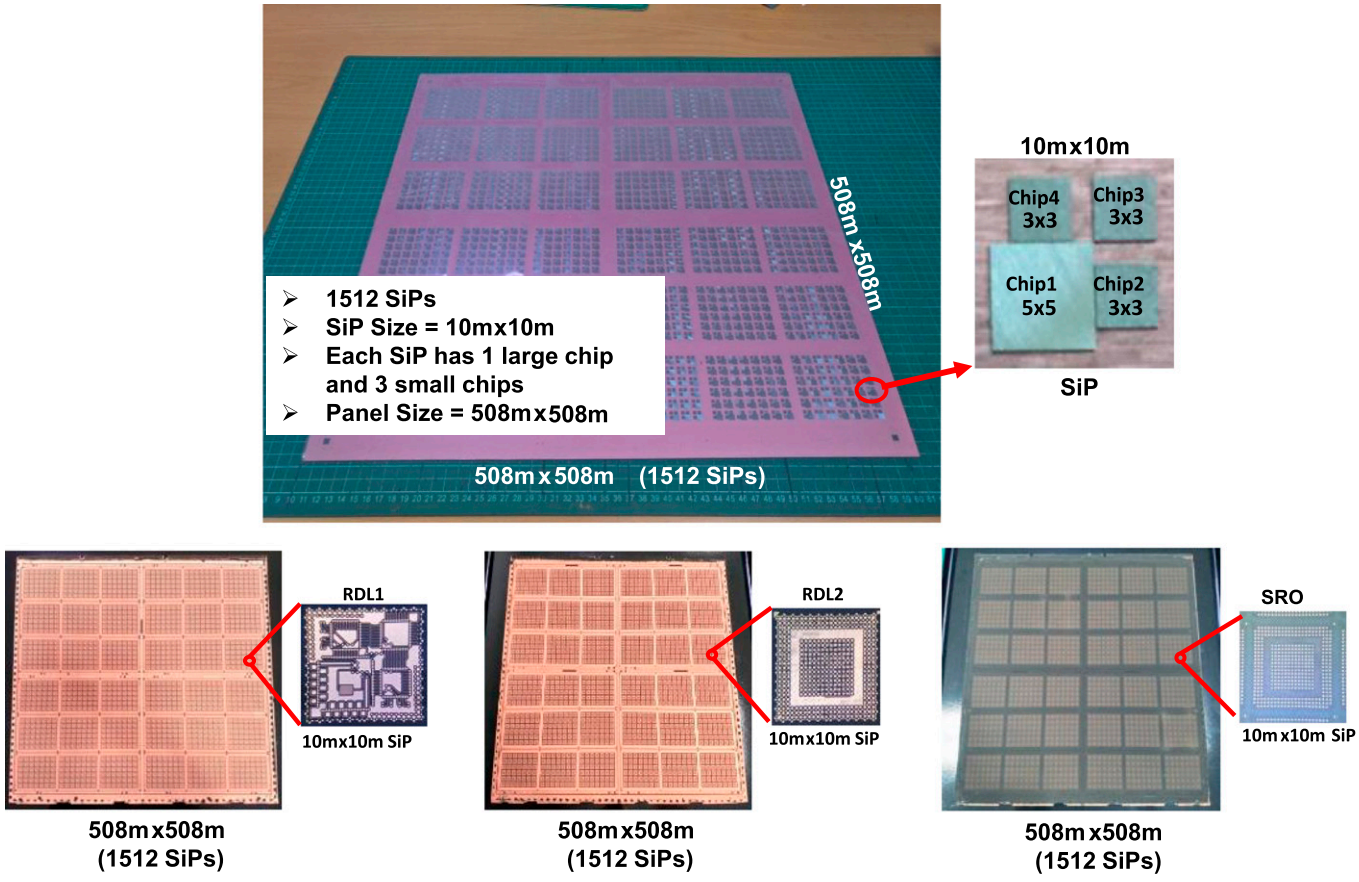


Fig. 24. Heterogeneous integration of four chips by FOPLP.

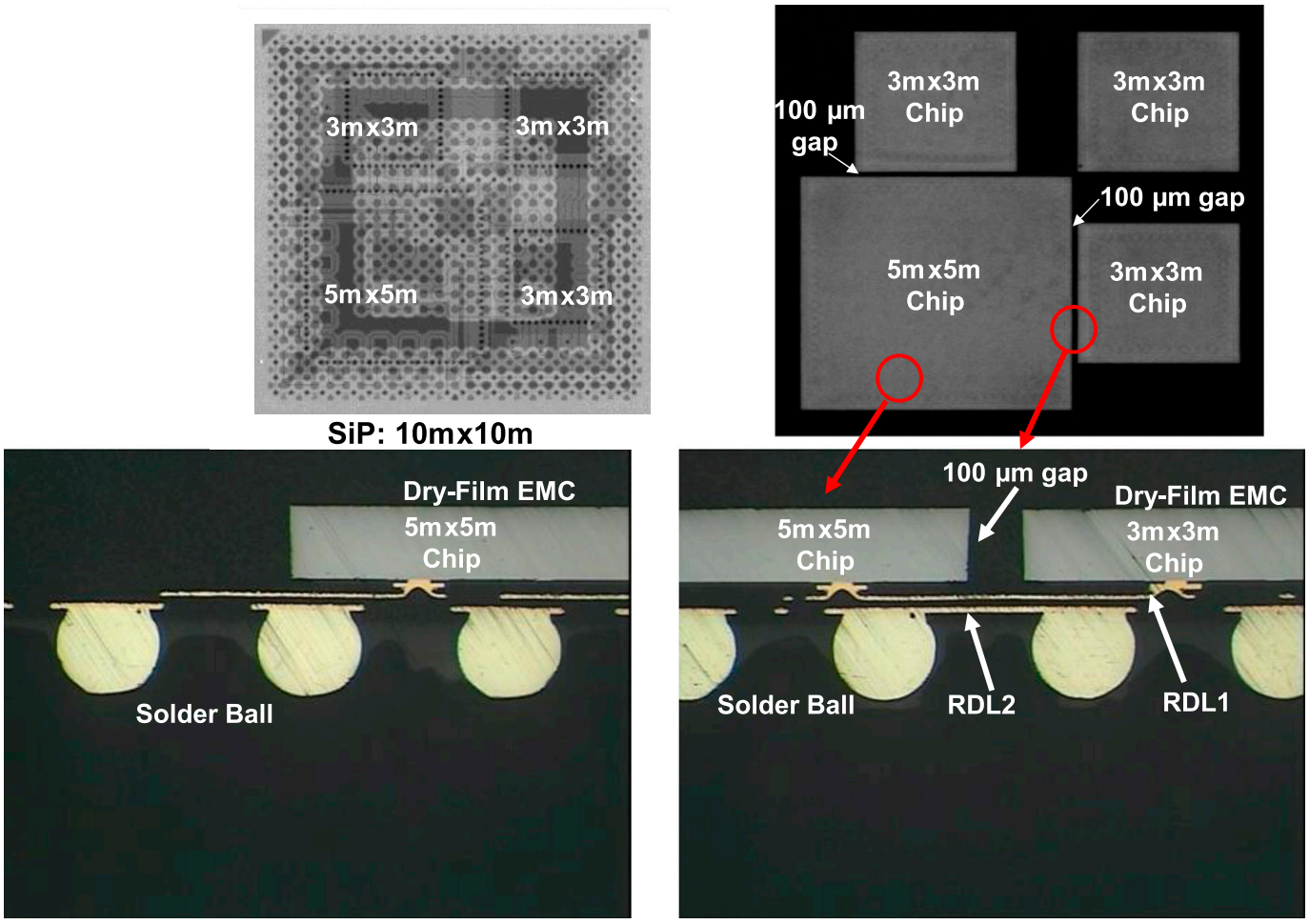


Fig. 25. Cross section of the heterogeneous integration package (by FOPLP) showing the RDLs.

the wafer bumping, fluxing, flip chip assembly, cleaning, underfill dispensing and curing, and build-up package substrate (of the A9 AP shown in Fig. 34) have been eliminated and are replaced by the RDLs (for the A10 AP as shown in Fig. 35). This results in a lower cost, higher performance, and lower profile package.

C. Samsung's Package-on-Package for Smart watch

Fig. 36 shows Samsung's luxury smart watch shipped in July 2018. It is a PoP. It can be seen that the upper package is housing the memory ePoP, which consists of two DRAMs, two NANDs, and one controller. The bottom package is housing the AP and PMIC in the cavity of a three-layer organic substrate by their fan-out panel-level packaging. There are underfills between the upper and bottom packages. The chip size of the AP is about 3.57 × 5.18 mm.

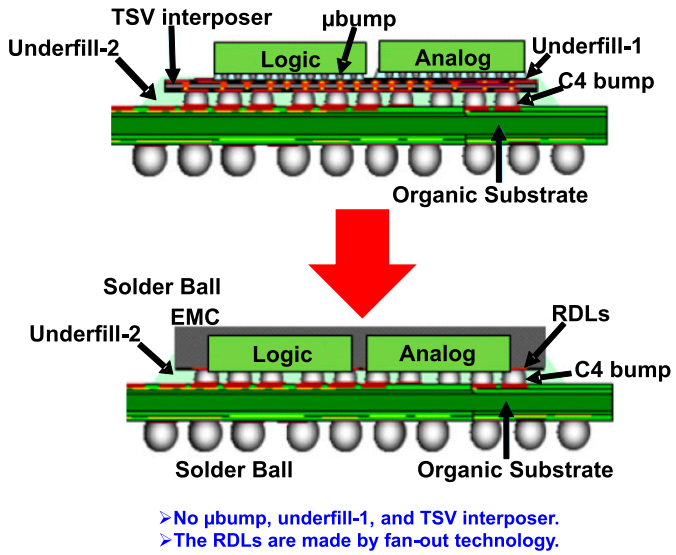


Fig. 26. STATSChipPac's fan-out RDL substrate (FOFC-eWLB).

Heterogeneous Integration of Memory Stacks

A. Heterogeneous Integration of Memory Chips by Wire Bonding

Fig. 37 shows the heterogeneous integration of two memory chips and a logic chip [139]. They are stacked by wire bonding.

B. Heterogeneous Integration of Memory Chips by Low-Temperature Bonding

Fig. 38 shows the heterogeneous integration of memory chips and a logic chip. They are stacked by low-temperature bonding [140].

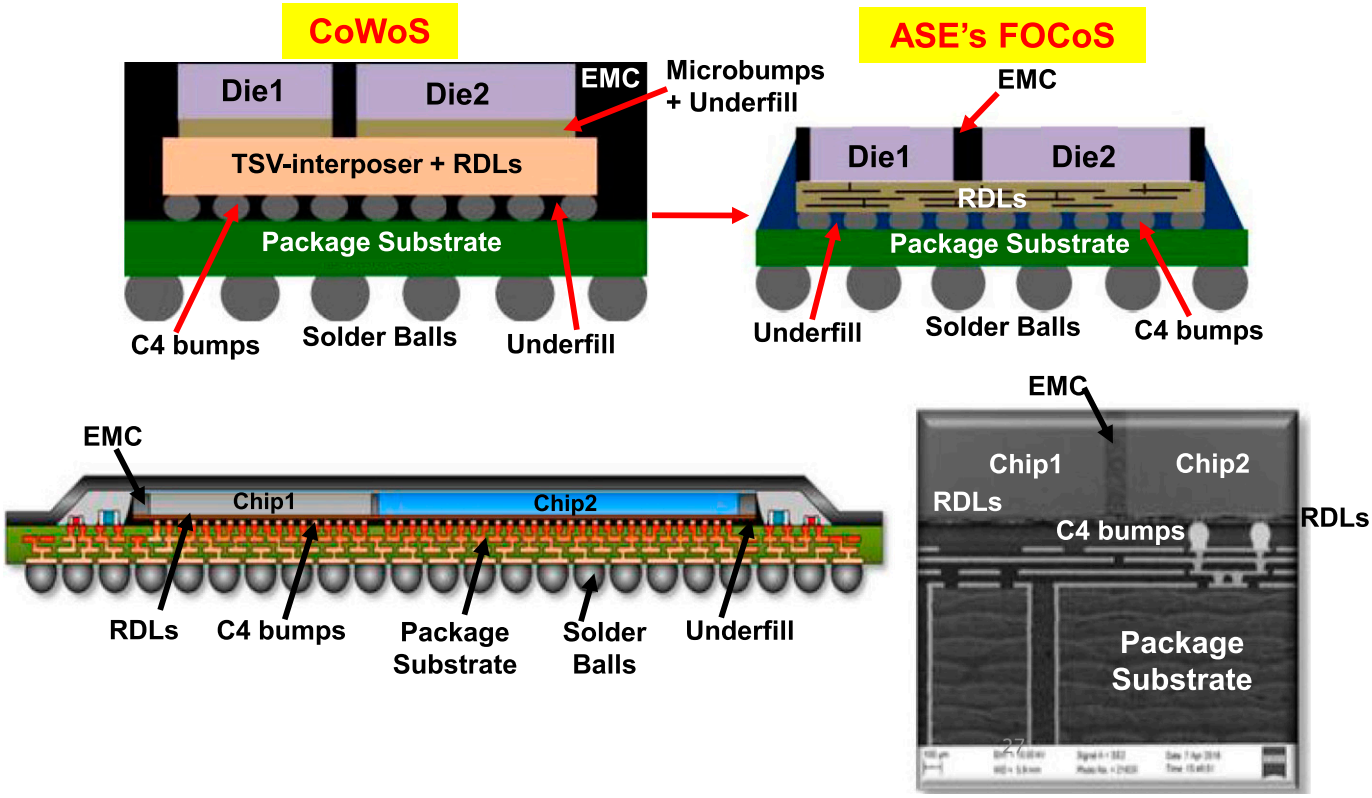


Fig. 27. ASE's FOCoS.

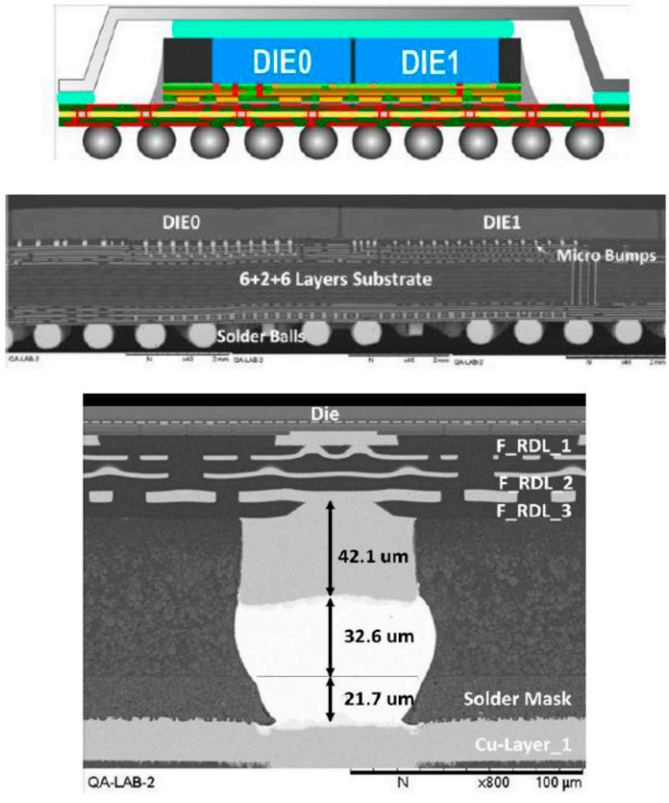


Fig. 28. MediaTek's fan-out RDL substrate.

Heterogeneous Integration of Chip-to-Chip Stacks

A. Intel's Modem Chipset for iPhone XR

Fig. 39 shows the modem chipset by Intel for the second most important chipset of the iPhone XR. It can be seen that the baseband AP is solder-bumped flip chip on a three-layer embedded trace substrate (ETS). The DRAM is die-attached on the backside of the AP and is wire-bonded on the ETS. This is an example of chip-to-chip and back-to-back stack.

B. IME's Chip-to-Chip Stack with Through-Silicon Vias

Fig. 40 shows the heterogeneous integration of chip-to-chip and face-to-face stack [141, 142]. The top chip could be a memory and the bottom chip could be a logic stack with TSVs.

C. IME's Chip-to-Chip Stack Without Through-Silicon Via

Fig. 41 shows the heterogeneous integration of chip-to-chip and face-to-face stack but without TSVs [143, 144]. The connection to the substrate is through the solder ball on the larger (mother) chip.

Heterogeneous Integration of CMOS Image Sensors

A. Heterogeneous Integration of Sony's CMOS Image Sensors

Sony is the first to use Cu-Cu direct hybrid bonding (which bonds the metal pads and dielectric layer on both sides of the

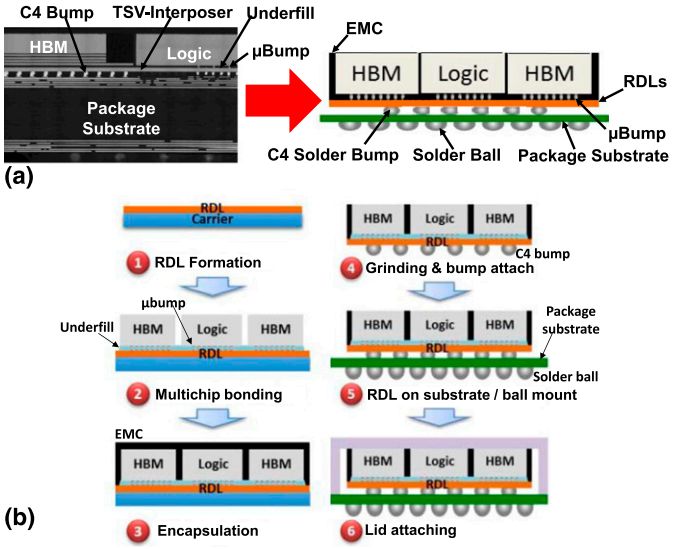


Fig. 29. Samsung's fan-out (chip-last) substrate (Si-less RDL interposer).

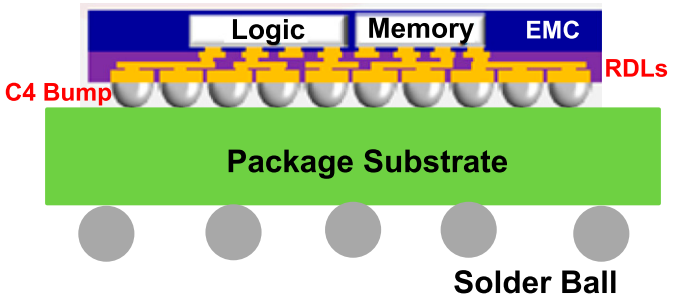


Fig. 30. TSMC's InFO_oS.

wafers at the same time) in HVM. Sony produced the IMX260 backside illuminated (BI)-CIS for the Samsung Galaxy S7, which was shipped in 2016. Electrical test results [145] showed that their robust Cu-Cu direct hybrid bonding achieved remarkable connectivity and reliability. The performance of the image sensor was also appreciable. A cross section of the IMX260 BI-CIS is shown in Fig. 42. It can be seen that unlike in [146] for Sony's ISX014 stacked camera sensor, the TSVs are no longer used and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu-Cu direct bonding. The signals were received from the package substrate with wire bonds to the edges of the processor chip.

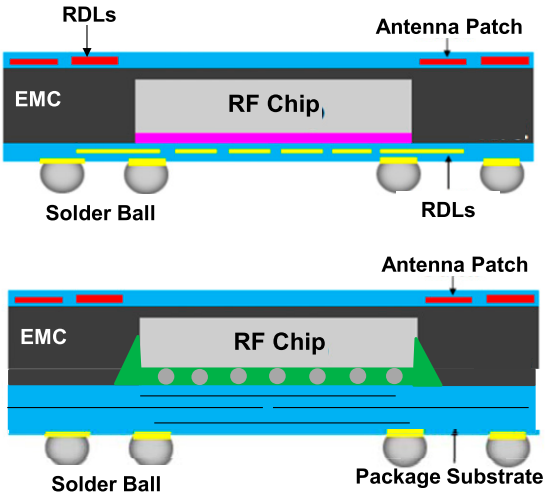
B. Heterogeneous Integration of STMicroelectronics' CMOS Image Sensors

Fig. 43 shows a 3D CIS and IC integration presented in [147]. It consists of the CIS, coprocessor IC, and glass carrier. The I/O count of the CIS is 80 and that of the IC is 164. The size of the CIS and the coprocessor is not the same. The dimensions of the CIS are 5 × 4.4 mm and of the IC are 3.4 × 3.5 mm. The IC and the CIS are bonded face-to-back, as shown in Fig. 43. The interconnects of the CIS and IC are Cu pillar with SnAg solder cap. The TSVs are in the CIS, which are connected to the substrate with solder bump and RDLs. Fig. 43 shows the 3D prototypes during the assembly process (balling first): mounted IC coprocessors and untreated sites.

Heterogeneous Integration of Light-Emitting Diode

A. Heterogeneous Integration of The Hong Kong University of Science and Technology (HKUST's) Light-Emitting Diode

Fig. 44 shows the top view and cross section view of an Si-substrate with cavity for phosphor printing and Cu-filled



THE TRANSMISSION LOSS FOR RDL AND SUBSTRATE TRACE AT 28 AND 38GHZ

Frequency	InFO RDLs	Substrate Trace
28GHz	0.175dB/m	0.288dB/m
38GHz	0.225dB/m	0.377dB/m

Fig. 31. TSMC's AiP with InFO and compared with flip chip-on-substrate.

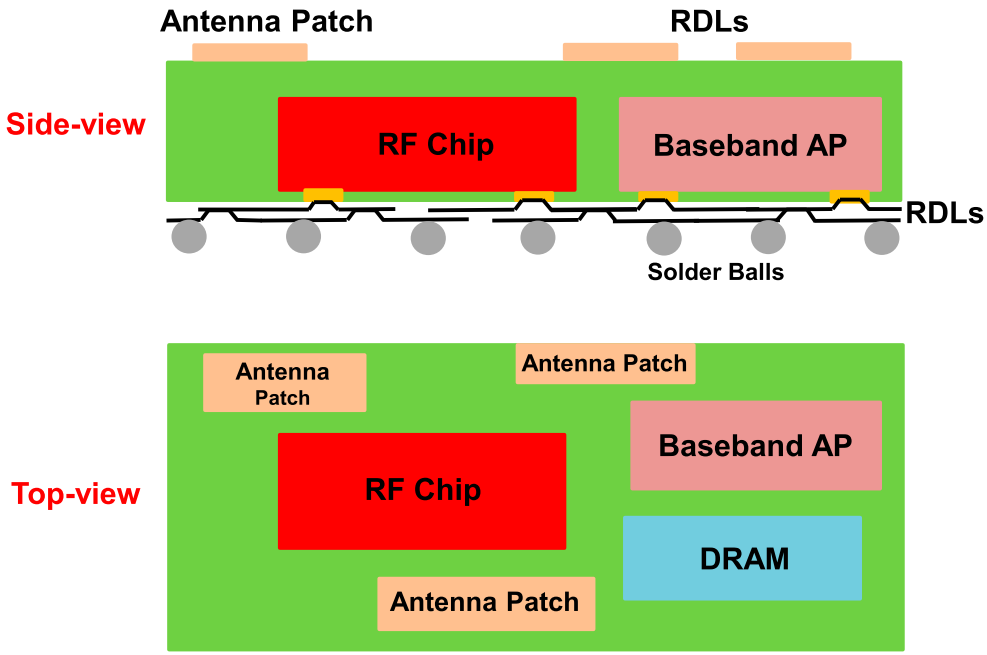


Fig. 32. A proposal on heterogeneous integration of RF chip, baseband AP, DRAM, and AiP.

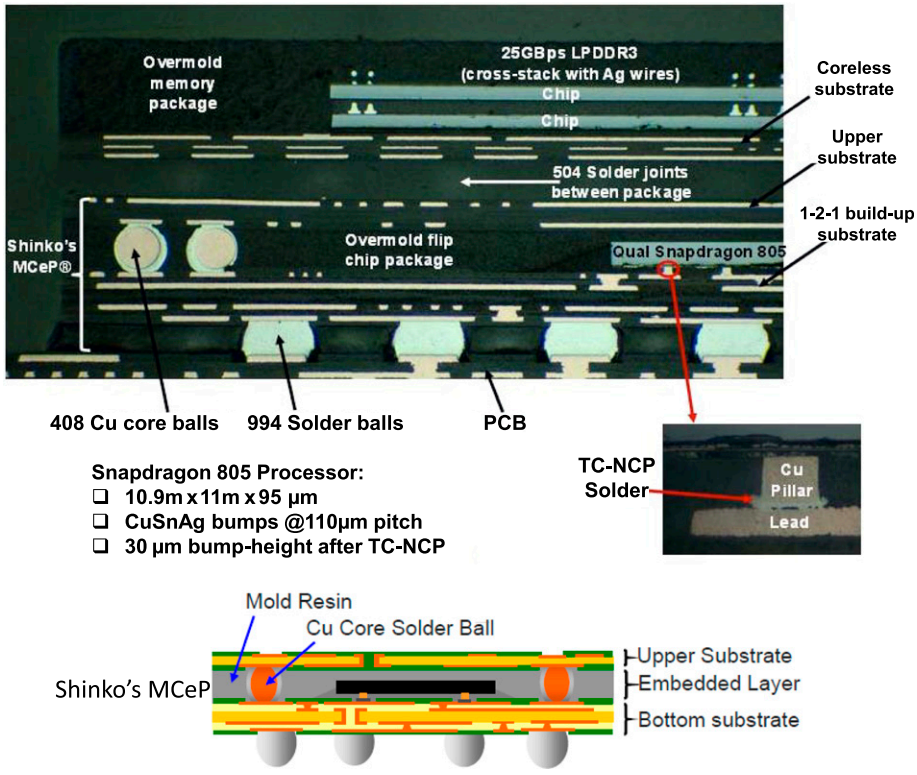


Fig. 33. Amkor/Qualcomm/Shenko's PoP with TC-NCF.

TSVs for interconnection LED [148, 149]. It can be seen that the Si-substrate is about 400-µm-thick with 3-µm-thick low temperature oxide on both sides. The dimensions of the cavity are 1.3 × 1.3 × .22 mm. The diameter of the TSV is 100 µm and is filled with Cu. The exposed tip of the Cu TSV is 30 µm and plated with solder. Figs. 44a-c show the images, respectively, of the top view and cross sectional view of the LED package. The Si-substrate, the RDL, the cavity, and the TSV tips with solder bumps (before LED mounting) can be clearly seen.

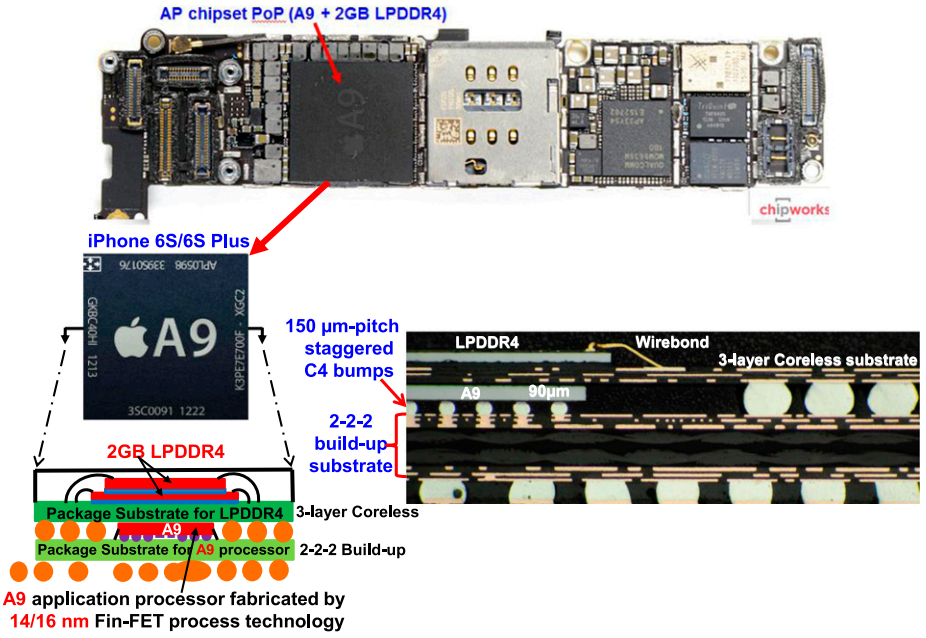


Fig. 34. Apple's PoP with solder-bumped flip chip-on-substrate for the AP.

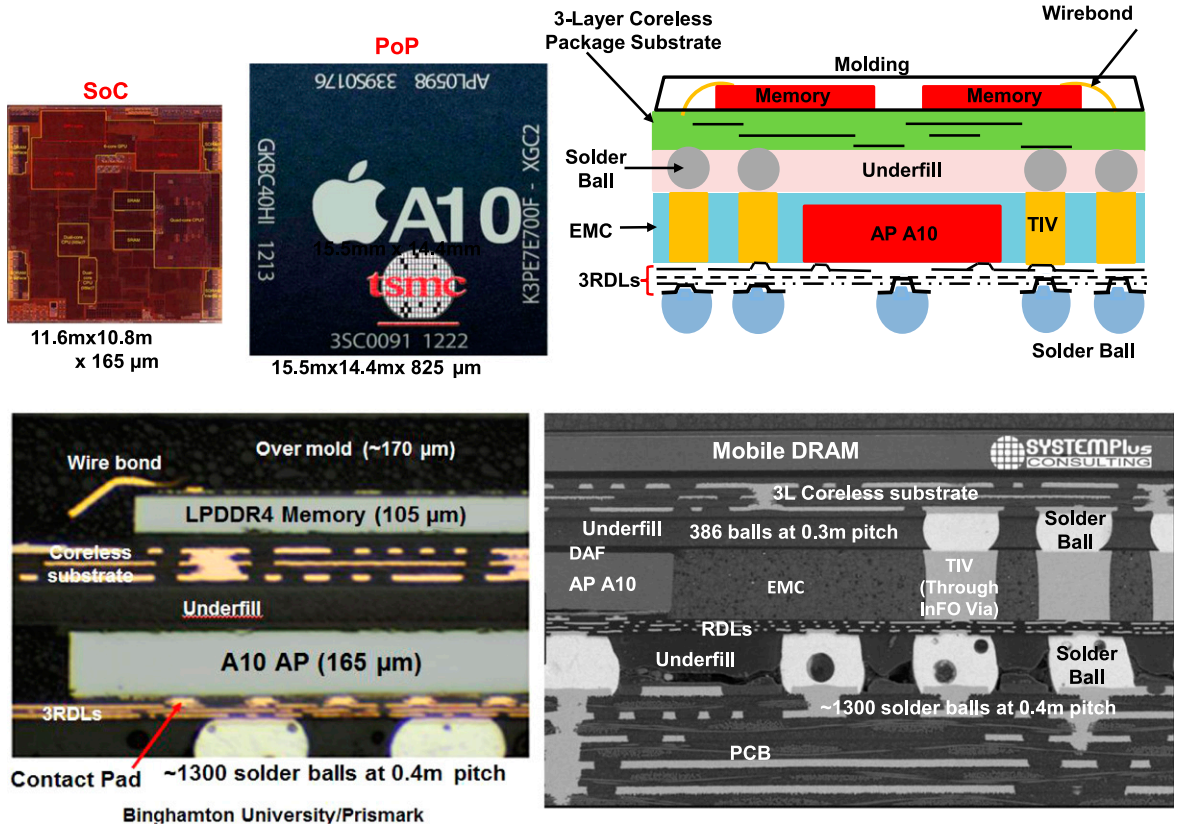


Fig. 35. Apple/TSMC's PoP with InFO for the AP.

B. Heterogeneous Integration of JiangYin ChangDian Advanced Packaging (JCAP's) Light-Emitting Diode

Fig. 45 schematically shows a wafer-level packaging with LED devices in the cavities of an Si-substrate [150, 151]. It can be seen that the Si-substrate has cavities on its top side to house the LED devices and TSVs to connect the LEDs to the RDLs on its bottom side. The Si-substrate is covered by a glass with yellow phosphor. Fig. 45 shows the SEM images of the cross

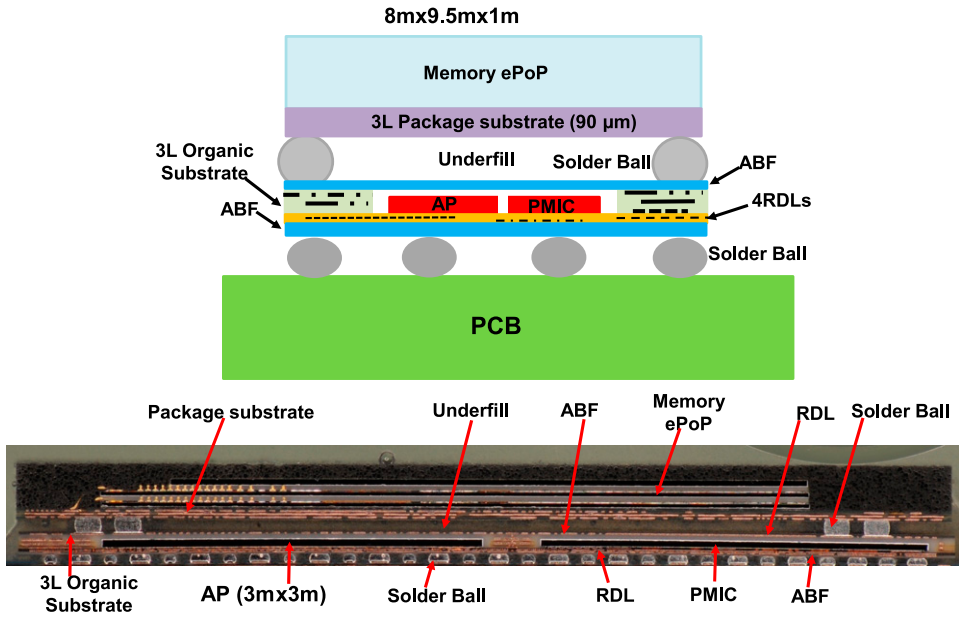
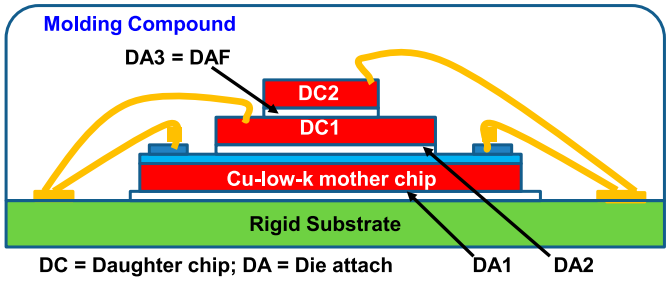


Fig. 36. Samsung's PoP for the luxury smart watch. The AP and PMIC are packaged with Samsung's FOPLP.



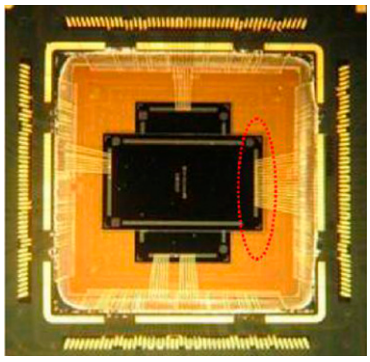


Fig. 37. IME's heterogeneous integration of three chips with wire bonding.

section of the LED package without phosphor. It can be seen that (1) the LED device is attached on the bottom of the cavity of the Si-substrate, (2) the glass is bonded on the top of the Si-substrate, (3) the LED pads are connected to the RDL through the TSV with contactor size of about 20 μm, and (4) the encapsulation separates the Si-substrate from the RDL, which prevents electrical shortage between the cathode and the anode.

Heterogeneous Integration of Microelectro-Mechanical Systems

A. Heterogeneous Integration of IME's Microelectro-Mechanical Systems

Fig. 46 shows the cross section and bird-view of the wafer-level packaging of a RF-MEMS device [152, 153]. It consists of the MEMS wafer (RF-MEMS device, high-resistivity silicon [HR-Si] substrate with RDLs, and AuSn solder for sealing ring and bonding pads) and the cap wafer (cap with a cavity, TSVs, and RDLs, and the solder bump). It is a 2.25D MEMS and IC integration. Main objective of [152, 153] is to study the insertion loss of RF-MEMS wafer during packaging with TSV cap wafer. Two different types of coplanar waveguide (CPW) structures (1-mm CPW and 2-mm CPW), as shown in Fig. 46, are designed and fabricated.

B. Heterogeneous Integration of Imec's Microelectro-Mechanical Systems

Fig. 47 shows the zero-level packaging for RF-MEMS device [154, 155]. It consists of the RF-MEMS, HR-Si substrate with RDLs, and Cu-Sn-Cu for sealing ring and bonding pads, the HR-Si cap with TSVs and RDLs, and the solder bump. Again, it is a 2.25D MEMS package. One of the main objectives of [154, 155] is to study the bonding characteristics (sealing ring and interconnect bumps) of the MEMS wafer and the cap wafer.

C. Heterogeneous Integration of Institut für Zuverlässigkeit und Mikrointegration (IZM's)Microelectro-Mechanical Systems

Fig. 48 schematically shows a MEMS package based on interposer wafer [156]. It can be seen that the MEMS device

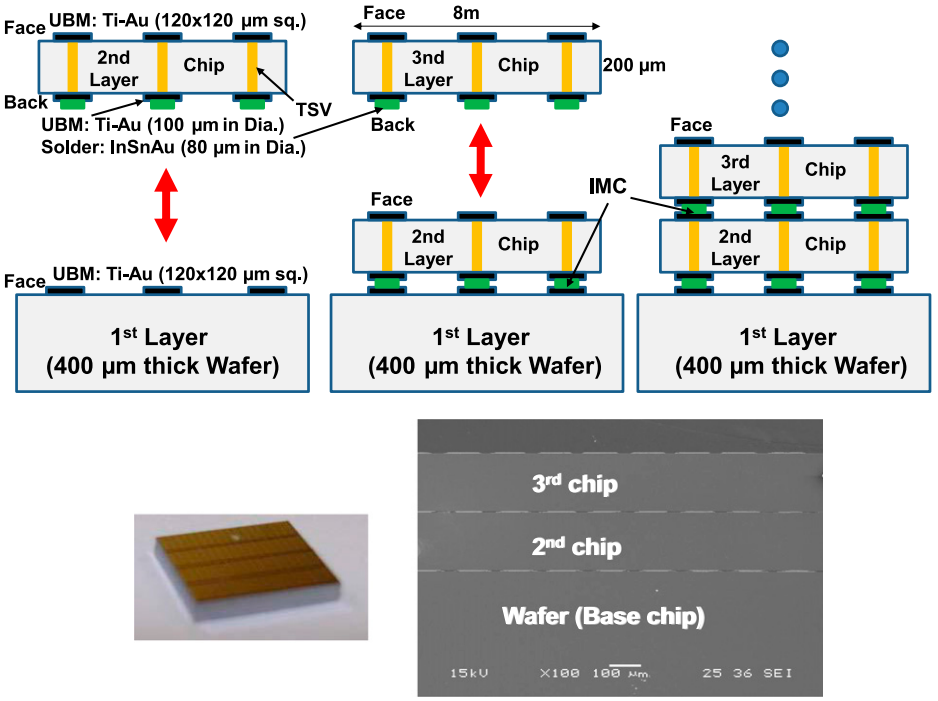


Fig. 38. IME's heterogeneous integration of a few chips with low-temperature bonding.

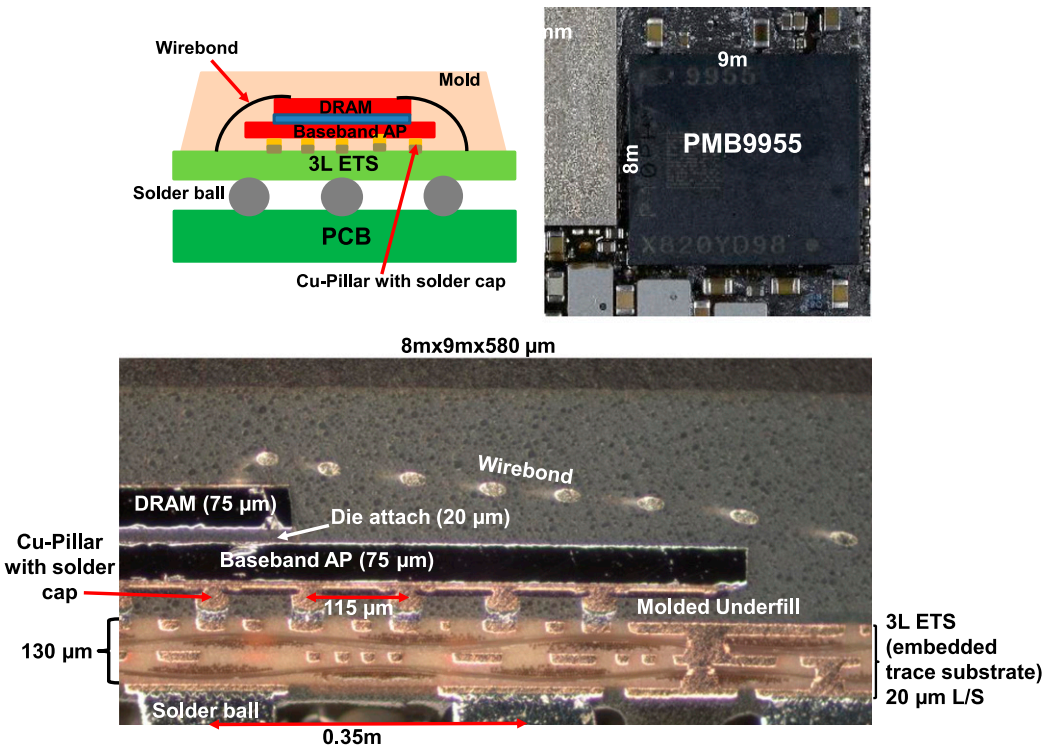


Fig. 39. Intel's heterogeneous integration of the modem chipset (baseband AP and DRAM).

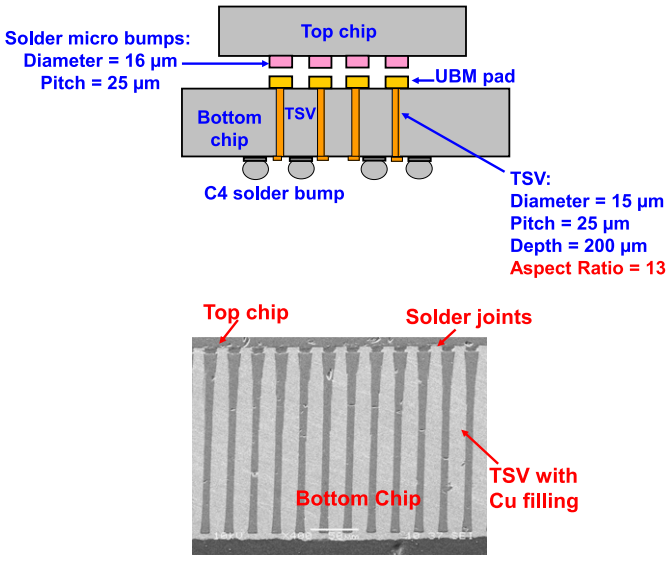


Fig. 40. IME's face-to-face and chip-to-chip (with TSV) heterogeneous integration.

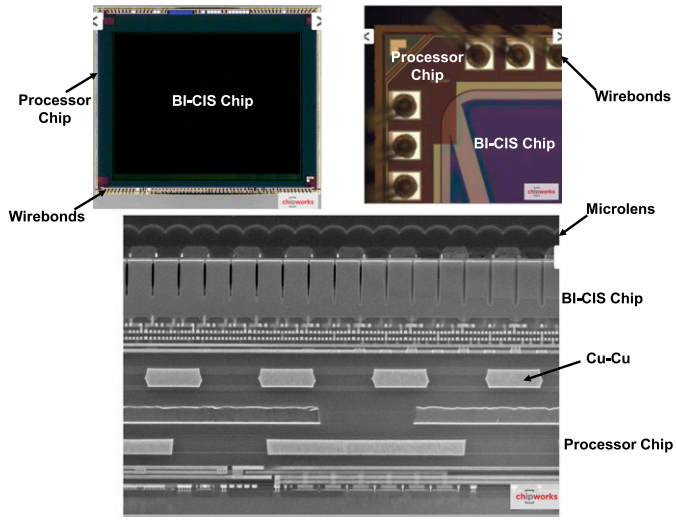


Fig. 42. Cross section image of Sony's CIS heterogeneous integration by Cu-Cu hybrid bonding.

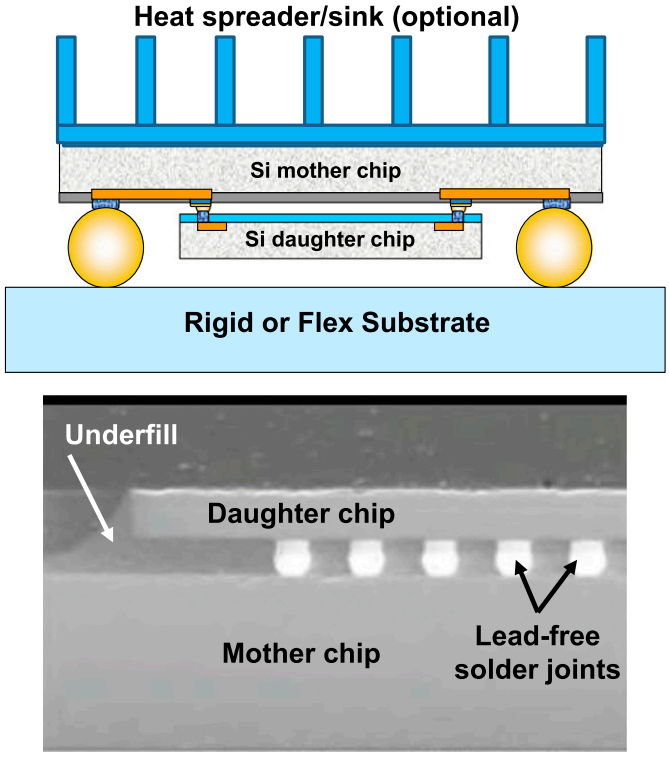


Fig. 41. IME's chip-to-chip and face-to-face (without TSV) heterogeneous integration.

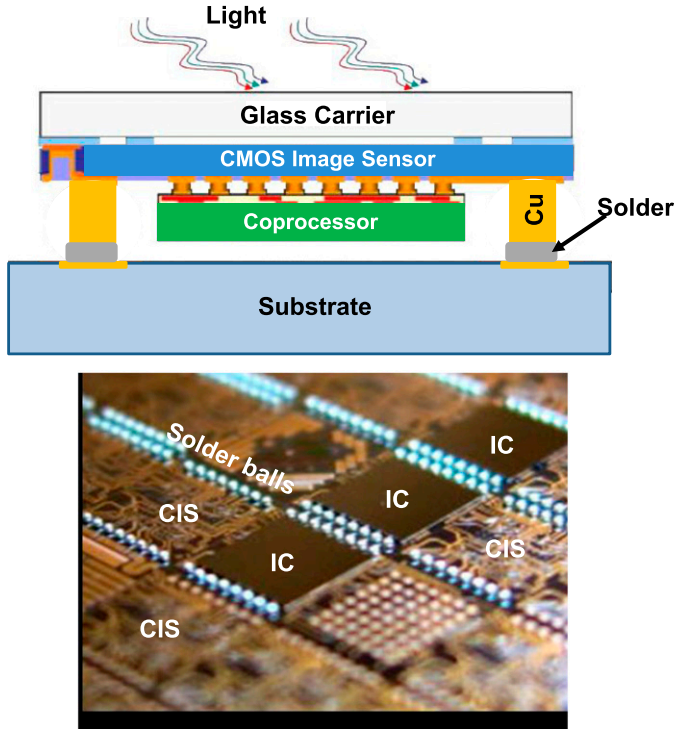


Fig. 43. STMicroelectronics' (face-to-back) CIS heterogeneous integration.

is attached to a Si-interposer wafer with Cu-filled TSVs and RDLs and is hermetic-sealed with a cap wafer with cavity. This is a 2.5D MEMS and IC integration. A typical cross section image of the final assembly is shown in Fig. 48. It can be seen that all the key elements of the MEMS package, such as the MEMS device, Si-interposer, TSV, microbump, and sealing ring, are in proper position.

D. Heterogeneous Integration of Discera's Microelectro-Mechanical Systems

Discera produced the MEMS resonator with TSVs shown in Fig. 49. It can be seen that (1) the MEMS resonator is right on top of the ASIC, (2) the connections between the ASIC and the

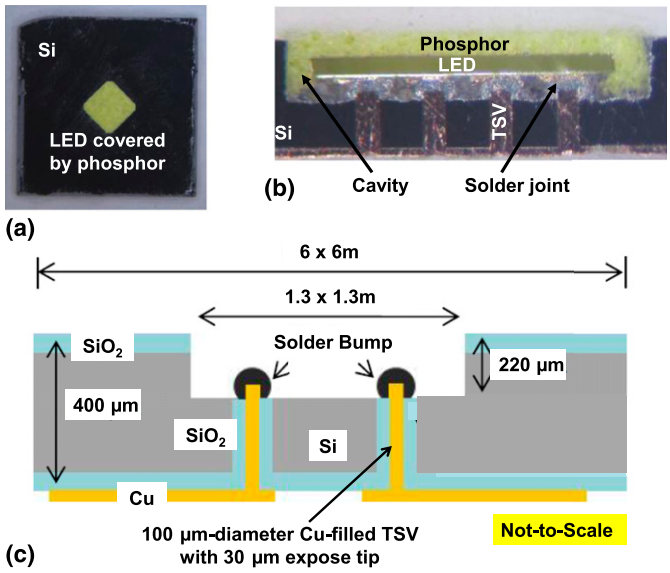


Fig. 44. HKUST's heterogeneous integration of LED on TSV interposer.

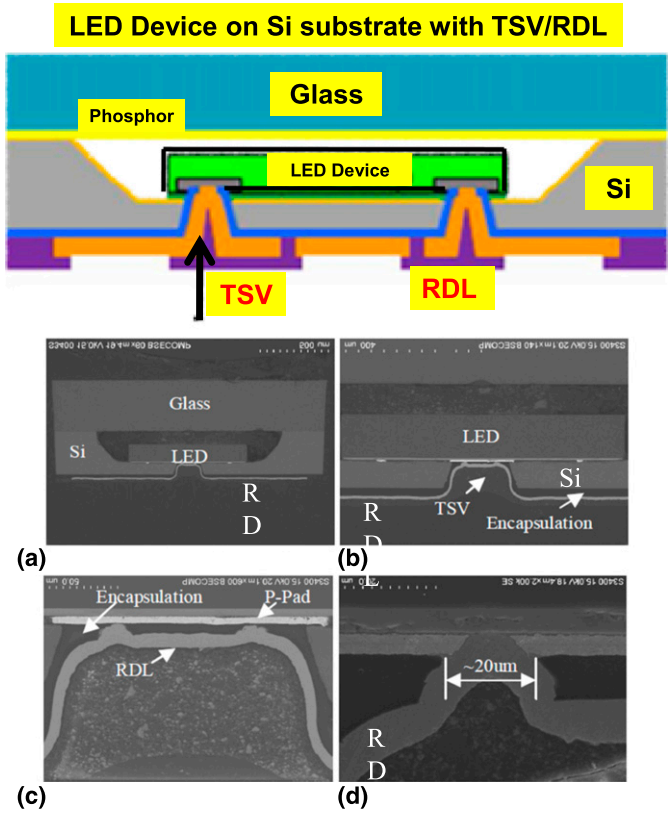


Fig. 45. JCAP's heterogeneous integration LED on TSV interposer.

TSV are by wirebonds, and (3) the TSVs are in the Si-substrate of the MEMS resonator.

E. Heterogeneous Integration of Analog Devices' Microelectro-Mechanical Systems

Fig. 50 shows the heterogeneous integration of the MEMS device and the ASIC provided by Analog Devices. It is

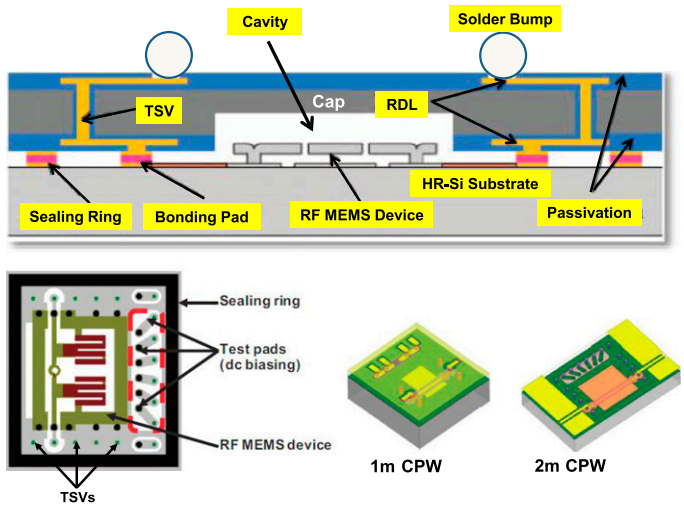


Fig. 46. IME's 3D MEMS packaging with lateral electrical feed-through.

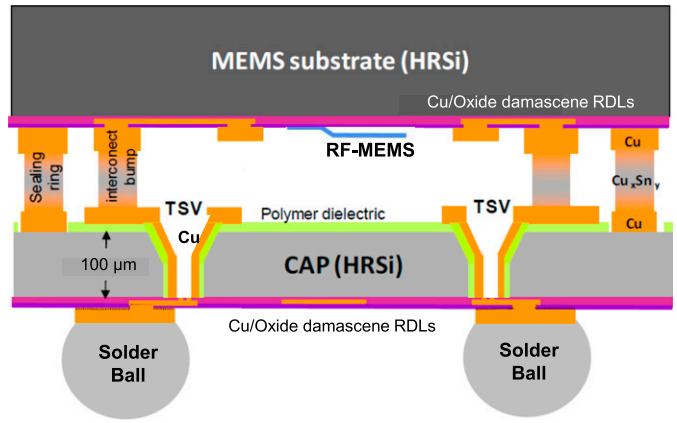


Fig. 47. Imec's heterogeneous integration of MEMS and cap with TSV.

assembled by chip (MEMS) to (ASIC) wafer bonding. The interconnection between the MEMS and the ASIC is by RDLs and TSVs.

F. Heterogeneous Integration of IME's Microelectro-Mechanical Systems

Fig. 51 shows the heterogeneous integration of the MEMS device on ASIC and is hermetic sealed by a silicon cap [157]. It is assembled by chip (MEMS) to (ASIC) wafer bonding and (cap) wafer to (ASIC with MEMS) wafer bonding.

G. Heterogeneous Integration of Avago's Microelectro-Mechanical Systems

Avago produced the film bulk acoustic resonator (FBAR) MEMS filter, ACMD-7612: UMTS Band I Duplexer shown in Fig. 52 [158, 159]. It can be seen that (1) there are circuits in the cap, (2) TSVs are in the Tx (transceiver) chip and the Rx (receiver) chip, and (3) the sidewall of the TSVs is metallized and the TSVs are not filled.

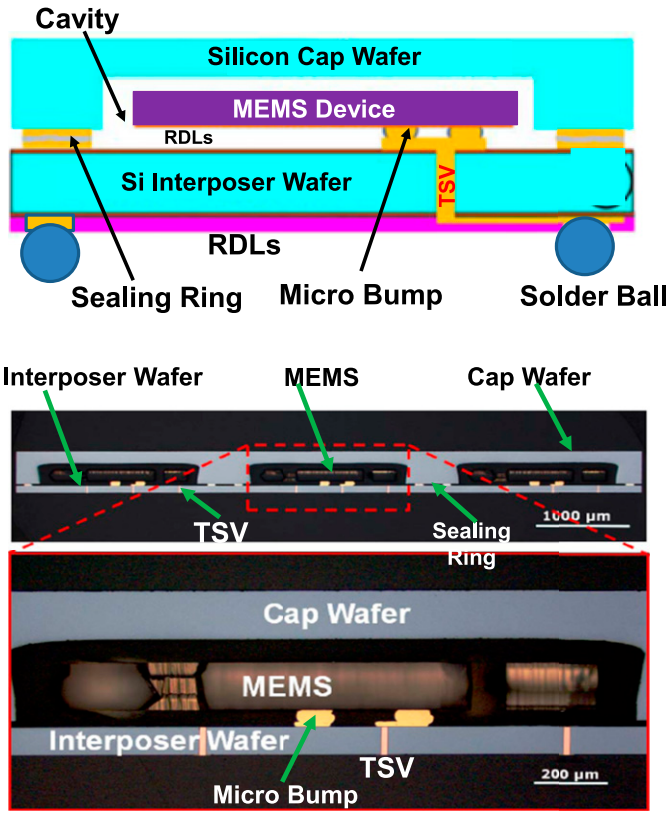


Fig. 48. IZM's heterogeneous integration of MEMS on TSV interposer.

Heterogeneous Integration of Vertical-Cavity Surface-Emitting Laser

A. Heterogeneous Integration of IME's Vertical-Cavity Surface-Emitting Laser

Fig. 53 shows a single-channel optoelectrical circuit board (OECB) with embedded waveguide using traditional PCB manufacturing process [160-165]. The OECB is made up of four electrical layers and one optical layer embedded below a 60-μm-thick BT substrate. Two optical vias with 100 μm diameter are formed to guide the optical beam from VCSEL to the 45° mirror coupler. Likewise, optical beam exiting the waveguide is diverted from the 45° mirror coupler through the optical via and received by the photodetector. A 10-cm-long embedded polymer waveguide consists of a 70 × 70-μm core and a 15-μm-thick top and bottom cladding. Two 45° mirror couplers are formed at both corners of the waveguide by using 90° diamond dicing blade. These mirrors convert optical beam emitted from VCSEL in the vertical path to the planar direction and into the waveguide.

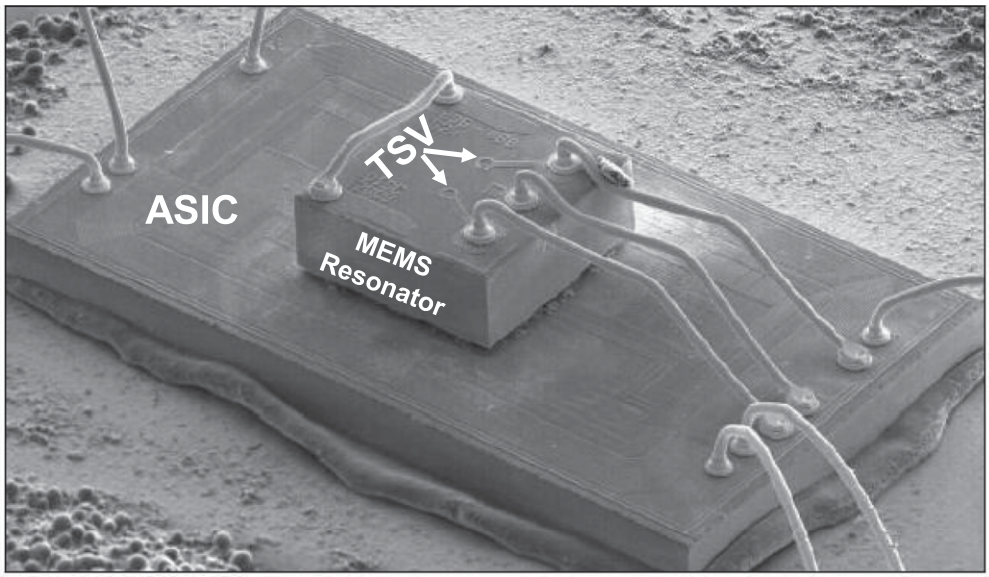
B. Heterogeneous Integration of HKUST's Vertical-Cavity Surface-Emitting Laser

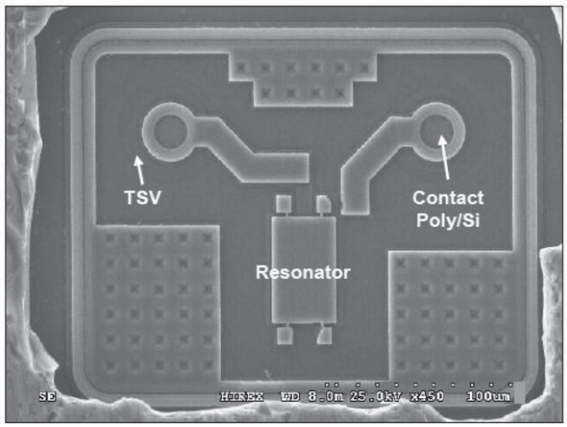
Fig. 54 shows an embedded hybrid 3D heterogeneous integration for optoelectronic interconnects [166-168]. It can be seen that the VCSEL is flip chip bumped with any materials on the VCSEL driver chip with TSV, which is solder-bumped flip chip on the serializer chip. Larger bumps with any materials are mounted on the serializer chip while it is in a wafer format. After dicing the 3D hybrid IC chipset, it is placed on the PCB (or substrate) on top of the polymer waveguide. Special encapsulant (underfill) such as the transparent polymer may be needed to protect the chipset. If it is needed, a heat slug or any conductive material can be attached to the backside of the serializer chip by a thermal interface material (TIM). Again, if it is needed, a heat spreader can be attached to the top side of the heat slug with a TIM. Similarly, the photodetector chip is solder-bumped flip chip on the transimpedance amplifier (TIA) chip, which is then solder-bumped flip chip on the deserializer chip. The thermal management and encapsulant techniques are the same as those of the VCSEL chipset.

Summary and Recommendations

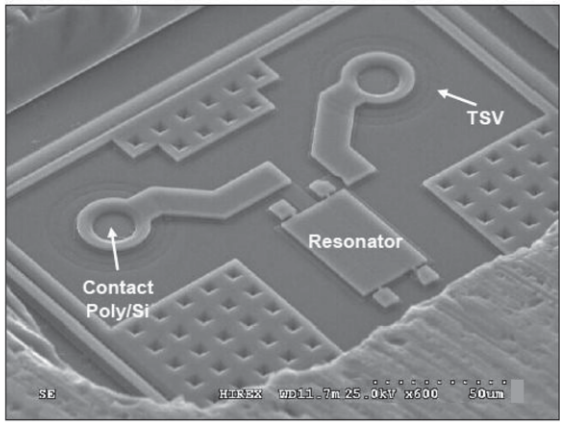
Some important results and recommendations are as follows:

1. Heterogeneous integration is defined as using packaging technology to integrate dissimilar chips, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless houses foundries, wafer sizes, feature sizes and companies into a system or subsystem on different substrates or stand alone.
2. Heterogeneous integrations is classified as (1) heterogeneous integrations on organic substrates, (2) heterogeneous integrations on silicon substrates (TSV interposers), (3) heterogeneous integrations on silicon substrates (bridges), (4) heterogeneous integrations on fan-out RDL substrates, and (5) heterogeneous integrations on ceramic substrates.
3. Seventy-five percent of the heterogeneous integrations will be on organic substrates (actually most are SiPs). Twenty-five percent of the heterogeneous integration will be on other substrates such as silicon (TSV interposers), silicon (bridges), fan-out RDLs, and ceramic.
   Figure 55 shows the application ranges (size and pin-count) of heterogeneous integrations on various substrates. It can be seen that: (1) the heterogeneous integrations on silicon substrates (TSV-interposers) can have the largest number of pin-counts (>100,000) but the largest substrate size is = 1200mm^2, (2) the heterogeneous integrations on silicon substrates (bridges) can have the number of pin-count of 4000 and the substrate size ≤ 1200mm^2, (3) the heterogeneous integrations on fan-out (chip-first) substrates can have the number of pin-count of 2500 and the substrate size ≤ 625mm^2, (4) the heterogeneous integrations on fan-out (chip-last) substrates can have the number of pin-count of 5000 and the substrate size ≤ 1400mm^2, and (5) the heterogeneous integrations on organic substrates can have the number of pin-count up to 6000 and the substrate size as large as 3000mm^2.
   How to select different heterogeneous integrations? It depends on applications. The most important indicator (selection criterion) is the metal line width and spacing of the RDLs of the heterogeneous integrations. For example, semiconductors driven by AI for HPC applications, the metal line width and spacing of the RDLs of the heterogeneous integrations must be ultra-fine (< 2μm or down to submicron). In this case, silicon substrate such as the TSV-interposer is





Resonator with connections – SEM view



Resonator with connections – Tilted SEM view

Fig. 49. Discera's heterogeneous integration of MEMS with TSV on ASIC.

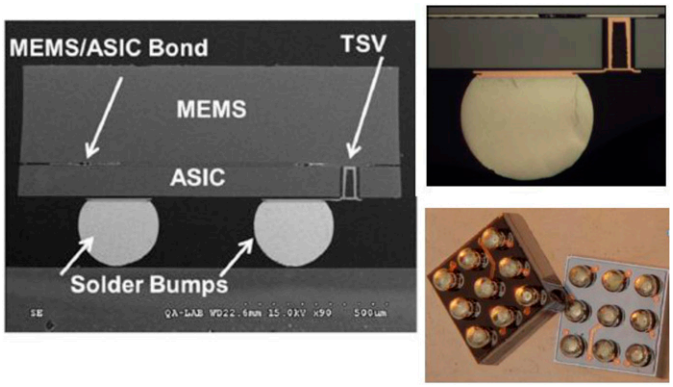
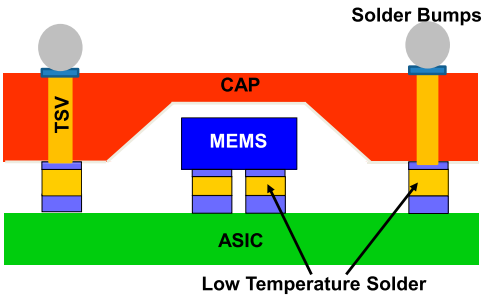
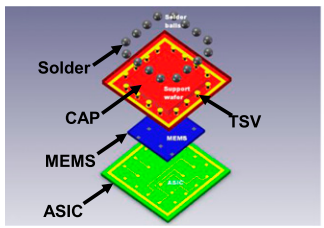


Fig. 50. Analog devices' heterogeneous integration of MEMS on ASIC with TSV.





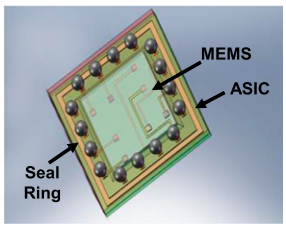


Fig. 51. IME's heterogeneous integration of VCSEL and photodetector with polymer waveguide on PCB.

needed. The silicon substrate with a bridge made by PECVD and Cu-damascene + CMP can also do the job. On the other hand, semiconductors driven by 5G for mobile applications, the metal line width and spacing of the RDLs of the heterogeneous integrations are in the 10μm range. In this case, a

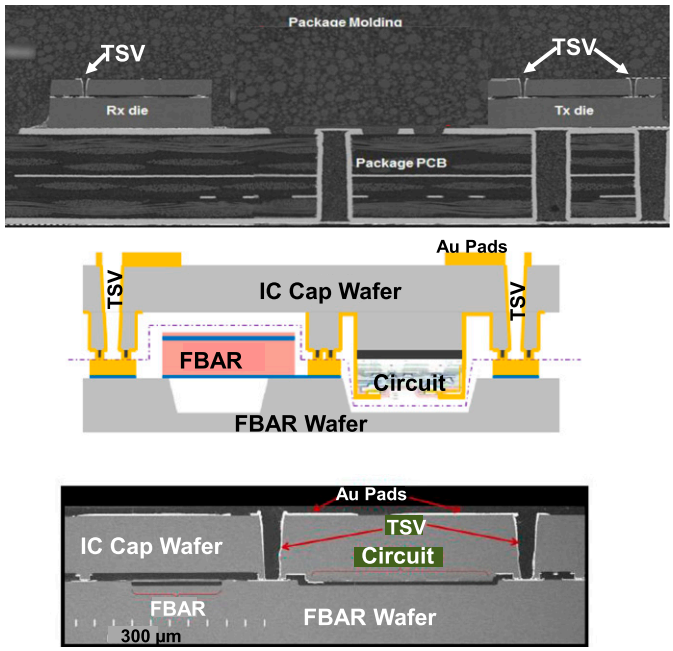


Fig. 52. Images of the FBAR hermetic package.

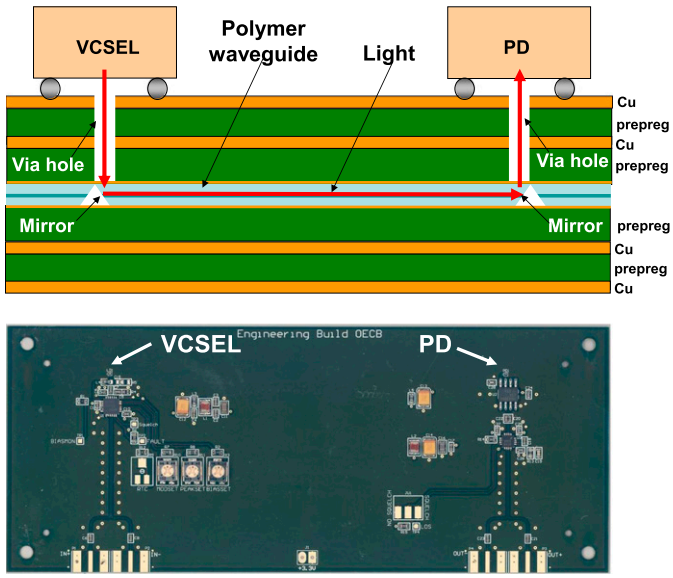


Fig. 53. IME's embedded heterogeneous integration of VCSEL and photodetector with polymer waveguide on PCB.

build-up organic substrate for connecting the RF-chip and the modem-chip is adequate, but on fan-out substrate is even better.

4. Examples for heterogeneous integrations on organic substrates, silicon substrates (TSV interposers), silicon substrates (bridges), and fan-out RDL substrates have been provided.
5. Heterogeneous integration of chip-to-chip, face-to-face, face-to-back, memory stacks, PoP, AiP, LED, CIS, MEMS, VCSEL, etc. have also been briefly mentioned.
6. To promote/popularize the heterogeneous integrations, standards are necessary! The DARPA program called CHIPS is heading into the right direction.

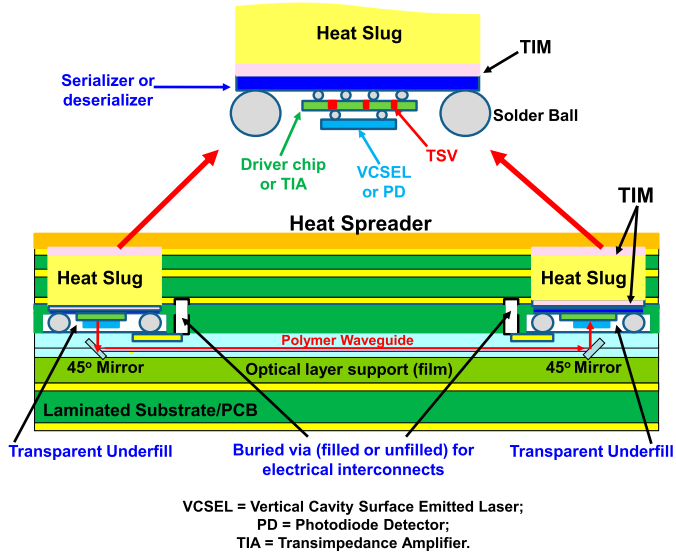


Fig. 54. HKUST's embedded 3D heterogeneous integration of optoelectronic interconnects.

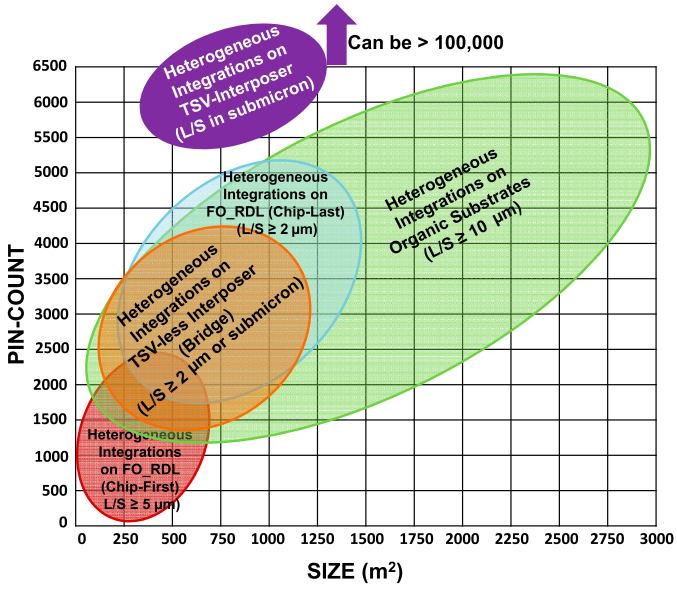


Fig. 55. Substrate size and pin-count for RDLs of heterogeneous integration on organic, silicon (TSV-interposer), silicon (bridge), and fan-out RDL substrates.

7. Electronic design automation tools for automating system partitioning and design are desperately needed for complex heterogeneous integration systems.
8. In the next few years, we will see more of a higher level of heterogeneous integrations, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, or cost.

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