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Cu Pillar Bump Development for 7-nm Chip Package Interaction (CPI) Technology

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***Abstract*—Power, performance, and area gains are important metrics driving the complementary metal–oxide–semiconductor (CMOS) technology from older nodes to newer ones. Over past several decades, a steady downscaling of feature sizes of CMOS technology has been a leading force enabling continual improvement in circuit speeds and cost per functionality. Increase in functionality drives larger number of inputs/outputs (I/Os), and the scaling-driven small intellectual property (IP) block sizes force these larger number of I/Os to be accommodated by reduction of I/O pitches. The result is an unrelenting pressure to reduce bump pitches from one generation of CMOS to another. In contrast to 14-nm/16-nm nodes which used 150-um bump pitch coming out of a die, for 7-nm node, the industry is targeting 130-um bump pitch for high performance devices. With this pitch reduction, conventional tin/silver (SnAg) solder bumps face limitations in terms of bridging. Cu pillar bumps are the best candidate for smaller bump pitches. However, for large die sizes prevalent in high-performance computing (HPC), the Cu pillar bumps will induce higher stress on the silicon resulting in higher risks of extremely low K (ELK) cracking. If copper pillar bumps are not properly developed, then there is a risk of marginal reliability in terms of chip package interaction. The situation becomes even more dire in large die sizes, where coefficient of thermal expansion mismatch between silicon and laminate substrate magnifies the stress. The present article discusses successful development of Cu pillar bumps for 7-nm technology. The development program included a 2-step development path. In the first step, extensive thermomechanical modeling was carried out to find optimal design of copper pillar bump for robustness of interactions with 7-nm back end of line ELK layers. In the second step, a 460-mm^2 7-nm Silicon test vehicle was fabricated, and its assembly process was optimized to characterize the copper pillar bumps and prove their extended reliability on 7-nm silicon. As a result of this development, copper pillar technology has been qualified on Advanced Micro Devices (AMD) products. Today, copper pillar is a fully integral part of AMD's ever-growing 7-nm product offering in HPC.**

***Keywords*—7 nm, chip package interaction (CPI), Cu pillar bump, extremely low K (ELK), finite element analysis (FEA), qualification, reliability, simulation, electromigration (EM)**

Introduction

Power, performance, and area gains are important metrics driving the complementary metal–oxide–semiconductor (CMOS) technology from older nodes to newer ones [1]. Over past several decades, a steady downscaling of feature sizes of CMOS technology has been a leading force enabling continual improvement in circuit speeds and cost per functionality. Increase in functionality drives larger number of inputs/outputs (I/Os), and the scaling-driven small IP block sizes force these larger number of I/Os to be accommodated by reduction of I/O pitches. The result is an unrelenting pressure to reduce bump pitches from one generation of CMOS to another. In contrast to 14-nm/16-nm nodes which used 150-um bump pitch coming out of a die [2-4], for 7-nm node, the industry is targeting 130-um bump pitch for high-performance devices.

With the smaller bump pitch, conventional SnAg lead-free solder bumps are not suitable because they are prone to solder bridging and bump shorts. Cu pillar bump is a promising solution to cope with these challenges of tighter bump pitches. However, one big challenge with copper pillar bumps is their interaction with extremely low K (ELK) dielectric in the underlying back end of line (BEOL) layers. Cu pillar bump is much stiffer than solder bumps. Under the coefficient of thermal expansion (CTE) mismatch between silicon and laminate substrate, the stiff copper pillar will transfer high stress to the Silicon BEOL layer, causing potential for ELK cracking [5-12]. This will affect reliability through suspected marginality of chip package interactions (CPI). To prevent this CPI marginality, the copper pillar design and subsequent laminate assembly process needs to be carefully optimized.

Present work describes development of reliable Cu pillar bumps for 7 nm. Here, modeling & simulation has been used to

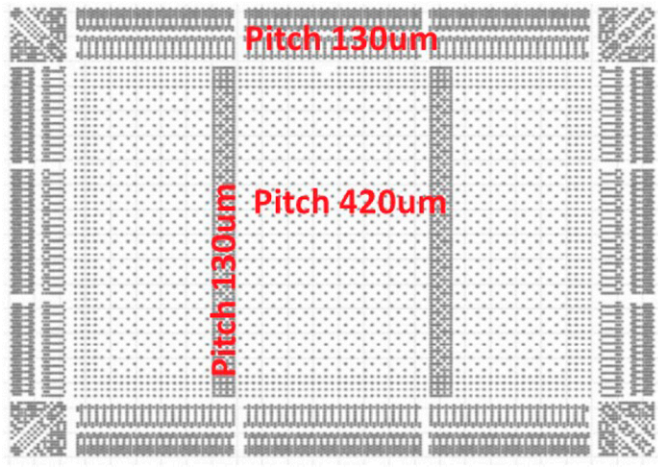

Fig. 1. A 7-nm CPI TV bump pattern.

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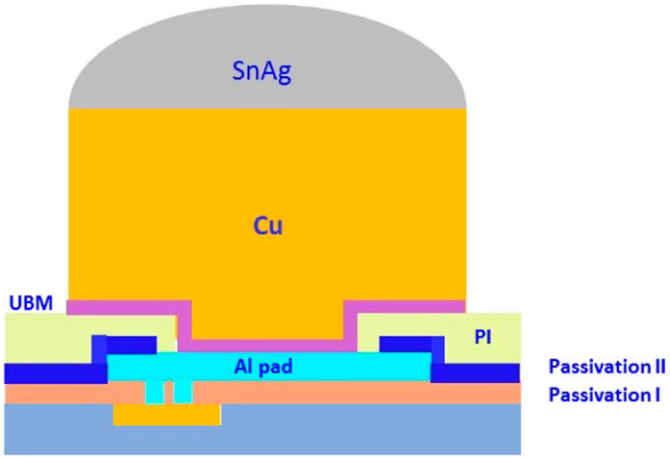


Fig. 2. Schematic of Cu pillar bump structure.

assess the effects of design features such as under bump metallization (UBM) size, polyimide (PI) opening, Cu pillar height, min bump pitch, terminal metal diameter, and die thickness on the stress seen by ELK layers in the vicinity of bumps. This sensitivity analysis has been used to finalize the optimum design of copper pillars for 130-um bump pitch. In the second phase, a 460-mm^2 CPI test vehicle has been fabricated with 7-nm BEOL and 130-um pitch optimum Cu pillar design. Assembly process has been developed and optimized for attaching this TV to laminate substrate.

Accelerated thermal cycling (ATC) test has been used to study ELK cracking risks in the vicinity of Cu pillars. Joint Electron Device Engineering Council (JEDEC) standard–based reliability validation has been conducted to qualify the copper pillars for 7-nm products. Electromigration (EM) tests have been run to evaluate max current that Cu pillar can carry. The results show that the Cu pillar bumps performed much better than SnAg bump in terms of EM current limits. The Cu pillar bump technology has passed the qualification for use in 7-nm products. AMD has a host of Cu pillar–based 7-nm products catering to high-performance computing sector.

CPI Test Vehicle Configuration

Our 7-nm CPI TV mimics the BEOL layers of 7-nm AMD products. The CPI TV and products also share the same ELK material, same 7-nm process, same substrate technology, and the same assembly process. Daisy chains have been designed through BEOL layers for validating BEOL integrity. A TV die size of 25 × 18 mm^2 that was selected to cover most of the expected AMD 7-nm products has been used. To evaluate the worst case CPI risk, 130-um bump pitch in the periphery area and large bump pitch at the die center have been defined in our CPI TV. Figs. 1 and 2 show the schematics of the CPI TV bump pattern and Cu pillar bump structure, respectively. Optimized Cu pillar bump design, which results in less stress on the ELK layers, has been selected and evaluated. 40 × 40-mm^2 substrate has been used in our CPI technology qualification. JEDEC standard tests (precondition, unbiased highly accelerated stress test (UBHAST), thermal cycling test-G (TCG), and high temperature storage test (HTS)) are used as criteria for the CPI technology qualification. ATC test has been used to assess CPI margin for copper pillar interactions with ELK layers.

Cu pillar bump optimization

Stress on the ELK layer has been simulated by using the finite element analysis (FEA) method. The CPI risk has been judged based on tensile stress on the ELK layer. First, global stresses have been estimated by modeling the entire package. Temperature difference experienced during packaging process has been input as the loading condition. Because white bump occurrence was most common during cooling after die attach, peak reflow temperature and room temperature were considered, respectively, as initiation and termination points of the temperature difference. Then, stress acting on a local model, which reflects details of BEOL structure, was analyzed from the boundary conditions of global stress model. Linear elastic material behavior was assumed for the thermomechanical stress analysis. Fig. 3 shows typical global and local model employed for the stress analysis.

Cu pillar dimensions such as UBM size, PI opening, Cu pillar height, minimum bump pitch, terminal metal diameter, and die thickness have been simulated to determine the optimum design to be selected as bump geometry process of record.

Results and discussion

A. Under Bump Metallization Size Effect

Cu pillar bump is more rigid than lead-free bump. With Cu pillar bump, more stress can transfer to the ELK layer underneath

Fig. 3. Model of FEA.

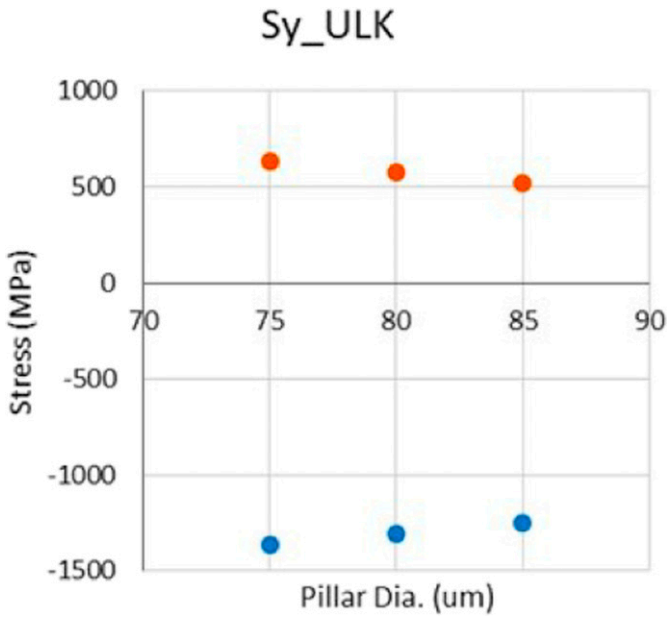


Fig. 4. UBM size effect on ELK stress.

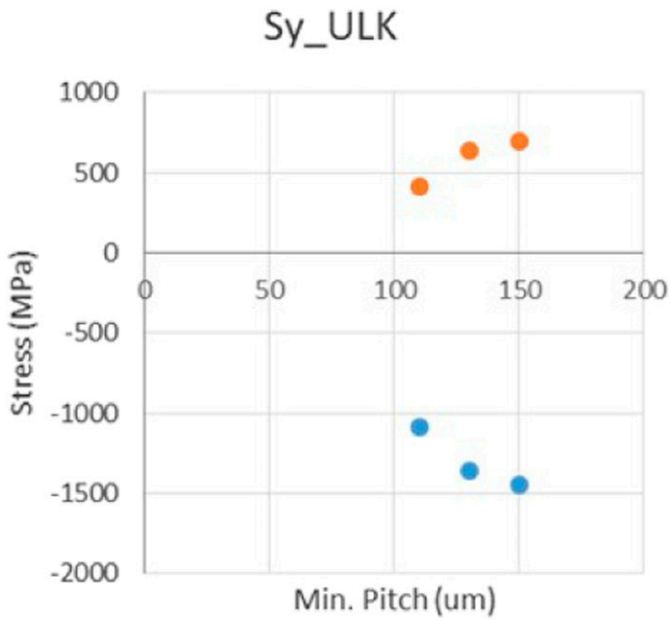


Fig. 6. Minimum pitch effect.

the bump causing cracking of ELK (this failure is normally called white bump). To reduce the white bump failures, the better way is to prevent stress from reaching the ELK layer by dissipating it as much as possible. Large UBM is one of the effective ways to spread the stress across the bump area. In our simulation, 75-85 um UBM sizes have been simulated. Fig. 4 shows FEA results of ELK peeling stress with different UBM sizes. The results indicate that ELK peeling stress is reduced 18% with 85 versus 75-um UBM.

Large UBM can reduce the white bump risks, but it can also induce solder bridging during die attach process. The best UBM size should be selected in conjunction with the assembly process window to avoid solder bridging issues.

B. Cu Pillar Height Effect

Cu pillar height is a very important factor for the assembly because it decides the standoff height after assembly. The higher standoff height with taller pillars reflects in the better flow of the underfill (UF). Better flow of the UF means less stress on the ELK layers and, hence, enhanced CPI reliability. However, the tall pillars can increase the ELK stress without UF. Fig. 5 lists

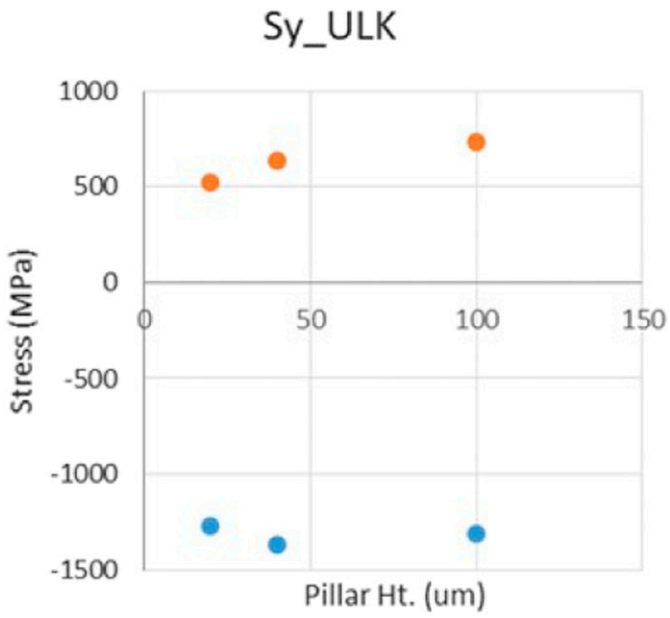


Fig. 5. Cu pillar height effect on ELK stress.

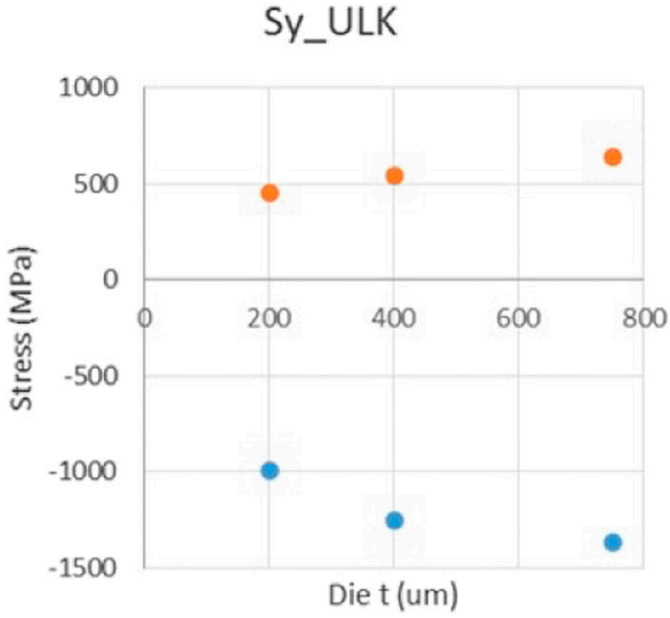


Fig. 7. Die thickness effect on ELK stress.

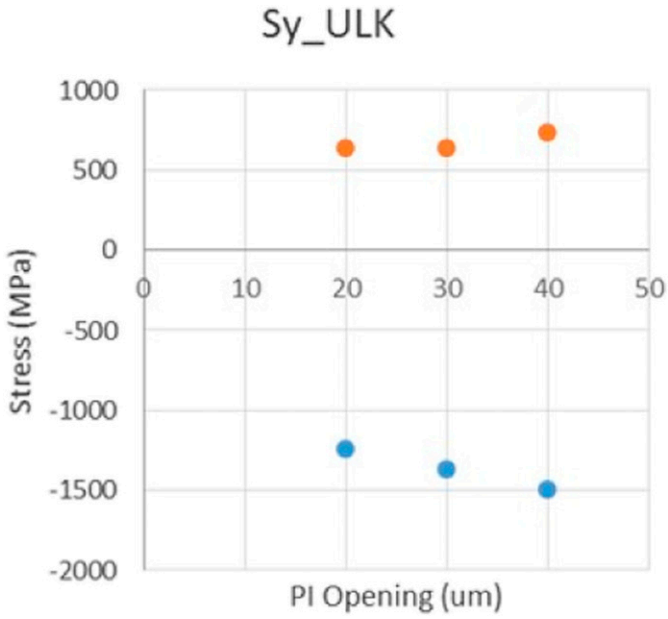


Fig. 8. PI opening effect on ELK stress.

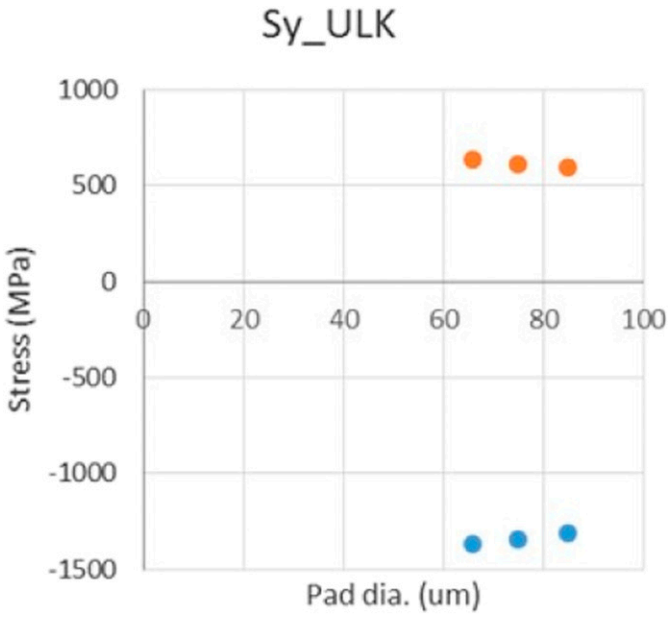


Fig. 9. Al pad diameter effect on ELK stress.

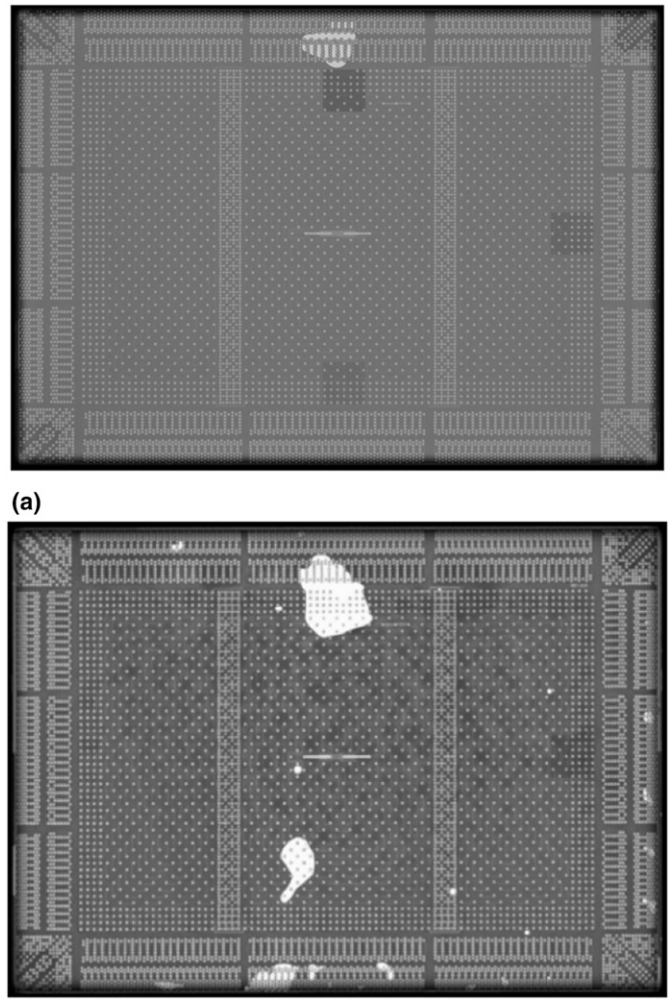


Fig. 10. CSAM images of ATC test. (a) ATC T0 CSAM image. (b) ATC 30 cycles CSAM image.

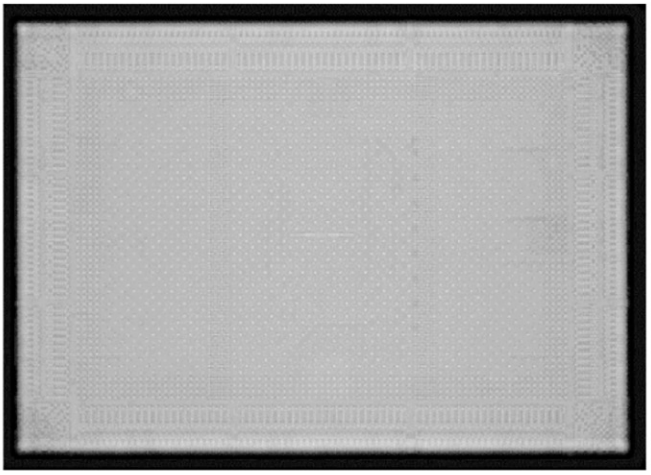
ELK stress at different bump heights showing bump stress increasing 22% from a height of 20 um to 40 um and 15% from 40 um to 100 um. It is best to decide the Cu pillar height with inputs from the assembly process team.

C. Minimum Bump Pitch Effect

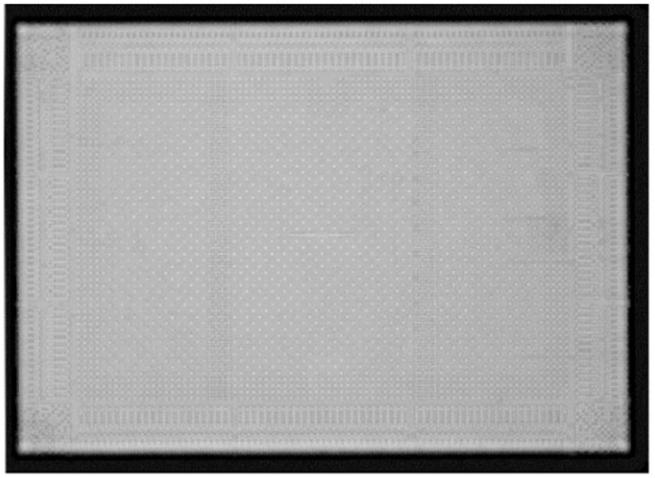
With transistors scaling-down, more transistors are on the die with the same die size. More transistors amount to more

Table I
Reliability Test Condition and Result Summary

Reliability test	Reference standard	Sample size	Results	Conclusion
ATC	AMD spec	45	0/45	Pass
Preconditioning MSL4 (@30° C/60% RH; 96 h + 3× reflow)	JES22 – A113	462	0/462	Pass
Temperature cycling, Cond.G (−45 to 125° C)	JES22 – A104D	154	0/154	Pass
Unbiased HAST (130°C/ 85% RH, 96 hr)	JESD22 – A118	154	0/154	Pass
High-temperature storage (150°C)	JESD22 – A103	154	0/154	Pass



(a)



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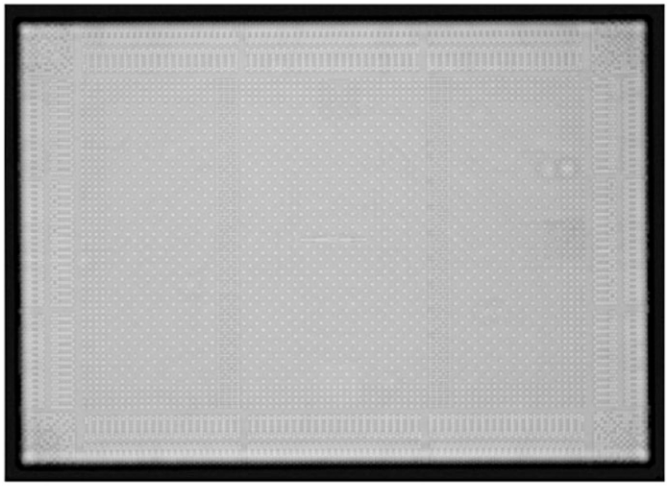
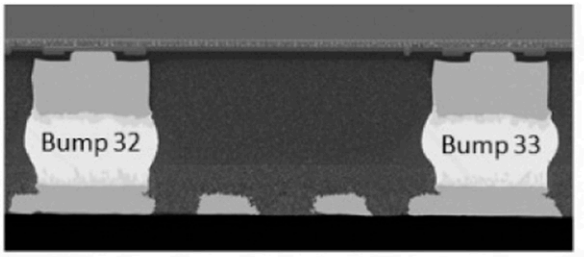


(c)

Fig. 11. CSAM images after reliability tests. (a) CSAM after UBHSAT96hrs. (b) CSAM after HTS1K hours. (c) CSAM after TCG1.2K cycles.



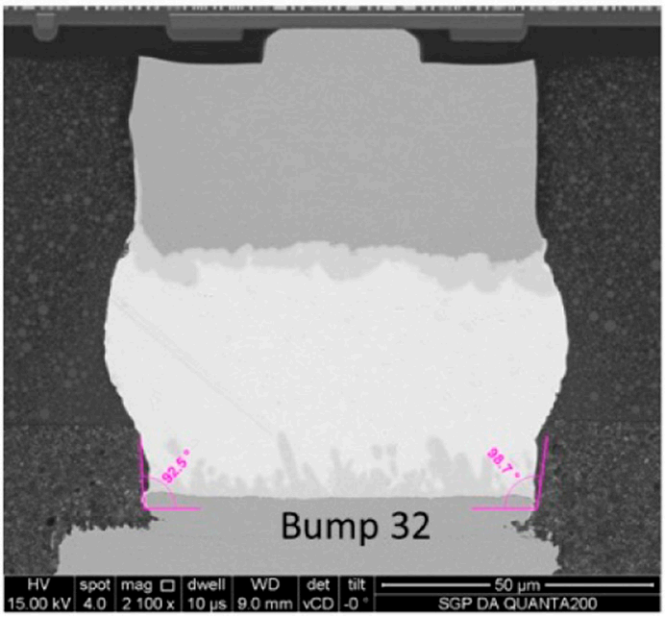


Fig. 12. SEM images of Cu pillar bumps after UBHAST96hrs.

functionality, but the impact is greater number of bumps to support power/ground as well as additional signal lanes. These additional I/Os need to be supported on smaller die sizes. This is achieved through scaling down of the bump pitch. Fig. 6 shows the effect of the bump pitch on the ELK stress. Reducing bump pitch from 150 um to 110 um will lower 69% of the ELK stress and this will improve CPI reliability. Decreased pitch results in more support at the die corners, thus reducing stress concentration on individual bumps and reducing stress on the ELK layers.

D. Die Thickness Effect

To further reduce the stress on the chip, chip thickness reduction can be considered. By using thinner chips, effective CTE difference between the chip and package substrate can be reduced because the volume of chip is reduced. The die stiffness also reduces. The net effect is expected reduction in stress. As shown in Fig. 7, ELK peeling stress decreases 40% with die thickness from 750 um to 200 um.

E. Polyimide Opening Effect

PI acts as stress buffer layer and plays an important role in ELK stress reduction. Geometric parameters associated with PI are investigated to find ways to lower stress on the ELK layers. Fig. 8 shows the effect of PI opening dimension on the ELK

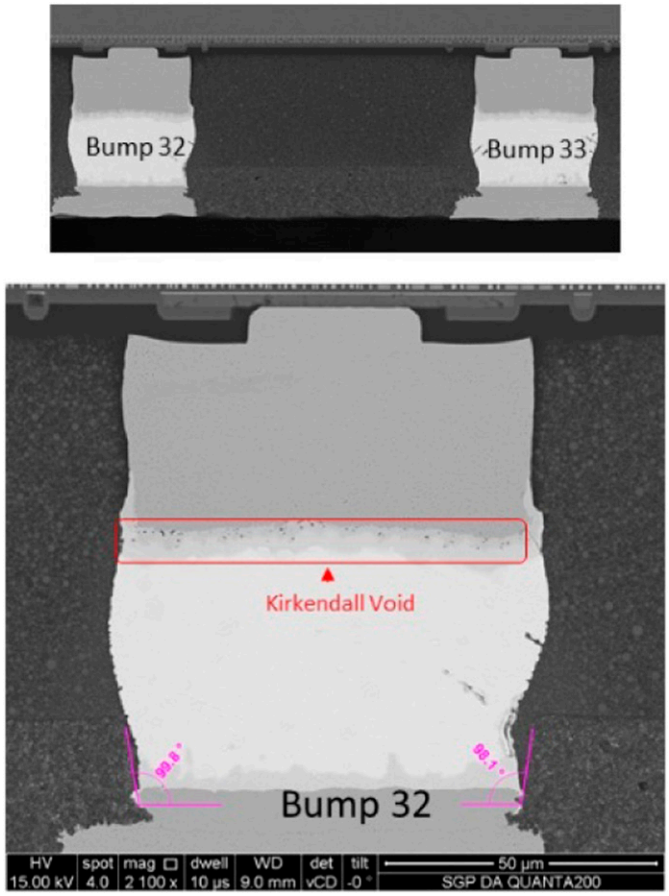


Fig. 13. X-section after HTS1000 h.

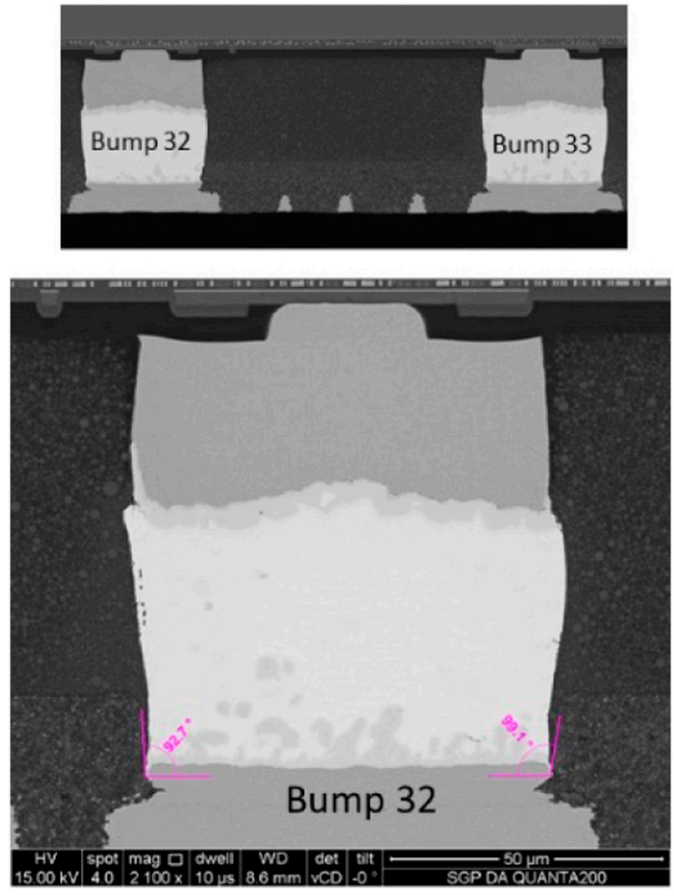


Fig. 14. X-section after TCG1.2K cycles.

stress. It indicates that ELK peeling stress increases 16% with PI opening increase from 20 um to 40 um. Smaller PI opening offers greater padding of PI to act as a stress buffer layer.

F. Aluminum Terminal Pad Diameter Effect

Al pad has been widely used on the die as a bump terminal metal to increase CPI reliability margin and reduce white bumps failures. Fig. 9 shows the effect of Al pad diameter on ELK peeling stress. It shows that the ELK peeling stress decreases with increasing pad diameter. This is because larger pad provides larger area for the stress dissipation & energy absorption.

Reliability test results

The optimized bump geometry was determined based on the aforementioned simulation results. The resulting 7-nm CPI TV was used to optimize the assembly process. Subsequently, the same CPI TV was used for 7-nm CPI qualification.

ATC test was used to evaluate the CPI margin of ELK layers. The parts are built without UF and are run through a thermal cycling test (−40 to 60°C). The pass/fail criteria is decided by the absence/presence of white bump defects after ATC. Normally, passing 30 ATC cycles without white bumps is selected as the release condition for starting CPI qualification. The more the cycles passed, the stronger the ELK dielectric material and the better the CPI performance. Representative confocal scanning acoustic microscopy (CSAM) pictures in Fig. 10 at ATC 0 (Fig. 10a) and ATC 30 cycles (Fig. 10b) show no white bumps encountered. The white areas in the CSAM images are due to water voids. Sometimes, water cannot wet all the surface and form the voids. They appeared white during CSAM and are not real defects.

The standard JEDEC tests with selected conditions (preconditioning, TCG, UBHAST, and HTS) are used for our Cu pillar development for 7-nm CPI qualification. Table I lists the tests and conditions, sample size, and test results. Samples have passed all the test specs. The test results prove optimized Cu pillar bump working well and passing CPI qualification. Our current Cu pillar bump design rules, bump selection, assembly process, and substrate technology have been implemented in AMD's 7-nm products.

Fig. 11 provides the CSAM images after reliability tests. There is no anomaly after unbiased HAST96hrs (Fig. 11a), high temperature storage 1,000 hrs (Fig. 11b), and thermal cycling test (G) 1,200 cycles (Fig. 11c). Scan Electron Microscopy (SEM) cross-section analysis was used to check the bump integrity after reliability tests. Fig. 12 is the SEM X-section images after UBHAST96hrs. There is no bump crack and anomaly. Thin layer of intermetallic compound (IMC) is formed at a SnAg/Cu pillar and SnAg/substrate pad interface.

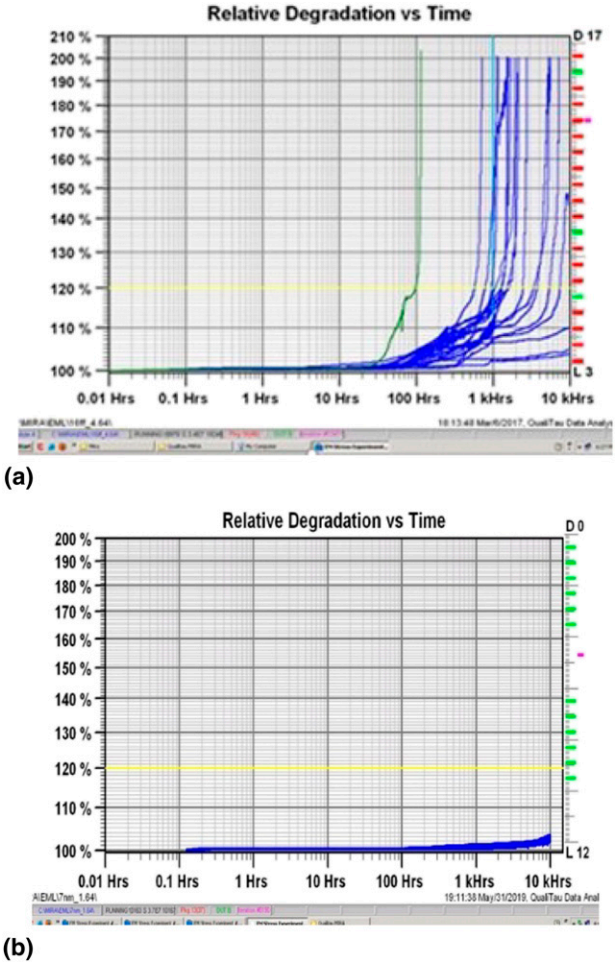


Fig. 15. EM performance comparison between SnAg bump and Cu pillar bump. (a) SnAg EM test data at 0.6A/140°C. (b) Cu pillar bump EM test result at 0.6A/140°C

Fig. 13 lists SEM images of the sample after HTS 1,000-h test. No solder crack observed. A thick and uniform IMC layer and Kirkendall voids were found to have formed at the interface between the Sn solder and Cu because of the Cu diffusion at high temperature. Fig. 14 showed SEM X-section images after TCG1.2K cycles. IMC thickness is slightly thinner and there are less Kirkendall voids than HTS1000hrs. No anomaly was encountered in any of the reliability tests. All the X-section images are taken from the center bumps of the outermost row.

EM results in structural damage of metallic conductors because of atomic diffusion driven by high electric current density. This phenomenon is related greatly to the current density and temperature experienced by a metallic conductor. Recently, EM has received a lot of attention because of high-performance computing and gaming requirements. The evaluation of the Cu pillar bump EM performance provides very important information to the device designers. It helps them decide the maximum current that can be applied to the device. This helps drive performance in the devices.

An EM test TV was designed and built. An EM test system has been set up to test optimized Cu pillar bumps. Fig. 15 shows EM test result of SnAg bump and Cu pillar bump under the same test condition. There are a few early failures for SnAg bumps. Many units start to fail after 1,000 h, and most of the samples fail at 10k hours with the test condition of 0.6A/140C. Looking at Cu pillar bumps, no unit failed in 10k hours under the same test condition. It can be concluded that a Cu pillar bump has much better EM performance than a SnAg bump.

Conclusion

FEA was used as an effective tool to evaluate ELK stress with different geometries of the Cu pillar bump. Copper pillar bump designs should be fixed based on pointers from FEA studies and based on assembly process window considerations. Optimized Cu pillar bump design has been applied on 7-nm CPI TV, and the assembled TV has been successfully passed through CPI qualification runs. The ATC test has been used as a quick method of testing robustness of the optimized Cu pillar bump. All reliability tests pass without any failures. The EM tests confirm Cu pillar bump has much better performance as compared with lead-free solder bumps. A 7-nm CPI TV passes full reliability qualification as defined by the relevant JEDEC standards. The resulting Cu pillar bump has been applied to all 7-nm products in AMD.

Acknowledgments

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