Electrical Characterization of High Performance Memory FBGA BOC Package

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Abstract

A multilayer Fine-pitch Ball Grid Array (FBGA) Board-on-chip (BOC) memory package used for applications running at more than 1 Gbit/p/s has been characterized using S-(distributed) parameter measurements and three types of test chips made using state of the art technology. The low parasitics FBGA test board itself was characterized for frequencies up to 5 GHz (the frequency range of interest) with the transmission being greater than -0.12 dB below 5 GHz. S-parameter model simulation of the package itself indicated that the transmission was greater than -1.5 dB up to 5 GHz. Correlation between the S-parameter simulation and measurements for the package and fixture combined was acceptable - in the order of tenths of dB in the frequency range DC to 2.5 GHz. Comparison of the S-parameter model versus lumped (RLC) model in the frequency range from DC to 5 GHz showed that the lumped model can be used for frequencies up to 2.9 GHz. A high degree of correlation between simulation and measurement has been shown. The lumped model bandwidth has been assessed and its application limits for time domain signal integrity simulations have been evaluated.

Key words: FBGA BOC package, electrical characterization, package electrical performance, vector network analyzer.

1. INTRODUCTION

This paper describes the characterisation of a multilayer FBGA-BSP (Fine-pitch Ball Grid Array – Back Side Protection) Board-on-chip (BOC) memory package used for applications running at more than 1 Gbit/pin/s. Here the power distribution system (PDS) with its parasitics has a major impact on signal integrity even at clock frequencies below 1 GHz as it serves as return path in comparison to differential designs. Therefore availability at an early design stage of an accurate package model valid in a wide frequency range is necessary.

The objective has been to correlate the simulated S-parameter and lumped package models to the measurement, estimating the simulation model bandwidths and the limits of their application.

2. THE FBGA BOC HIGH SPEED MEMORY PACKAGE

The package under investigation uses Infineon in-house FBGA-BSP BOC package technology, allowing a family concept with clustered package sizes for standardized memory ball outs. As seen in Fig.1, the chip with center pad row is mounted face – down on the substrate and is connected to it by bonding wires. Mold resin ensures backside as well as bonding wires protection.

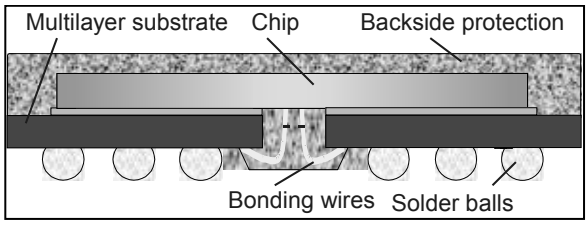

Fig. 1. The FBGA BOC package cross-section.

The electrical behavior of the chip package has to fulfill the tight requirements for system timings as a part of the high-speed memory interconnect channel, while maintaining low cost within tight design windows.

Therefore the availability of an accurate package model to be used at the early development stages is crucial for the design success. To achieve this goal, a correlation between simulation models and measurement has been carried out.

3. MEASUREMENT

3.1 Measurement Setup

In order to assess the package electrical characteristics, three types of test chip packages, providing open, short and thru connections at chip side for the adjacent pin pair requested for characterization, have been soldered onto FBGA test boards, allowing the use of coplanar probes and adding minimum parasitics. The pins around the measured pin pair have been connected to the board ground plane. HP 8753E VNA (Vector Network Analyzer) has been used for 2-port S-parameter measurement.

3.2 Test Fixture Characterization and De-embedding

To get the test fixture scattering parameters for the de-embedding, a full-wave solver [4] has been used. The test fixture model is shown in Fig. 2. The test fixture has been modeled following the available cross-section and material information from the supplier.

Two adjacent signal vias surrounded by 10 ground vias have been included in the model. Two ports have been placed at the probing reference plane and other two ports at package landing pads.

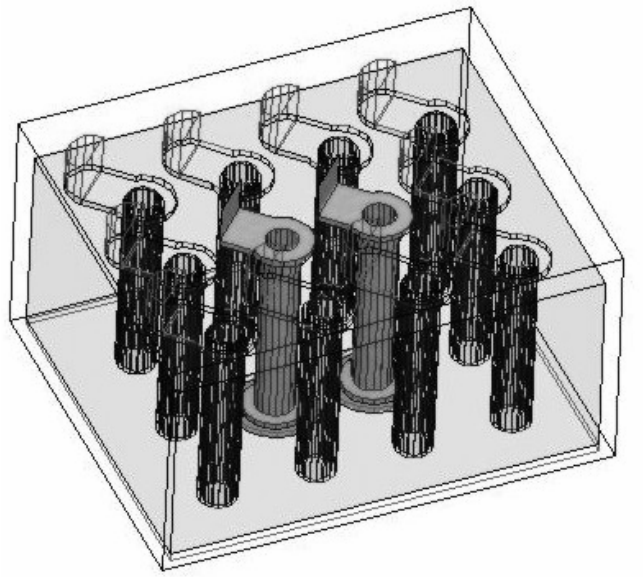

Fig. 2. Test fixture simulation model.

The fixture has been characterized in the frequency range 0-5 GHz, Figures (3) and (4).

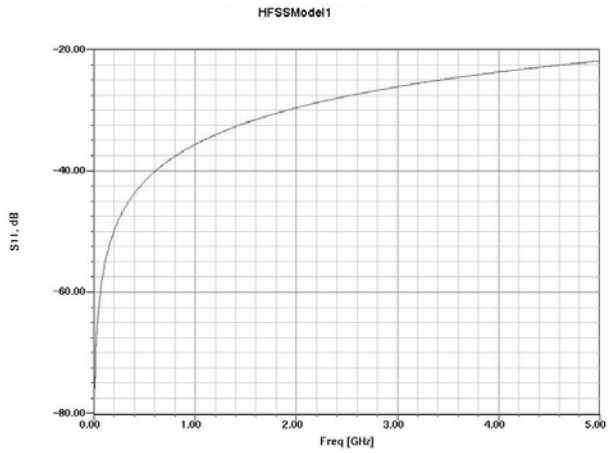

Fig.3. Simulated reflection for the test fixture.

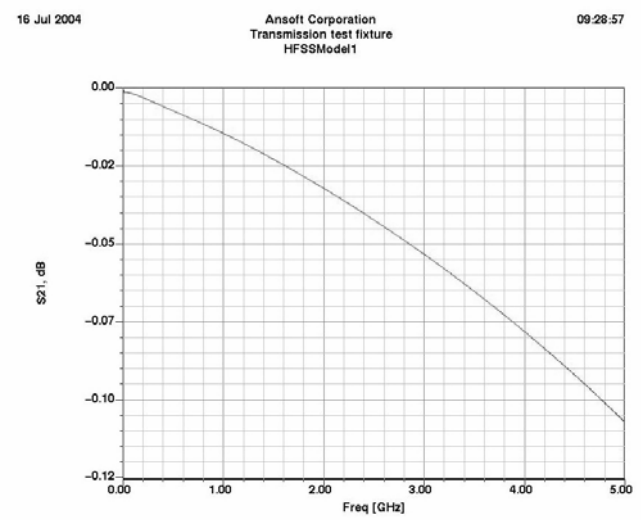

Fig.4. Simulated transmission for the test fixture.

As can be seen from Fig.3 and Fig.4, the reflection at the balls of the test fixture is less than -20 dB for the frequency range of interest, and the transmission is greater than -0.12dB below 5GHz.

3.3 Measurement Results

To characterize the electrical behavior of package, the following 2-port S-parameter measurements have been performed:

- 2-port S-parameter measurement for characterization of test board.
- 2-port S-parameter measurement for the pin pair under the termination conditions of open, short and thru at chip side [2], [3].

In order to compare with the simulated lumped package model, the lumped RLC values for the measured pin pair have been extracted from the measured S-parameter data using ADS (Advanced Design System) software [6]. The lumped RLC model extracted from S-parameter shown in Fig. 5.

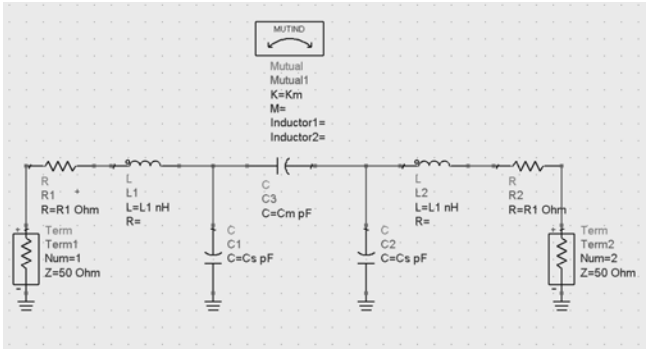

Fig.5. Equivalent circuit topology for adjacent signal pins.

Element definition in Fig. 5:
R1, R2: series resistance of signal path from solder ball to chip bond pad
L1, L2: self inductance of signal path from solder ball to chip bond pad
M: mutual-inductance between the measured pin pair
C1, C2: self capacitance of signal path from solder ball to chip bond pad
C3: mutual-capacitance between the measured pin pair

The self capacitance C and mutual capacitance Cm values of the elements in the equivalent circuits have been extracted from the open measured S-parameters by following formulas [1]:

$$Cself = \frac{1}{2\pi f Z_0}\,\mathrm{Im}\left[\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}\right] \quad (1)$$

$$Cm = \frac{1}{2\pi f Z_0}\,\mathrm{Im}\left[\frac{-S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}\right] \quad (2)$$

The self inductance L, mutual inductance Lm and resistance values R have been extracted from the short 2-port S-parameters by the following formulas [1]:

$$Lself = \frac{Z_0}{2\pi f}\,\mathrm{Im}\left[\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}\right] \quad (3)$$

$$Lm = \frac{Z_0}{2\pi f}\,\mathrm{Im}\left[\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}\right] \quad (4)$$

$$R = Z_0\,\mathrm{Re}\left[\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}\right], \quad (5)$$

where Z_0 is the system characteristic impedance in Ω and f is the excitation frequency in Hz.

3.4 De-embedding Procedure

The system has been characterized by measuring the 2-port S-parameters at the inputs of the test-fixture (TF) - each number represents one port against ground (Fig.6.):

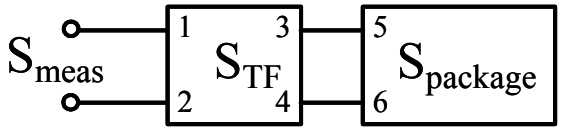

Fig.6. Measurement setup: TF plus package.

The TF itself has been described as a 4-port, modeled with HFSS using its geometrical data and compared against TF measurements (open at package side) for verification.

To compute the 2-port S-parameters of the package, another "inverse" S-parameter matrix S_{TF}^{-1} of the TF have been used for embedding the S-parameter network of the TF (Fig.7):

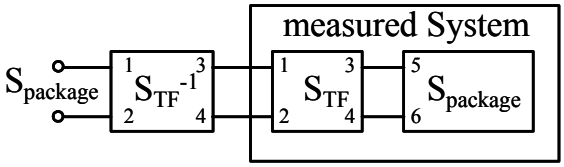

Fig.7. Embedding of an "inverse" network.

This has been applied as given in Fig. 8:

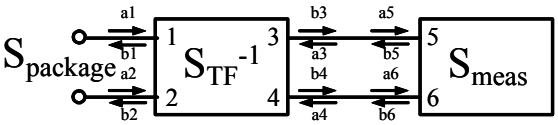

Fig. 8. S-parameter package matrix as a result of embedding of an "inverse" network.

A set of ten S-parameter equations (6) - (15), describing the whole system has been set up according to Fig. 8 above:

$$g1:\ b1 = s11 \cdot a1 + s12 \cdot a2 + s13 \cdot a3 + s14 \cdot a4 \quad (6)$$
$$g2:\ b2 = s21 \cdot a1 + s22 \cdot a2 + s23 \cdot a3 + s24 \cdot a4 \quad (7)$$
$$g3:\ b3 = s31 \cdot a1 + s32 \cdot a2 + s33 \cdot a3 + s34 \cdot a4 \quad (8)$$
$$g4:\ b4 = s41 \cdot a1 + s42 \cdot a2 + s43 \cdot a3 + s44 \cdot a4 \quad (9)$$

$$g5:\ a3 = b5 \quad (10)$$
$$g6:\ a4 = b6 \quad (11)$$
$$g7:\ b3 = a5 \quad (12)$$
$$g8:\ b4 = a6 \quad (13)$$

$$g9:\ \ b5 = s55 \cdot a5 + s56 \cdot a6 \quad (14)$$
$$g10:\ b6 = s65 \cdot a5 + s66 \cdot a6 \quad (15)$$

Equations (6) - (9) describe the inverse network of the TF using S_{TF}^{-1}, (10) - (13) - the connection between this network and the measured network (given by S_{meas} – measured at TF inputs) and finally *(14)* and *(15)* describe the S-parameters of S_{meas} itself.

In that set of equations *b1* and *b2* can be computed as function of *a1*, *a2* and *s11 .. s44* (given by S_{TF}^{-1}) and *S55 .. S66* (given by S_{meas}) by eliminating *a3 .. a6* and *b3 .. b6*. The new set of equations has the following form:

$$b1 = s11\_pack \cdot a1 + s12\_pack \cdot a2 \quad (16)$$
$$b2 = s21\_pack \cdot a1 + s22\_pack \cdot a2 \quad (17)$$

s11_pack .. s22_pack are the desired S-parameters, expressed in terms of s11 .. s66. This elimination process has been performed with Mathematica [7]. The computed equations have been inserted into Excel to do the deembedding on the measured data.

4. PACKAGE MODELING

To compare the simulation vs. measurement results of the memory package, a simulation of the measurement setup has been performed. The measured signal pair (trace1, trace2) has been chosen for measurement setup simulation. Part of the package with surrounding pins has been modeled by a full-wave solver [4] using the three measured terminations (open, short, thru). The 3 sets of 2-port S-parameters ("open", "short", "thru") have been used for comparison with the measured results.

Then, a 4-port S-parameter model for the pin pair under investigation has been simulated. The model can be used in chip- and system-level simulations. The reflection for both signal traces has been found to be below -20 dB for frequencies up to 2.2 GHz, and the transmission up to 5 GHz has been higher than -1.5dB (Fig. 9. and Fig. 10.).

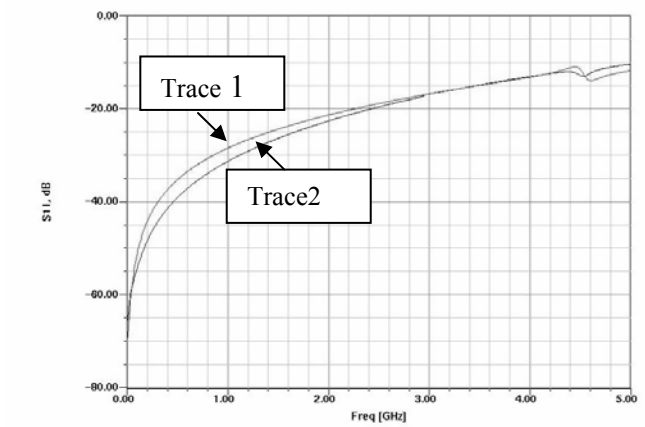

Fig.9. Simulated signal trace reflection.

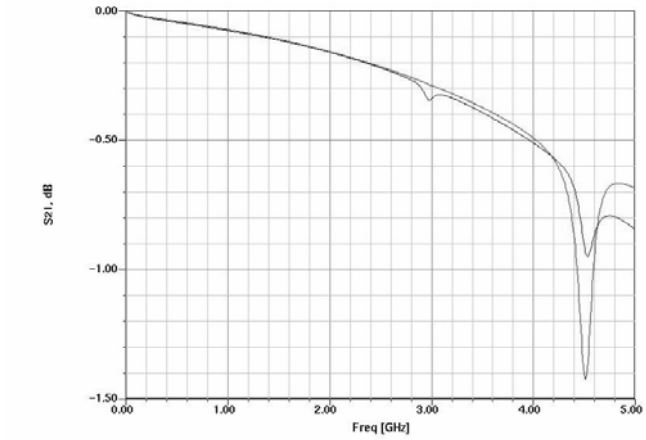

Fig.10. Simulated signal trace transmission.

5. COMPARISON

5.1 S-Parameter Comparison

Direct S-parameter comparison of the measured and the simulated result including test fixture parasitics is shown in Fig. 11 a) – f) for all three measured configurations.

All diagrams show a very good correlation in terms of S-parameters of simulation and measurement. The deviations in amplitude of reflection (short and open) and coupling (thru) are tolerable – in order of tenths of dB.

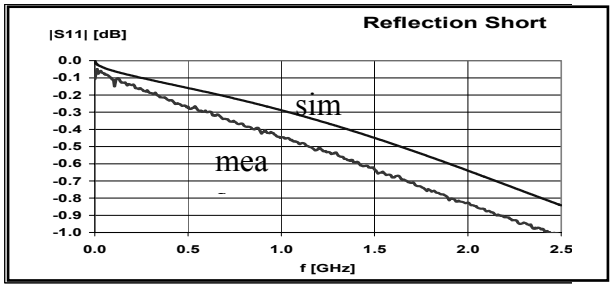

Fig. 11a. Measured vs. simulated reflection for "short" measurement configuration.

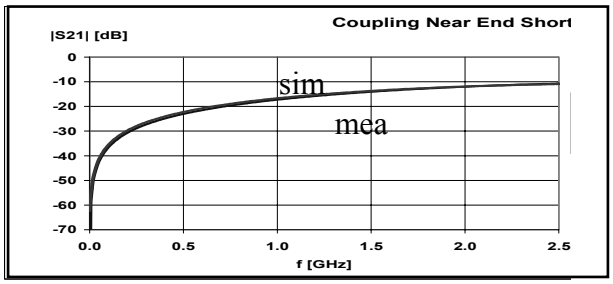

Fig. 11b. Measured vs. simulated near-end coupling for "short" measurement configuration.

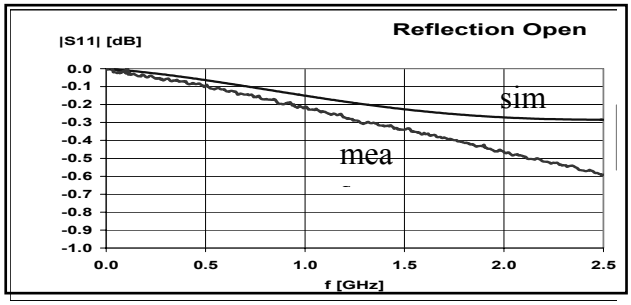

Fig. 11c. Measured vs. simulated reflection for "open" measurement configuration.

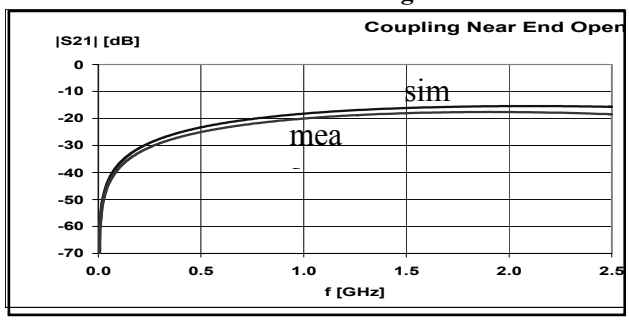

Fig. 11d. Measured vs. simulated near-end coupling for "short" measurement configuration.

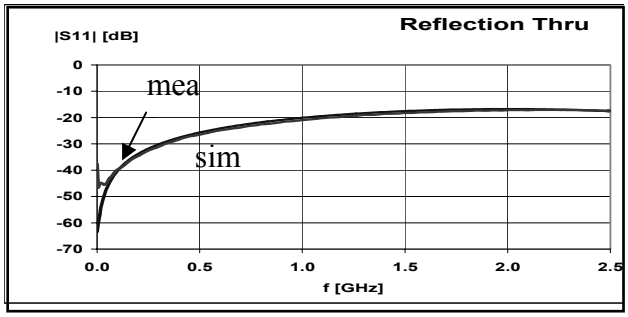

Fig. 11e. Measured vs. simulated reflection for "thru" measurement configuration.

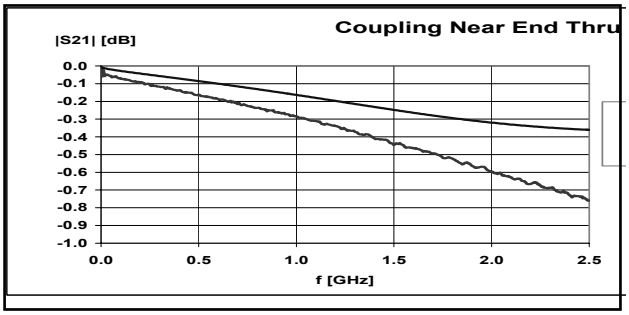

Fig. 11f. Measured vs. simulated near-end coupling for "thru" measurement configuration.

5.2 RLC Values Comparison

The measured data including the test fixture have been compared to the simulated data with regard to lumped RLC values.

For this comparison extracted RLC values from a quasistatic EM simulation [5] have been used.
For the correct comparison the following effects have been considered:

- the capacitance model from measurement calculates the C_{ii} value as a Spice capacitance, whereas the EM tool extracts the Maxwell one. The measured value has to be recalculated:

$$C_{sim} = C_{ii,\,meas} + \Sigma C_{ij,\,meas} \qquad (18)$$

- the resistance values are calculated from the "short" setup, therefore test chip layout resistance, wire bond contact resistance as well as ground return path resistance are included in the measured value:

$$Rmeas = Rpackage + Rtest\ layout + 2\ .\ Rcontact + Rreturn\text{-}path \qquad (19)$$

The comparison of measured vs. simulated capacitance values is shown in Fig. 12, and measured vs. simulated inductance values are shown in Fig.13.

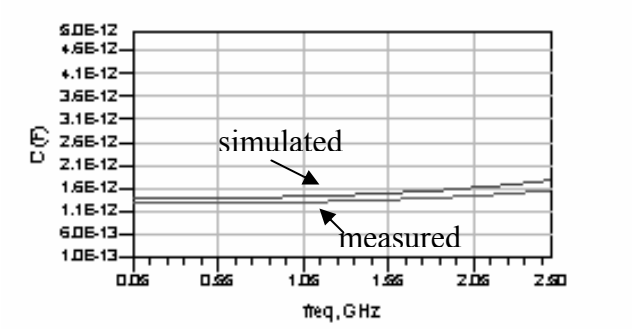

Fig.12. Comparison of simulated and measured capacitance values for trace1

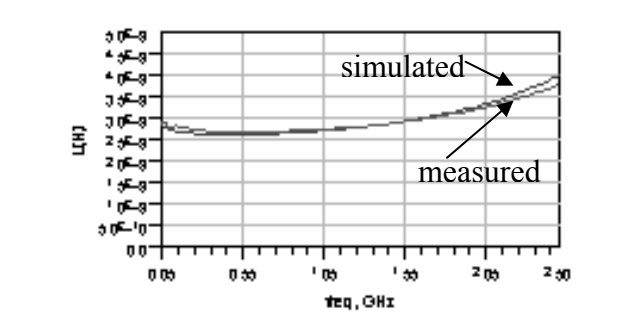

Fig. 13. Comparison of simulated and measured inductance values for trace1

The comparison of S-parameter model vs. lumped package model in the frequency range from DC to 5GHz shows that the lumped model can be used for bandwidths of up to 2.9GHz, which determines the validity of the lumped approach until this frequency (Fig. 14).

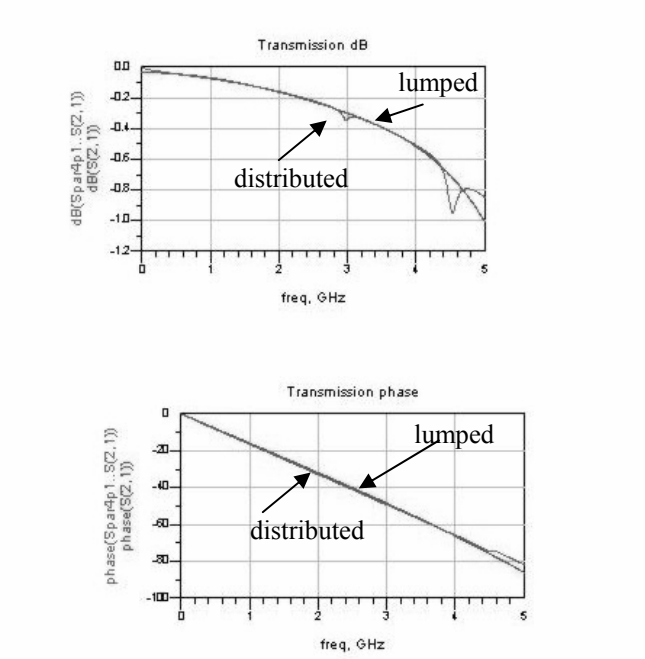

Fig. 14. Comparison of lumped vs. distributed package model behavior in frequency domain for trace1.

Finally, time-domain simulations have been carried out to compare the behavior of lumped vs. distributed package models (Fig. 15).

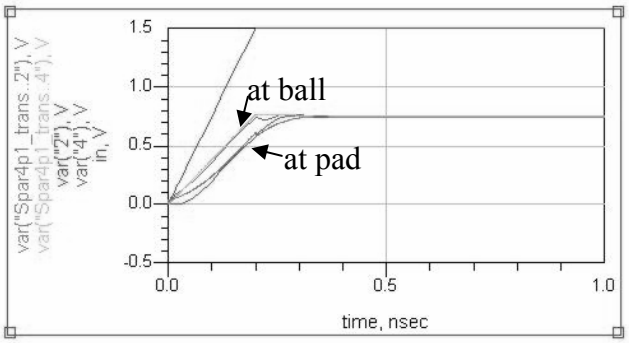

Fig. 15. Comparison of lumped vs. distributed package model behavior in time-domain for trace1

In time domain, the difference between pulse responses simulated using S-parameters and those using lumped element package models is not higher than a few picoseconds. That fact allows using lumped element approach in the required signal bandwidth. Also, it shows the validity of the generated package models for the given memory package application.

6. CONCLUSION

The objective of the paper has been to correlate the simulated S-parameters and lumped package models to the measurement, estimating the simulation model bandwidths and the limits of their application.

Advanced characterization techniques have been applied in order to achieve the above goal. The memory package has low parasitics values which have to be modelled with high precision in order to predict the timings on the memory bus with a high precision.

Modeling methodology including low parasitics test fixture de-embedding and assessment of comparison results has been developed. This procedure has been applied to correlate the simulation results to measurement in terms of S-parameters and RLC-values.

A high degree of correlation between simulation and measurement has been shown. The lumped model bandwidth has been assessed and its application limits for time domain signal integrity simulations have been evaluated to be accurate enough for using the generated models in system-level as well as chip-level simulations for the given high-speed memory application.

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Biographical Notes

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From 1983 until 2001 she worked as a lecturer and associated professor at the Department of Microelectronics, Technical University of Sofia, Bulgaria. Since 2001 she is with Infineon Technologies AG in Germany and works on DRAM package electrical characterization. She has published more than 40 conference and journal papers. Her current research interests include simulation and modeling of interconnects and chip packages, digital signal integrity, high-speed DRAM package design.
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Jochen Thomas holds a diploma degree (Dipl.-Ing.) and Ph.D. in electrical engineering, both from University of Erlangen, Germany, obtained in 1993 and 1999, respectively.

After working on diamond layer CVD at Tor Vergata University of Rome in 1994, he carried out a Ph.D. thesis on micro system technology vibration sensors for automated production tool state control, conducted at the Fraunhofer Institute of Integrated Circuits, Device technology section, at Erlangen until 1999. Since 1999, he has worked on package design and package definition for memory products at Infineon Technologies. Starting at Regensburg, Germany, he moved to Munich, Germany in 2001. He is responsible for memory products package design and definition group. His research interests deal with package design for meeting high speed and high density memory demands.

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Joachim Held graduated 1986 in electrical engineering at the Technical University of Erlangen, Germany. 1996 he joined the Siemens AG delivering EMC-support in Regensburg. Since 1998 he extended his field of operation from measurement to simulation in EMC at Siemens AG Munich, working on optimized decoupling for automotive microcontrollers, modeling and measuring of microcontroller supply-systems and emission simulation, e.g. in the EU-project COSIME.
Among his innovations are the principle of inductive current-dividing for supply-systems and the special measurement-method for VLSI supply-currents. His research interests are optimized decoupling concepts for digital VLSI circuits and EMC models of VLSIs and packages.