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State-of-the-Art in Chiplets Horizontal Communications

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***Abstract*—In this study, the recent advances and trends in chiplet lateral communications (bridges) will be investigated. Emphasis is placed on the definition, kinds, advantages and disadvantages, challenges (opportunities), and examples of chiplet horizontal communications. Some recommendations will also be provided.**

***Keywords*—Chiplets, heterogeneous integration, bridges**

Introduction

The key advantages of chiplet design, such as chip partition (for technology optimization) and chip split (for manufacturing yield), are cost, cost, and cost [1]. The key disadvantages (opportunities) of chiplet design and heterogeneous integration package are: (1) larger package size and (2) higher packaging cost. The reasons are: (1) in order to obtain higher semiconductor manufacturing yield, which translates to lower cost, the system-on-chips (SoCs) or chips are partitioned and/or split into smaller chiplets (thus, the size of the package is larger), and (2) in order to let those chiplets to perform lateral or horizontal communication, additional packaging efforts are needed (thus, the cost of the package are higher).

In the past, the lateral (horizontal) communication of chiplet design and heterogeneous integration packaging is by build-up high-density organic substrate or fine-metal line width and spacing (L/S) through silicon via (TSV)-interposer. Fig. 1 shows an application processor chipset in the smartphone of HTC (Desire 606 W), which was shipped in 2013. The application processor chipset is SPREADTRUM SC8502, which is a heterogeneous integration of the modem and application processor by the fan-out chip-first process. These chips are supported by the fan-out 2-layer redistribution layers (RDLs) substrate and then solder balled on a printed circuit board (PCB).

Fig. 2 shows AMD's 2nd Gen extreme-performance yield computing (EPYC) server processors [2, 3], the 7002-series, shipped in mid-2019., One of AMD's solutions is to partition the SoC into chiplets, reserving the expensive leading-edge silicon for the central processing unit (CPU) core while leaving the I/Os and memory interfaces in n-1 generation silicon. Another solution is to split the CPU core into smaller chiplets. In this case, each core complex die (CCD), or CPU compute die, is split into two smaller chiplets. AMD used the expensive 7 nm process technology fabricated by TSMC (in early 2019) for the core CCD chiplets and moved the dynamic random-access memory (DRAM) and logic to a mature 14 nm I/O die fabricated by GlobalFoundries.

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The 2nd Gen EPYC is a 2D chiplets IC integration technology, i.e., all the chiplets are side-by-side on a 9-2-9 build-up package substrate. The 20-layer fine-metal L/S organic substrate is not cheap.

Fig. 3 shows the Virtex-7 HT family shipped by Xilinx in 2013. In 2011, Xilinx asked TSMC to fabricate its field programable gate array (FPGA) SoC with 28 nm process technology [4, 5]. Because of the large chip size, the yield was very poor. Then, Xilinx redesigned and split the large FPGA into four smaller chiplets as shown in Fig. 3 and TSMC manufactured the chiplets at high yield (with the 28 nm process technology) and packaged them on their chip-on-wafer-on-substrate (CoWoS) technology. CoWoS is a 2.5D IC integration, which is the key structure (substrate) to let those four chiplets do

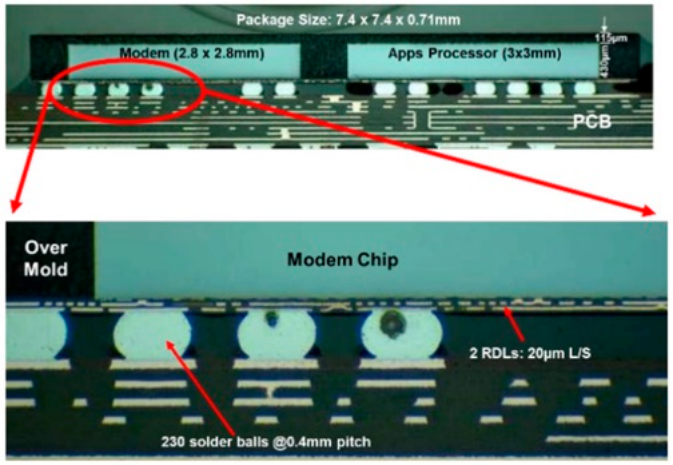

Fig. 1. Heterogeneous integration on a fan-out RDL.

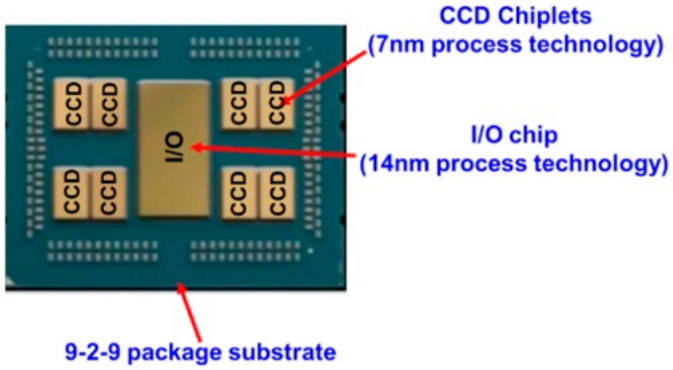

Fig. 2. Heterogeneous integration on a package substrate.

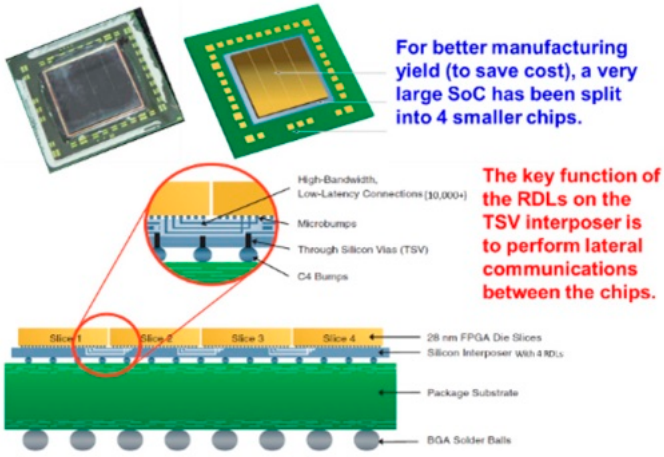

Fig. 3. Heterogeneous integration on a TSV interposer.

lateral communications. The minimum pitch of the four RDLs on the TSV interposer is 0.4 μm. The TSV interposer is known to have a very high cost.

It should be noted that the requirement of lateral communications (RDLs) between chiplets is fine-metal L/S/H (thickness) and at a very small and local area of the chiplets. There is no reason to use the whole fan-out RDL substrate, the whole build-up package substrate, or the whole TSV interposer to support the lateral communication between chiplets. Therefore, the concept of using small area and a fine-metal L/S/H RDLs bridge (a piece of chip without device) to connect the chiplets to perform lateral communication (to reduce cost and enhance performance) for chiplet design and heterogeneous integration packaging has been proposed in the industry [6-32] and is a very hot topic today. There are at least two different groups of bridge, namely rigid bridge and flexible bridge.

Rigid Bridges Versus. Flexible Bridges

Rigid bridge consists of the RDLs and the substrate . Most rigid bridges are with silicon substrate and the RDLs are fabricated on a silicon wafer. Some rigid bridges are even with TSVs. Flexible bridge is the RDL itself. Today, most of the products and publications with bridges are rigid bridges. The focus of this studyis mainly on rigid bridges w/o TSVs. There are at least two groups of rigid bridges, namely, (1) rigid bridges with build-up package substrate, and (2) rigid bridges with fan-out RDL substrate.

Intel's Embedded Multidie Interconnect Bridge

The most famous rigid bridge is Intel's embedded multidie interconnect bridge (EMIB) [6-9]. Fig. 4a shows one of Intel's EMIB patents [6], while Fig. 4b shows the omni-directional interconnect (ODI) Type 2. It can be seen that the EMIB die is embedded in the cavity of a build-up package substrate, which is supporting the chiplets. Fig. 5 shows Intel's processor (Kaby Lake) that combine its high-performance x86 cores with AMD's Radeon Graphics into the same processor package using Intel's own EMIB as well as HBM (2017). Intel canceled all the Kaby Lake-G products in October 2019. Fig. 6 shows the Agilex

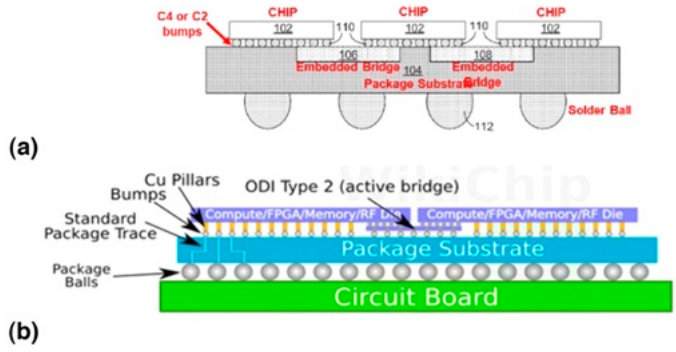

Fig. 4. (a) One of Intel's EMIB patents. (b) ODI (Type 2).

FPGA module. It can be seen that the FPGA and other chips are attached on top of a build-up package substrate with EMIB with fine-metal L/S/H RDLs. The TSV interposer is eliminated.

For EMIB, there are at least three important tasks (Fig. 7) namely: (1) wafer bumping of two different kinds of bumps on the chiplets wafer (but there are not bumps on the bridge); (2) embedding the bridge in the cavity of a build-up substrate and then laminating the top surface of the substrate; and (3) bonding the chiplets on the substrate with the embedded bridge.

A. Solder Bumps for Embedded Multidie Interconnect Bridge

It can be seen from Fig. 7 that there are two kinds of bumps on the chiplet, namely the C4 (controlled collapse chip connection) bumps and the C2 (chip connection or copper-pillar with solder-cap micro) bumps. Thus, wafer bumping of the chiplets wafer poses a challenge, but Intel has already taken care of this issue.

B. Fabrication of Embedded Multidie Interconnect Bridge Substrate

There are two major tasks in fabricating the organic package substrate with EMIB (Fig. 8). One is to make the EMIB, and the other is to make the substrate with EMIB. To make the EMIB, one must first build the RDLs (including the contact pads) on a Si-wafer. The way to make the RDLs depends on the line width/spacing of the conductive wiring of the RDLs. Finally, attach the non-RDL side of the Si-wafer to a die-attach film, and then singulate the Si-wafer.

To make the substrate with an EMIB, first place the singulated EMIB with the die-attached film on top of the Cu foil in the cavity of the substrate (Fig. 8a). It is followed by laminating a dielectric film on the whole organic package substrate. Then, drilling (on the dielectric film) and Cu plating to fill the holes (vias) to make connections to the contact pads of the EMIB. Continue Cu plating to make lateral connections of the substrate as shown in Fig. 8b. Then, it is followed by laminating another dielectric film on the whole substrate and drilling (on dielectric) and Cu plating to fill the holes and make contact pads (Fig. 8c). (Smaller pads on a finer pitch are for C2 bumps, while larger pads on a gross pitch are for C4 bumps.) The organic package substrate with an EMIB is ready for bonding of the chips as shown in Fig. 8d.

Today, the minimum metal L/S/H is 2/2/2 μm and the bridge size is from 2 × 2 mm to 8 × 8 mm [7], but most are equal and $<$5 × 5 mm [8]. The dielectric layer thickness is 2 μm. Usually, there are $\leqslant$4 RDLs. One of the challenges of the

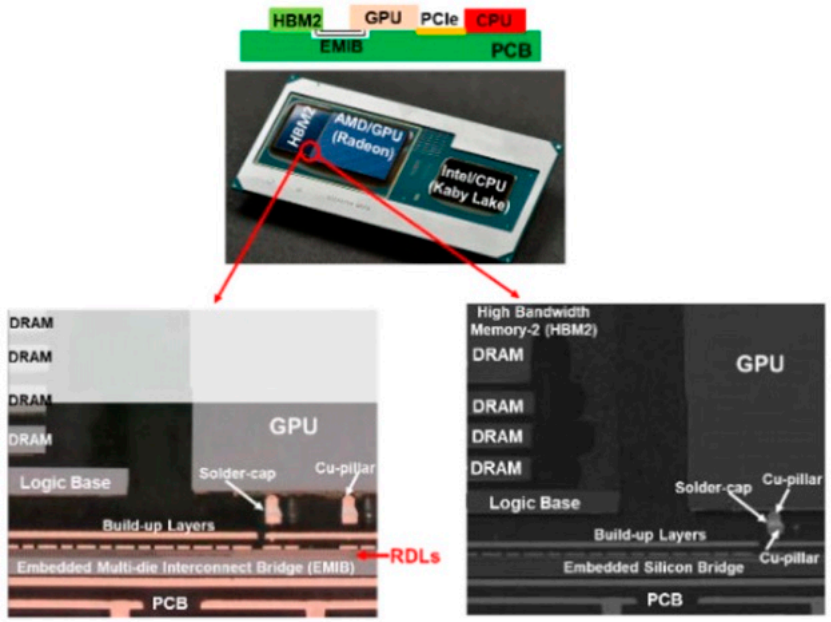

Fig. 5. Intel's Kaby Lake processor with AMD's Radeon graphics as well as HBM with EMIB.

EMIB technology is to fabricate the organic build-up package substrate with cavities for the silicon bridges and then laminate (with pressure and temperature) another build-up layer on top (to meet the substrate surface flatness requirement) for chiplets (with both C2 and C4 bumps) bonding. Intel and its suppliers are working toward high-yield manufacturing of the substrate.

C. *Bonding Challenges for Embedded Multidie Interconnect Bridge*

Intel published a paper at IEEE/ECTC 2021 [9] that pointed out the bonding challenges of chiplets:

1. Die bonding process.
2. Manufacturing throughput.
3. Die warpage.
4. Interface quality.
5. Die attach film material design.
6. Die shift.
7. Via-to-die-pad overlay alignment.
8. Integrated process considerations.

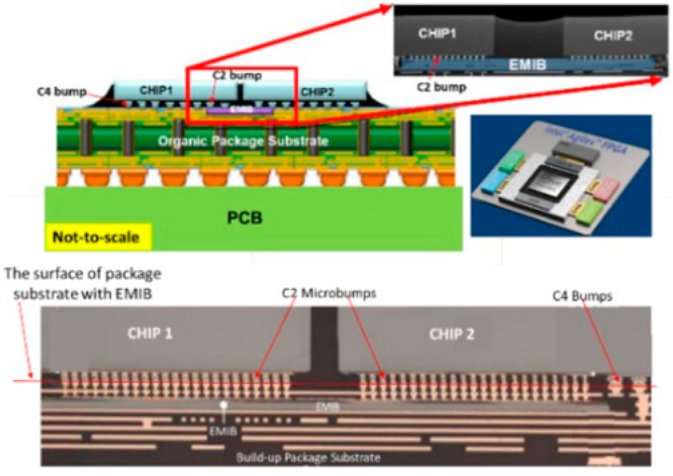

Fig. 6. Intel's Agilex FPGA with EMIB.

IBM's Direct Bonded Heterogeneous Integration

During IEEE/ECTC 2021 and 2022, IBM presented seven papers on "Direct Bonded Heterogeneous Integration (DBHi) Si Bridge" [10-16] (Fig. 9). The major differences between Intel's EMIB and IBM's DBHi are as follows:

1. For Intel's EMIB, there are two different bumps (C4 and C2) on the chiplets (and there are no bumps on the bridge)

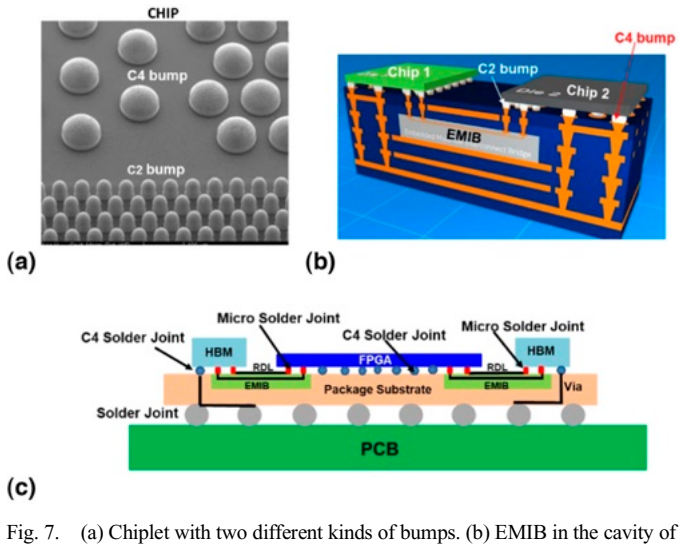

Fig. 7. (a) Chiplet with two different kinds of bumps. (b) EMIB in the cavity of a package substrate. (c) Schematic of a FPGA and HBMs with EMIBs.

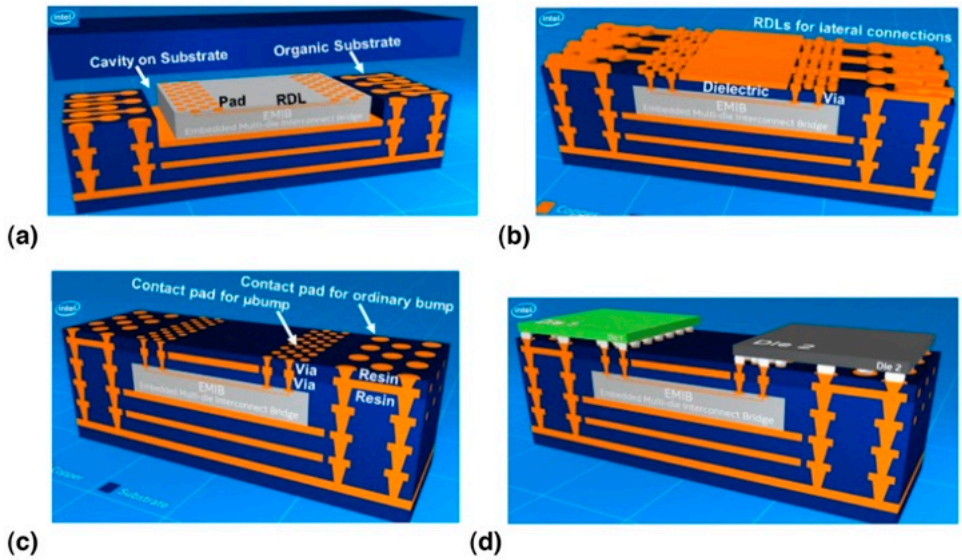

Fig. 8. (a) Attach the EMIB in the cavity of a build-up substrate. (b) RDL for lateral communications. (c) Contact pad for C4 and C2 bumps. (d) Chips mounted on the build-up substrate with EMIB.

(Fig. 7), while for IBM's DBHi, there are C4 bumps on the chiplets and C2 bumps on the bridge (Fig. 10a).

2. For Intel's EMIB, the bridge is embedded in the cavity of a build-up substrate with a die-attach material and then laminated with another build-up layer on top. Therefore, the substrate fabrication is very complicated as mentioned in section 5.3.2. For IBM's DBHi, the substrate is just a regular build-up substrate with a cavity on top as shown in Fig. 10b.

A. Solder Bumps for Direct Bonded Heterogeneous Integration

As shown in Fig. 10a, there are C2 bumps on the bridge. However, there are C4 bumps and Cu pads on the chiplet of the same wafer. Thus, wafer bumping post a challenge. IBM use a double lithography process to resolve this issue [10], which is shown in Fig. 11. It can be seen that the first lithography is used for making the UBM and metal pad, and the second

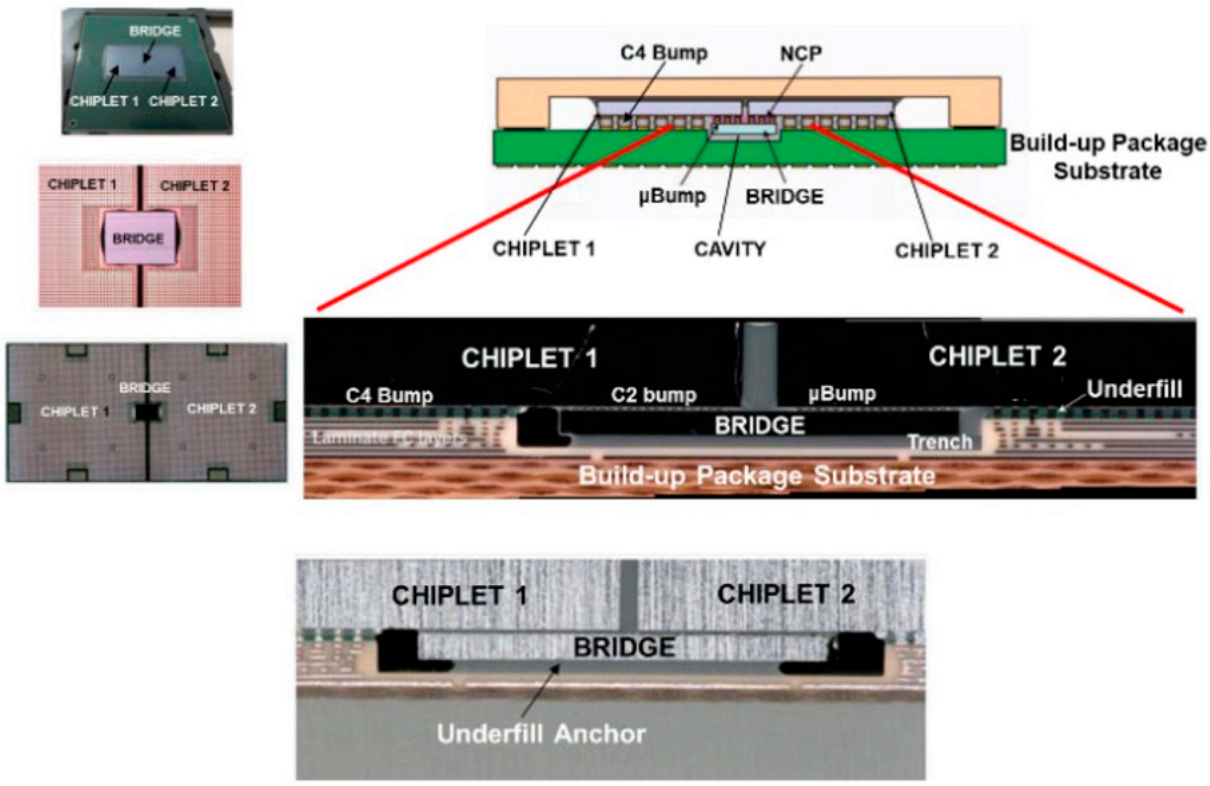

Fig. 9. IBM's DBHi.

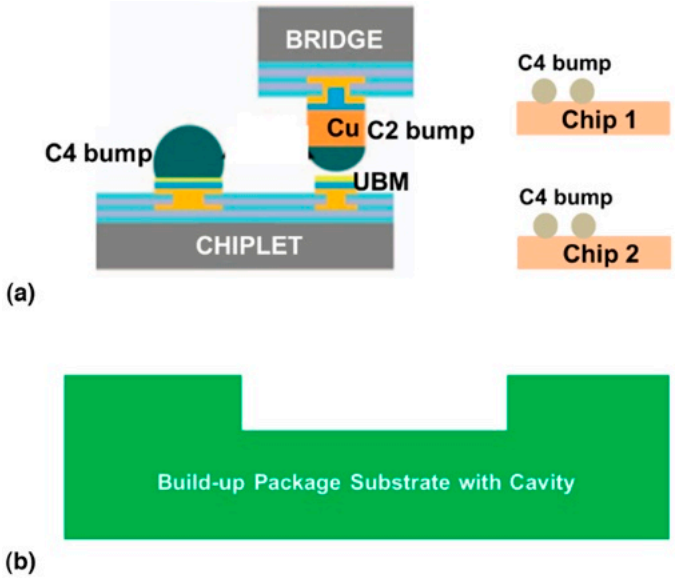

Fig. 10. IBM's DBHi. (a) C2 bumps on the bridge while C4 bumps on the chiplet. (b) Ordinary build-up package substrate with cavity.

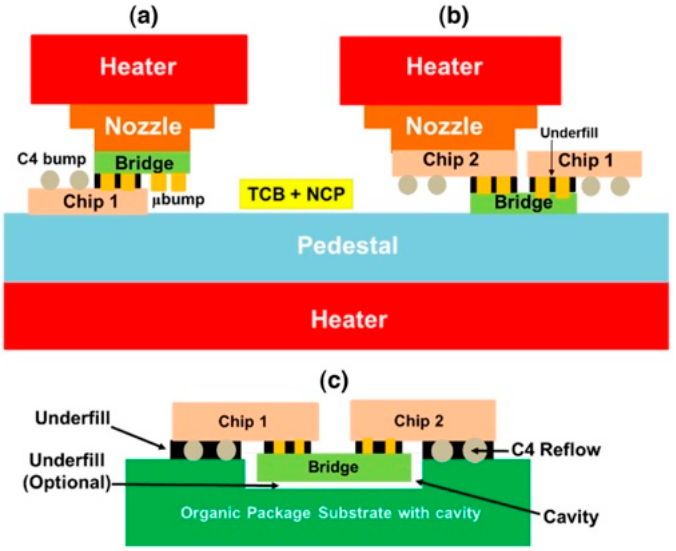

Fig. 12. DBHi bonding process. (a) TCB of the bridge die to Chip 1 with NCP. (b) TCB of the bridge die to Chip 2 with NCP. (c) C4 solder reflow of the Chip 1 and Chip 2 on the package with cavity and then underfill.

lithography is used to make the C4 bumps by injection molded solder (IMS) method.

B. Direct Bonded Heterogeneous Integration Bonding Assembly

The bonding assembly process of DBHi is very simple (Fig. 12). First, apply the nonconductive paste (NCP) on Chip 1. Then, bond the Chip 1 and the bridge with thermocompression bonding (TCB). After bonding, the NCP becomes the underfill between Chip 1 and the bridge. Then apply NCP on the bridge and bond Chip 2 and the bridge with TCB. Those steps are followed by placing the module (Chip 1 + bridge + Chip 2) on the organic substrate with a cavity and then going through the standard flip-chip reflow assembly process.

The stage temperature, bonding force, and bond-head temperature versus time during bonding are shown in Fig. 13. It can be seen that: (1) the bonding stage temperature (T_1) is small and kept at constant all the times; (2) the bond-head temperature consists of three stages; (i) at the first stage, the temperature (T_2) is larger than T_1, which is used to melt and flow the NCP: (ii) at the second stage, the temperature ($T_3 = 2T_1$) is the largest, which is used to reflow the solder; and (iii) at the final stage, the temperature (T_4) is $<$T2 and larger than T_1, which is used to solidify the solder joints.

The underfill under the bridge is optional. Fig. 9 shows the demonstration by IBM [9]. If the bridge is very thin, e.g., 50 μm and the C2 bump is very short, e.g., 30 μm, then the cavity of the package substrate is not needed if the C4 solder bump height is $>$85 μm as shown in Fig. 14.

In Horbe et al. and Chowehury et al. [15, 16], a detailed study on the TCB with NCP has been given. Fig. 15 shows the structure for simulation. It can be seen that there are two chiplets and one bridge as shown in Fig. 15a. Fig. 15b shows the zone-in of the one chiplet and the bridge. Fig. 16a schematically shows the cross section of the DBHi. During thermal cycling ($-25 \leftrightarrow 125$°C), due to the thermal expansion mismatch between the silicon chip (2.5×10^{-6}/°C) and the build-up

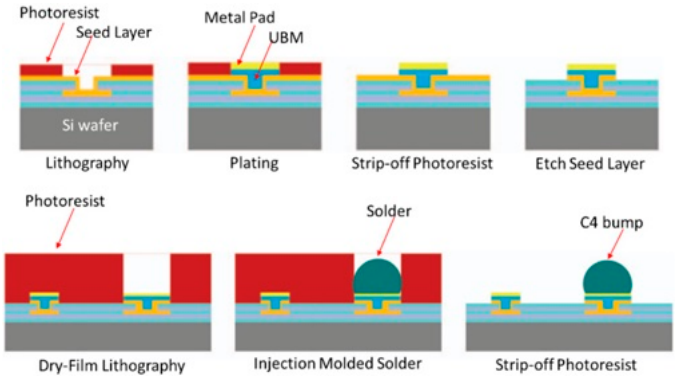

Fig. 11. IBM's double lithography process in making the C4 bumps and Cu pads.

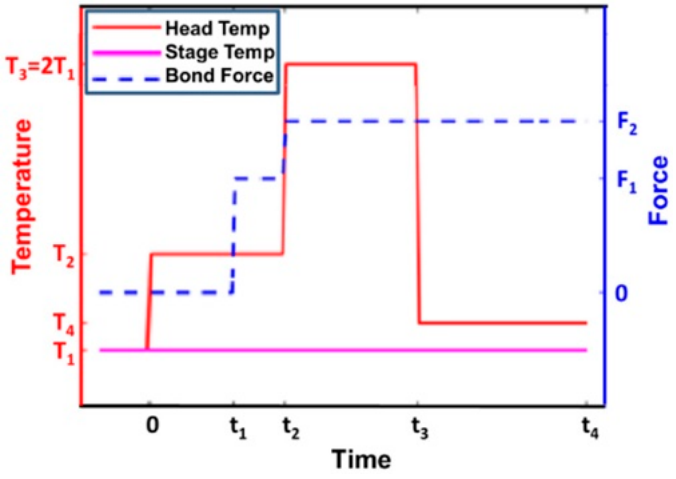

Fig. 13. DBHi TCB temperature-force-time profile.

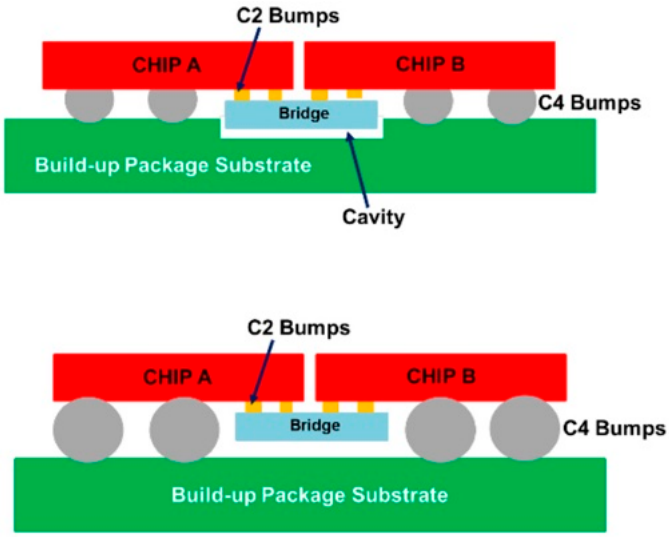

Fig. 14. DBHi options.

package substrate (18.5×10^{-6}/°C), the C4 bumps are subjected very large shearing stress as shown in Fig. 16b. Thus, underfill is needed to ensure the C4 solder joint reliability. The tensile stress is shown in Fig. 16c.

The test vehicle is shown in Fig. 17. It consists of an organic package substrate (laminate), a Si interposer, μC2 or μC4 bumps, and a Si chip. Apparently, the chip is for the chiplet, the Si interposer is for the bridge, and the organic laminate is for the build-up package substrate. Fig. 18a shows the solder joints with entrapped fillers while Fig. 18b shows the optimal solder joints without fillers. Fig. 19 shows the optimal solder joint cracks after thermal cycling test at 1,000 cycles (−55 ↔ 125°C).

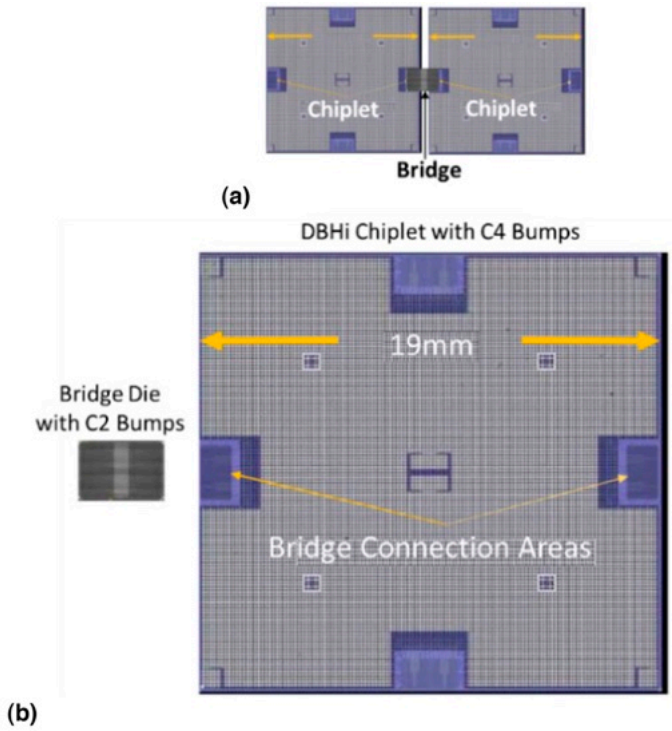

Fig. 15. DBHi structure for simulations. (a) Two chiplets and a bridge die. (b) Close-up of the structure.

C. Direct Bonded Heterogeneous Integration Underfilling

In Marushima et al. [13], IBM study the underfill flow characteristic of their DBHi structure. Fig. 20a schematically shows the side view and top view of the DBHi structure. In order to observe the flow of the underfill between the gaps by a high-speed camera, the material of all the key components is made of glass. Fig. 20b shows the underfill dispensing pattern.

The critical dimensional parameters to be studied are shown in Fig. 21. It can be seen that these parameters are: (1) the gap between the two chips; (2) the gap between the chips and the package substrate; (3) the gap between the bridge bottom and the package substrate cavity; (4) the gap between the bridge sidewall and the package substrate cavity; and (5) the gap between the module (chips + bridge) and the package substrate.

Fig. 22a shows the test vehicle to investigate the underfill flow characteristics between two glass substrates connected with C4 bumps. There are two different C4 bump heights: 49 and 85 μm. Fig. 22b shows the underfill dispensing characteristics. The dark areas are filled with underfill from the top view of the samples. It can be seen that: (1) the longer the times, the more underfills are filled; and (2) the larger the C4 bump heights, the more underfills are filled.

Fig. 23a shows another test vehicle to investigate the underfill flow characteristics between two chips. This is to study the effect of gap between the bridge sidewall to the cavity of the package substrate. Tow gaps are studied, 44 and 86 μm, and the C4 bump height of both chips is 50 μm.

Fig. 23b shows the underfill dispensing characteristics. The dark areas are filled with underfill from the top view of the samples. It can be seen that: (1) the larger the gaps between the bridge sidewall and the cavity, the larger the underfills filled; and (2) the longer the times, the more the underfills are filled.

D. Direct Bonded Heterogeneous Integration Challenges

The challenges in IBM's DBHi are:

1. Handling and bonding of a portion of the tiny rigid bridge on a portion of the large chiplet with very fine pitch pads.
2. Dealing with a situation in which there are more than one rigid bridge on a chiplet.
3. Dealing with a situation in which there are more than two chiplets on a package substrate.

University Sherbrooke/IBM's Self- Aligned Bridge

Université de Sherbrooke/IBM's self-aligned bridge is shown in Fig. 24 [17]. It can be seen that in this study, they are trying to use self-aligned method to assembly the bridge and the self-aligned structure is the V-groove opening of the bridge and Sn3Ag0.5Cu solder spheres. When the solder spheres reflow, the surface tension of the melted solder is supposed to pull (self-align) the bridge to the accurate position. In this study, the substrate is not an organic package substrate but a silicon substrate.

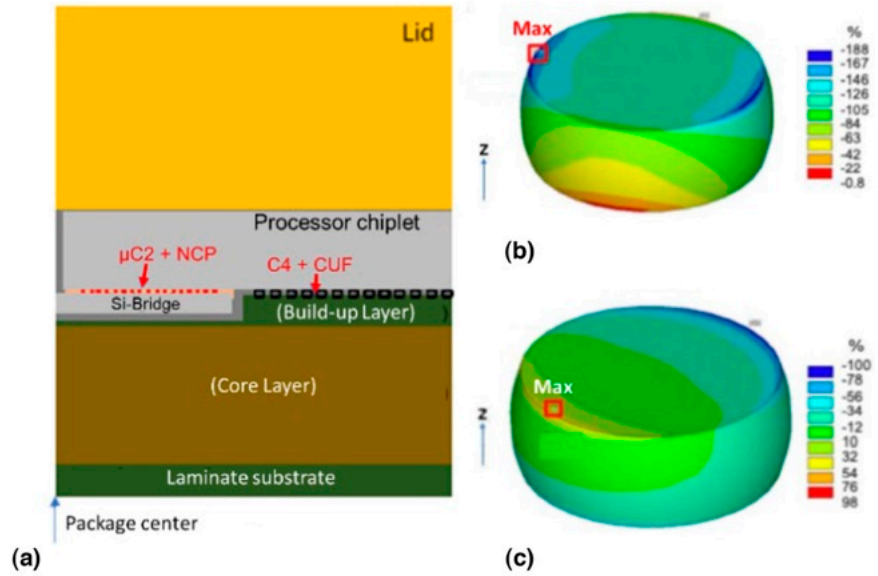

Fig. 16. (a) Close-up of the chiplet, bridge, C4 bump + underfill, and substrate. (b) Shear stress distribution in the C4 bump. (c) Tensile stress distribution in the C4 bump. (−25 ↔ 125°C).

A. Process Flow of the V-Groove Opening of the Self-Aligned Bridge

The V-groove opening process of the self-aligned bridge is shown in Fig. 25 [17]. First, fabricate the Cu-pillars on the top-side of a piece of silicon sample (3.35 × 2.5 × 0.2 mm) and then spin coat BrewerScience's Waferbond CR200 (65-μm thick) to cover the Cu posts and BrewerScience's Protek PSB to the backside of the sample (Figs. 25[1-3]). The CR200 is to protect the Cu posts from KOH etching bath and the ProTEK PSB is an alternative to SiO_2. It is followed by the photolithography exposure and development of hard mask layer (ProTEK PSB) (Fig. 25[4]). Then, wet etching in KOH bath of V-groove on the backside of the Si bridge and then removing the ProTEK PSB as shown in Figs. 25(5) and 25(6). It is followed by removing the CR200 and cleaning the sample (Figs. 25[7] and 25[8]).

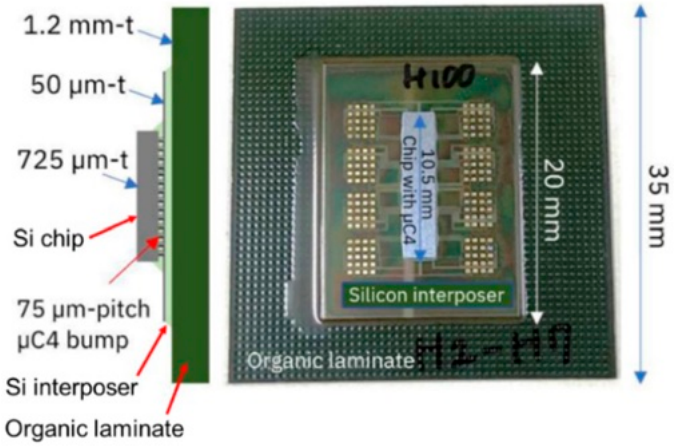

Fig. 17. DBHi test vehicle.

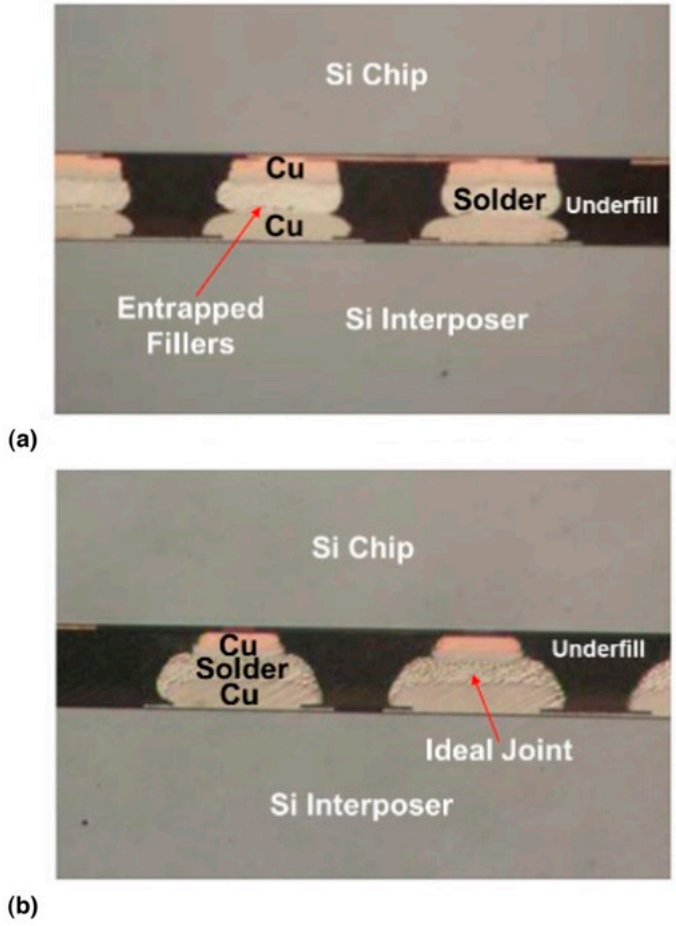

Fig. 18. DBHi TCB with NCP. (a) Solder joint with entrapped fillers. (b) Optimal solder joints.

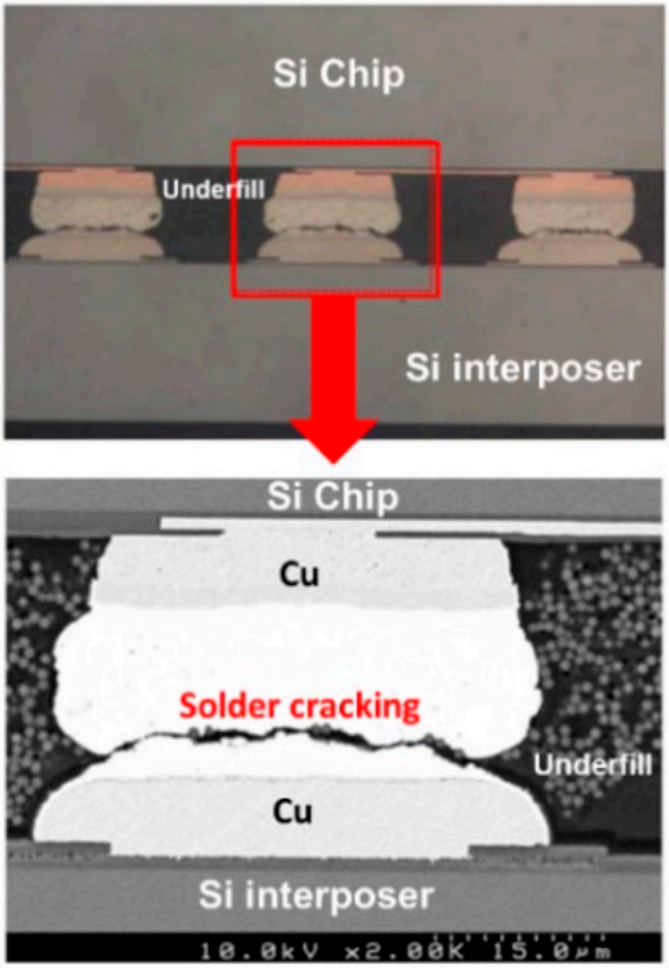

Fig. 19. Thermal cycling test results. Solder cracks at 1,000 cycles (−55 ↔ 125°C).

The mean height of the Cu posts is 39 μm before the V-groove opening and is 38.1 μm after. The mean diameter of the Cu posts is 37.1 μm before the V-groove opening and is 38.2 μm after.

The KOH etching bath conditions are: concentratio N = 32%, formulatio N = 400 mL 45% KOH solution + 160 mL DI water, total volume = 560 mL, temperature = 75°C, additive = 60 mL isopropanol, stirring (not applied), and duratio N = 45 min.

Fig. 26a shows the laser confocal microscopy image of the top-down view of the etched V-groove before the removal of ProTEK PSB. It can be seen that noticeable defects, such as: (1) undesired undercuts; (2) four round corners; and (3) slightly curved outlines in some regions. Fig. 26b shows the images of the etched V-groove after the removal of the ProTEK PSB. Fig. 26c shows the optical-laser 3-D top-down view of the etched V-groove after the removal of the ProTEK PSB and it can be seen that there are some tiny dents on the sidewall, but generally it is smooth.

The SAC305 solder spheres with an average diameter equals to 102 μm are shown in Fig. 27a. The Cu bonding pad (101.5 μm) with NiAu finishing on a silicon substrate for the solder sphere is shown in Fig. 27b. The reflow temperature profile with a peak temperature equals to 260°C is shown in Fig. 28. The assembly of the bridge (with Cu posts on its topside and V-groove at its bottom side) and the silicon substrate are shown in Fig. 29 (the central portion of the assembly is not shown). The L shape is for alignment purposes. Underfill has been applied between the gap of the bridge and substrate.

B. *Measurement Results*

The measurement results show that: (1) the rotation of the Si bridge with respect to the silicon substrate is very small (0.001°); (2) the Si bridge shift merely 2.5 ± 0.9 μm in the short dimension; and (3) the Si bridge shift 9.5 ± 2.2 μm in the long dimension.

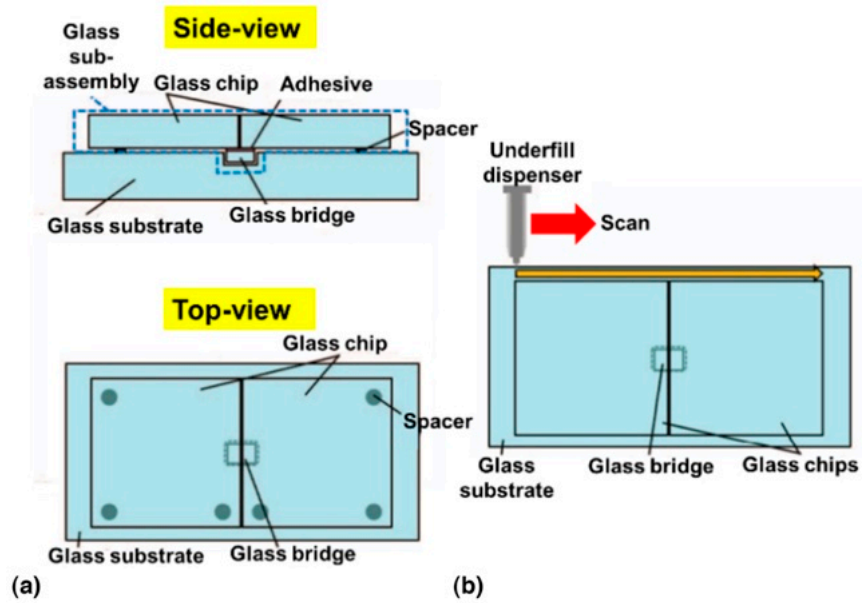

Fig. 20. (a) Glass mock-up for a DBHi structure. (b) The underfill dispense pattern.

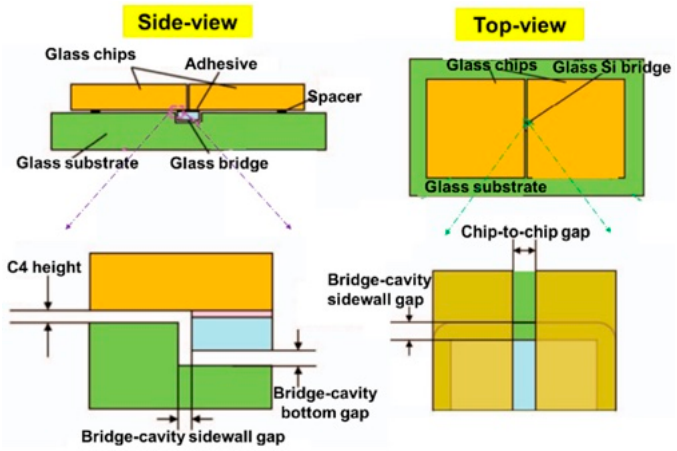

Fig. 21. Critical dimensional parameters of the underfill flow in the DBHi structure.

C. Challenges of Self-Aligned Bridge

The most challenge of self-aligned bridge is the vertical variation between the Cu posts of the Si bridge and the top surface of the Si substrate, which has not been discussed in the paper. The flatness of the surface (from the Cu posts of the Si bridge and from the Si substrate) is the most important factor for the high-yield assembly of chips bonding.

Patents on Rigid Bridges with Fan-Out Packaging

Intel's and IBM's rigid bridges are either embedded in or are on an organic package substrate. There is another class of rigid bridge, which is embedded in the fan-out EMC and/or connected to the fan-out RDL substrate. On May 12, 2020, Applied Materials obtained the U.S. patent 10,651,126 [18]. The company's design embedded the bridge in EMC by the fan-out chip (bridge) first and die face-up process (Fig. 30). This could be the very first patent of a rigid bridge embedded in fan-out EMC. On May 7, 2021, and on June 21, 2022,

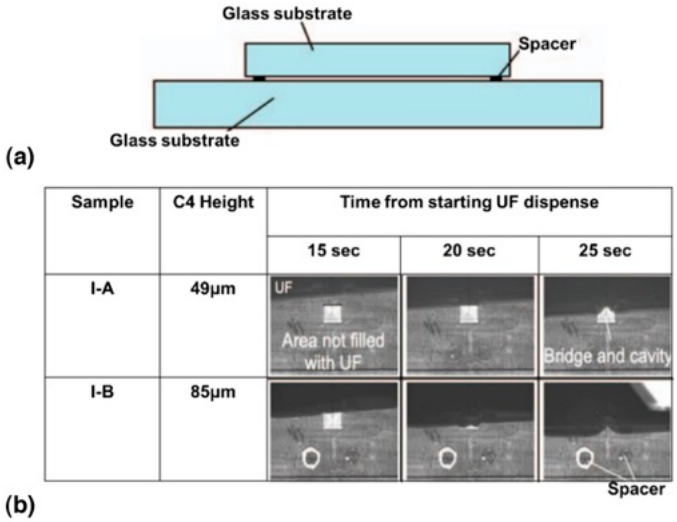

Fig. 22. (a) Test vehicle. (b) Underfill flow characteristics for different C4 bump heights.

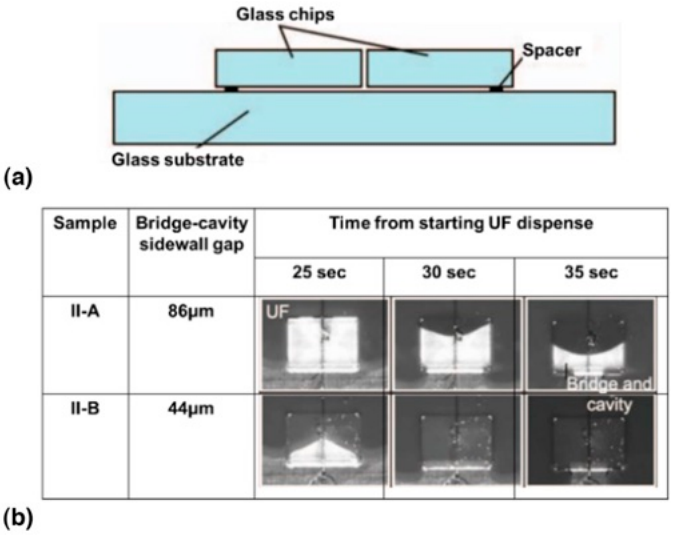

Fig. 23. (a) Test vehicle. (b) Underfill flow characteristic for different bridge-cavity sidewall gaps.

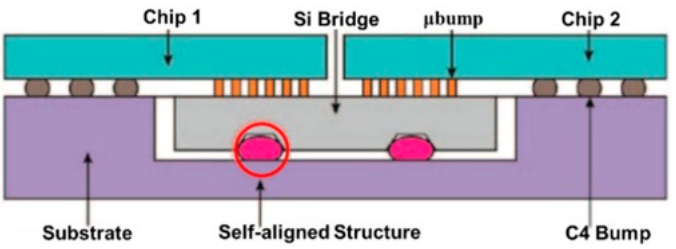

Fig. 24. Self-aligned structure in an embedded bridge in the cavity of package substrate.

Unimicron obtained the Taiwan patent TW 1,768,874 [19] in which the bridge is embedded in the fan-out EMC by the chip (bridge) first and die facedown process (Fig. 31). For the patent on rigid bridge embedded in the EMC and connected to the RDL substrate by the chip (bridge) last or RDL-first fan-out process, please see IME US 11,018,080 (May 25, 2021) (Fig. 32) [20].

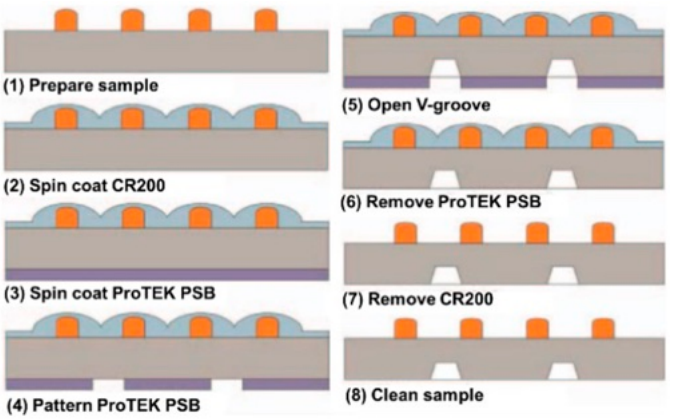

Fig. 25. Process flow of the self-aligned bridge.

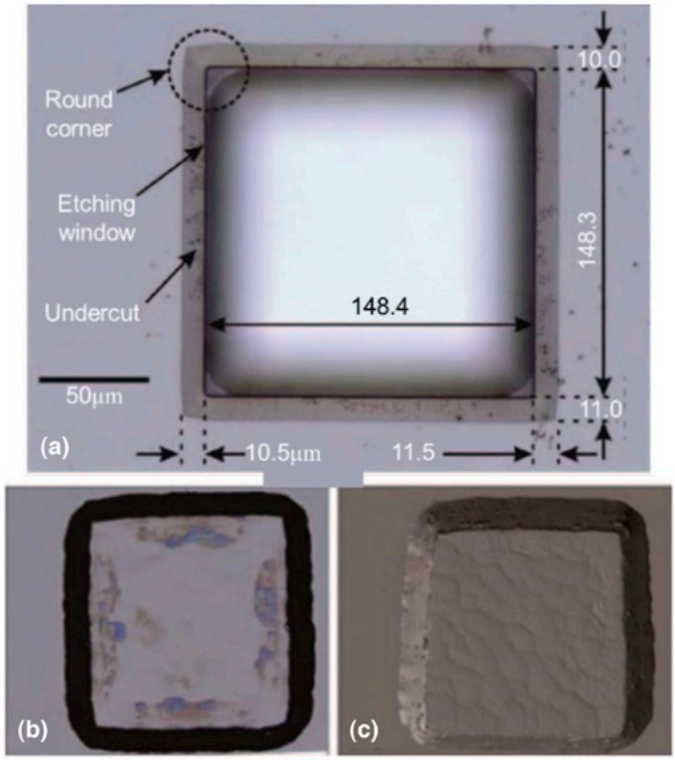

Fig. 26. (a) Top view of the V-groove before the removal of ProTEK PSB. (b) Top view of the V-groove after the removal of ProTEK PSB. (c) 3-D optical-laser view of the V-groove after the removal of the V-groove.

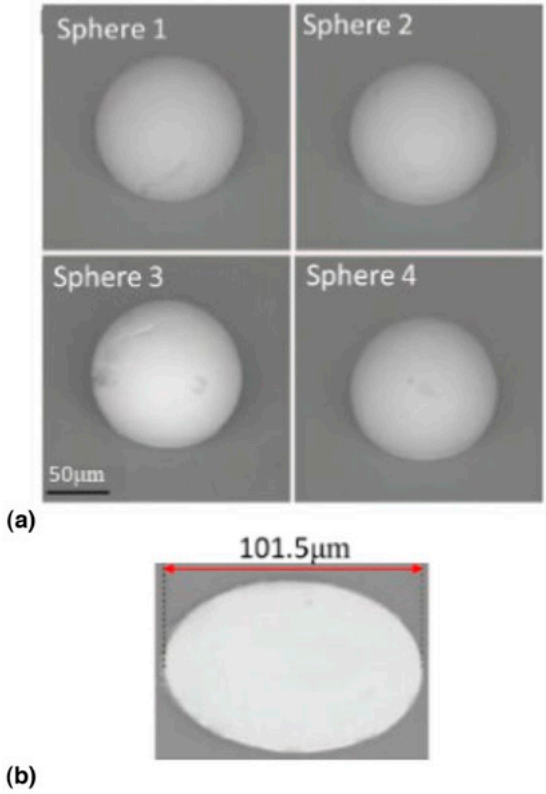

Fig. 27. (a) Top view of the SAC solder spheres. (b) Pad geometry.

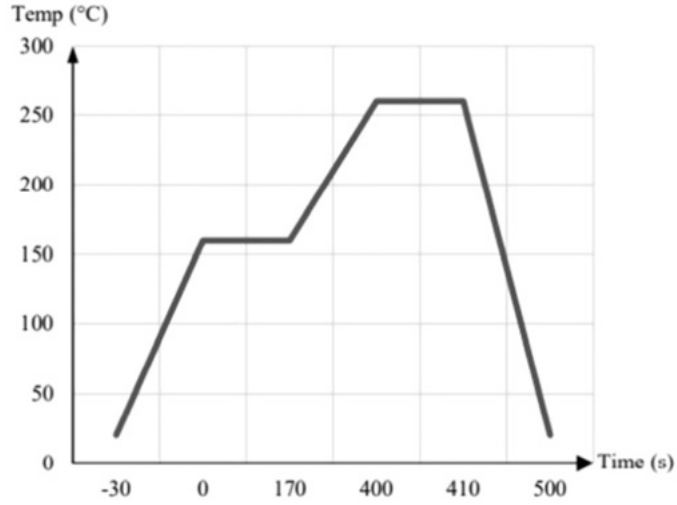

Fig. 28. Lead-free reflow temperature profile.

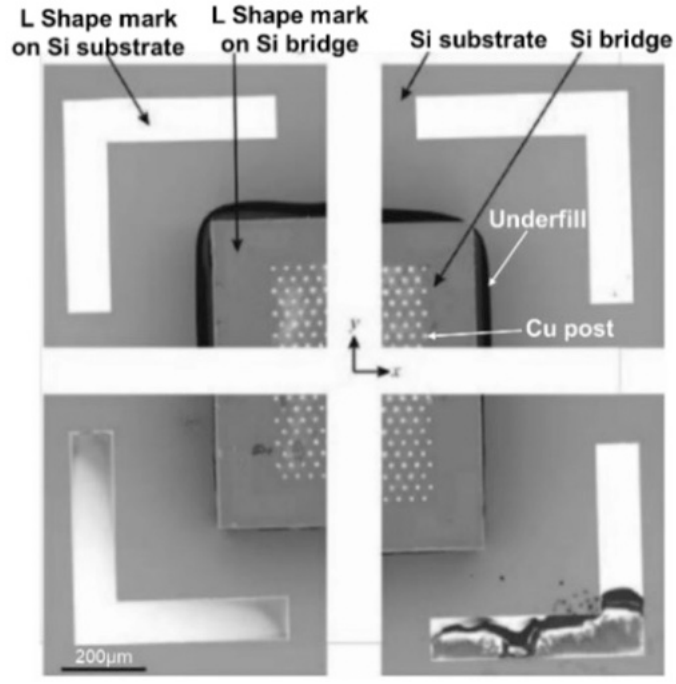

Fig. 29. SEM images of the four corners of the final stack. Alignment (L shape) mark is on the bridge as well as on the substrate.

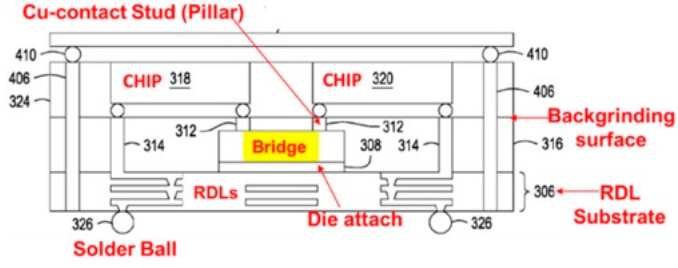

Fig. 30. Applied Materials' bridge patent with fan-out chip (bridge) first and die face-up process (US 10,651,126).

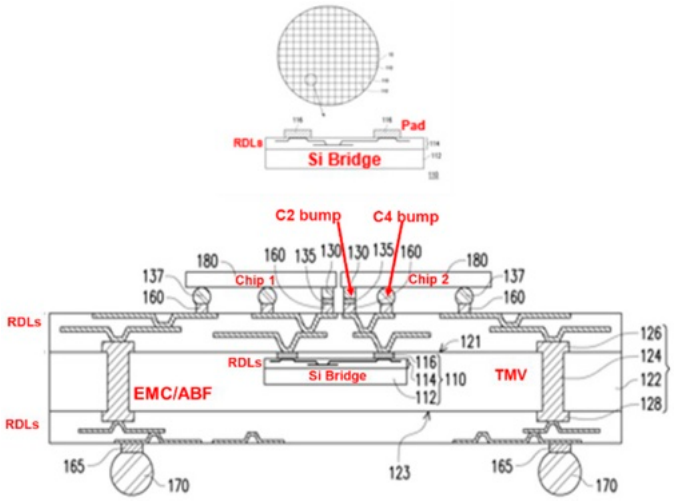

Fig. 31. Unimicron's bridge patent with fan-out chip (bridge) first and die facedown process (US 11,410,933).

TSMC's Local Silicon Interconnect

On August 25, 2020, during TSMC's Annual Technology Symposium, the company announced its local silicon interconnect (LSI) technology for chiplet lateral communication. The integrated fan-out LSI (InFO_LSI) is schematically shown in Fig. 33a and the CoWoS_LSI is shown in Fig. 33b.

SPIL's Fan-Out Embedded Bridge and Fan-Out Embedded Bridge with Through Silicon Vias

During IEEE/ECTC and IEEE/EPTC 2020-2022, SPIL published at least five papers on bridges embedded in EMC and connected to RDL substrate [21-25]. They called it fan-out embedded bridge (FO-EB) and FO-EB with TSV (FO-EB-T).

A. Fan-Out Embedded Bridge

Fig. 34 shows the FO-EB by SPIL [21-24]. It can be seen that the SoC is connected to the HBM with the embedded silicon bridge die. The silicon bridge die is embedded in an EMC and is connected to the RDL.

The assembly process is shown in Fig. 35. It can be seen that on the temporary glass carrier, they first build the RDL1, Cu-pad, and electroplate the Cu post, and then attach the bridge

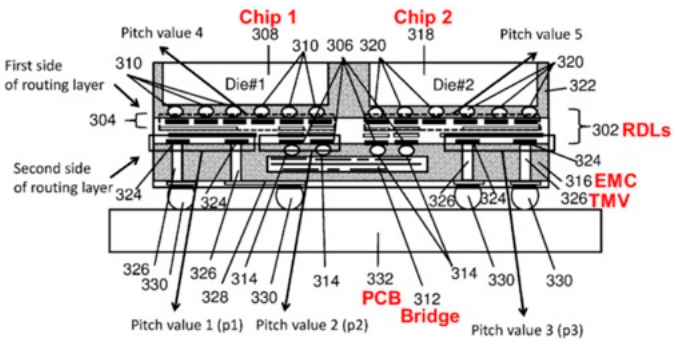

Fig. 32. IME's bridge patent with fan-out chip (bridge) last or RDL-first process (US 11,018,080).

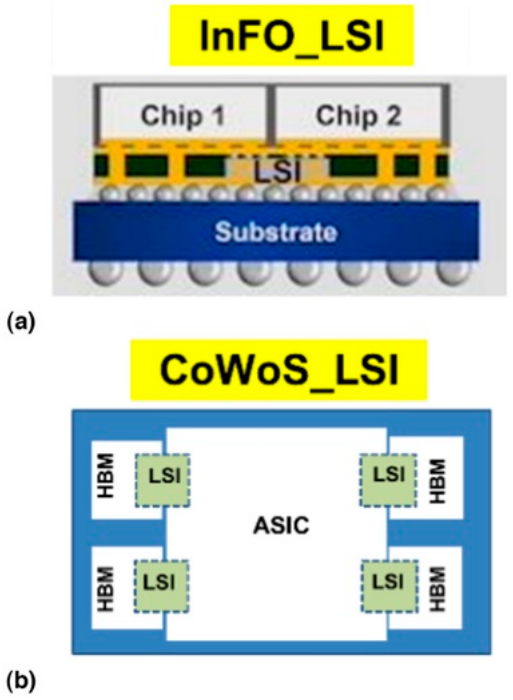

Fig. 33. (a) TSMC's InFO-LSI. (b) CoWoS-LSI.

die on the RDL1 (Fig. 35a). It is followed by molding and grinding to expose the Cu posts (Fig. 35b). Then, fabricate RDL2 and the micropads (Fig. 35c). It is followed by SoC and HBM bonding on RDL2 and then molding (Fig. 35d). Then remove the temporary glass carrier and C4 bumping (Fig. 35e). Finally, flip-chip assembly the module on a package substrate (Fig. 35f). A typical cross section SEM image of the FO-EM is shown in Fig. 30. The bridge, SoC, HBM, μbump, RDL1, and RDL2 are clearly seen.

A test vehicle of FO-EB is shown in Fig. 36. It can be seen that the fan-out RDL2 is supporting the graphics processing unit (GPU) and the four HBMs on its topside and the four inter connect dice (ICDs) or bridges on its bottom side. The whole module is attached on a build-up package substrate. The maximum

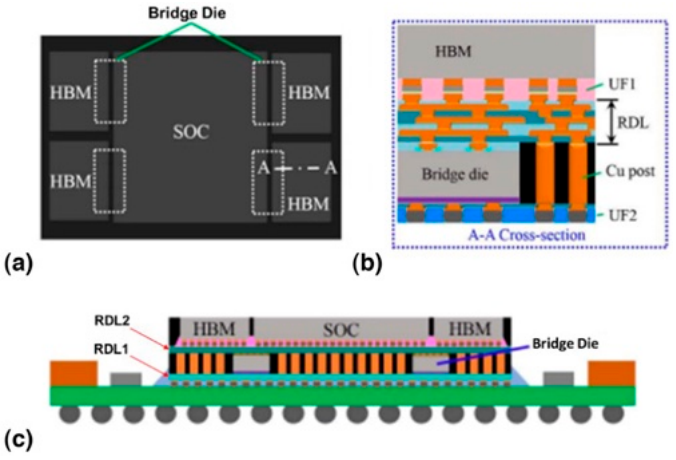

Fig. 34. SPIL's FO-EB. (a) SEM image of FO-EB. (b) Schematic of FO-EB. (c) Schematic of the FO-EB structure.

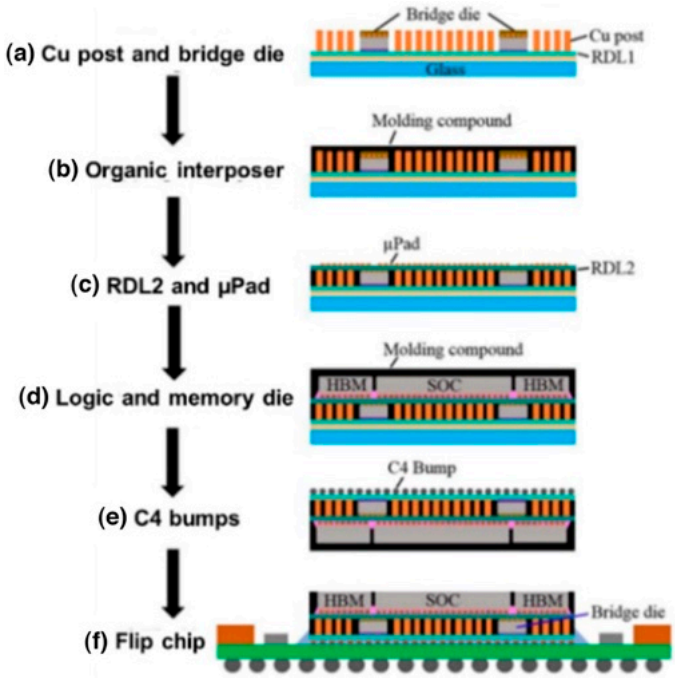

Fig. 35. Process flow of FO-EB.

bridge die size is 36 mm^2. The module size is 30 × 45 mm and the package size is 70 × 80 mm.

Fig. 37 shows the SEM images of some critical areas. Fig. 38(1) shows the interface between the SoC and the HBM. Fig. 38(2) shows fan-out RDL2 with the Cu-stud of the GPU on its topside and the bridge with µbump on its bottom side. Fig. 38(3) shows the bridge. Fig. 38(4) shows a couple of the through interconnect vias (TIY) and Fig. 38(5) shows the underfill. All these images demonstrate the key components are properly done.

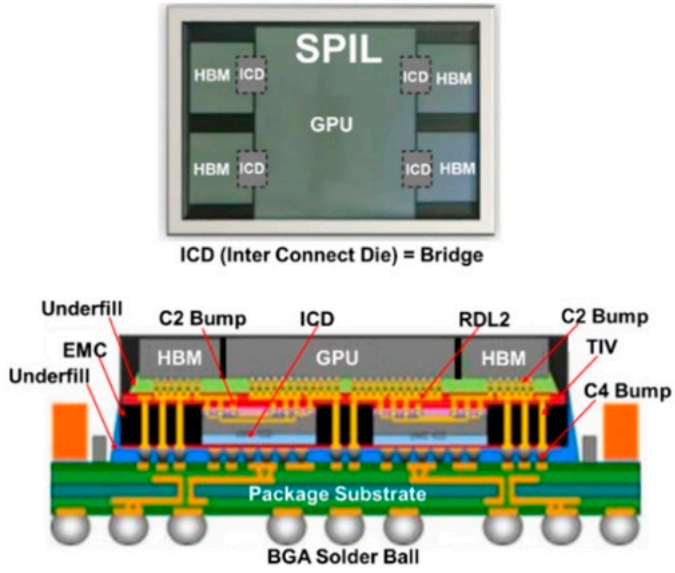

Fig. 36. Test vehicle of FO-EB.

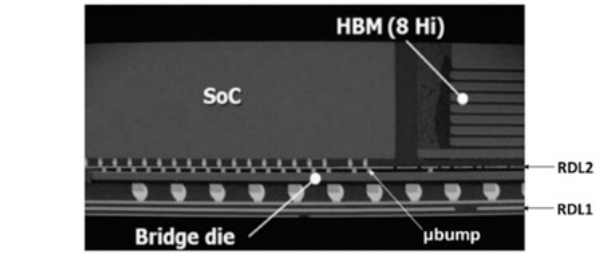

Fig. 37. SEM image of the FO-EB.

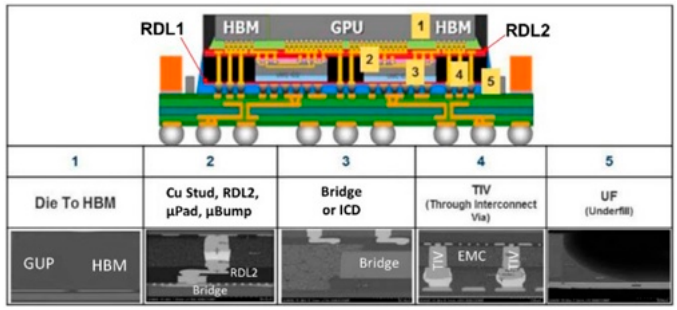

Fig. 38. Details of the FO-EB.

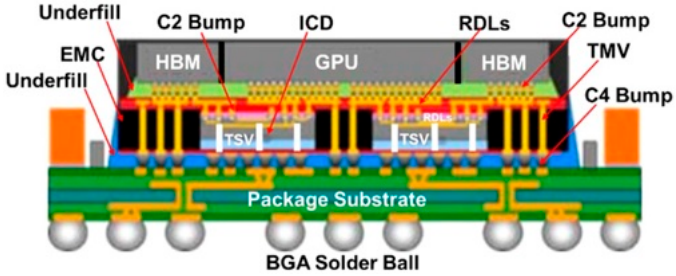

Fig. 39. SPIL's FO-EB-T.

B. Fan-Out Embedded Bridge with Through Silicon Vias

Fig. 39 shows the schematic of the FO-EB-T [25]. It can be seen that the key difference between the FO-EB and the FO-EB-T is that there are TSVs in the bridge of the FO-EB-T as shown in Fig. 40. The assembly process of the FO-EB-T is

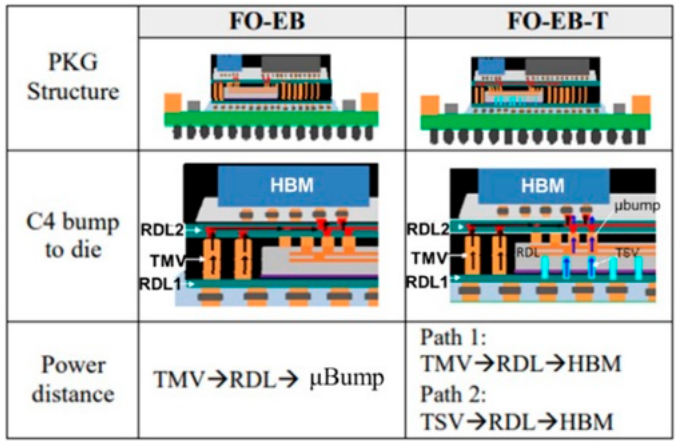

Fig. 40. Comparison between FO-EB and FO-EB-T.

Table I
Electrical Comparison Between FO-EB and FO-EB-T

Platform		2.5D	FO-EB	FO-EB-T
Configuration			SoC + HBM	
RDL layer, L/S		4 L, 0.4/0.4 μm	1 L, 10/10 μm	1 L, 10/10 μm
Bandwidth		Baseline	Lower	Lower
SoC to HBM	RC delay	Baseline	Lower	Lower
SoC to C4 bump	DCR (power)	Baseline	Higher	Same as baseline
SoC to solder ball	Insertion loss (1 GHz)	Baseline	Lower	Lower

exactly the same as that of the FO-EB, except while fabricating the RDLs on the silicon wafer, the TSVs should also be fabricated.

The electrical performances among FO-EB-T, FO-EB, and 2.5 IC integration are shown in Table I. It can be seen that; (1) for SoC and HBM construction, the electrical simulation is performed by resistive-capacitive (R-C) delay from the SoC to the HBM; (2) for SoC and C4 bump construction, the simulation is performed by direct current resistant (DCR) from the SoC to C4 bump; and (3) for SoC and solder ball construction, the simulation is performed by the insertion loss from the SoC to solder ball.

The simulation results of the 2.5D are to be taken as the baseline and some of the results are summarized in Table I. It can be seen that the R-C delay and insertion loss of FO-EB and FO-EB-T are lower (better) than that of 2.5D. This is because of the wider line width and spacing of the RDL of the FO-EB and FO-EB-T. The DCR of FO-EB is higher than that of 2.5D because the power transmission by TIV is poorer than that of TSV. On the other hand, the DCR of FO-EB-T (the bridge with TSVs) is the same as the 2.5D IC integration. The simulation result shows [25] that because of the bridge with TSVs, there are 55% resistance improvement.

ASE's sFOCoS

A. The Structure and Process of Si Bridge Fan-Out Chip on Substrate

Fig. 41 shows the bridge embedded in EMC and connected to fan-out RDLs, which is called stacked Si bridge fan-out chip on substrate (sFOCoS) [26]. It can be seen that the fan-out (L/S = 10/10 μm) RDLs are supporting the one ASIC and one HBM on its topside and the (L/S = 0.8 μm) Si bridge die (6 × 6 mm) at its bottom side.

The assembly process is shown in Fig. 42. First, separately, prepare the temporary glass wafer carrier and bridges with μbumps from a silicon wafer. Then attach the bridge with μbumps to the wafer carrier and electroplate the Cu posts from the wafer carrier. It is followed by EMC molding of the whole wafer carrier, grinding the EMC to expose the Cu post, and fabricating the RDLs. Then attach the ASIC and HBMs on the RDLs and mold the EMC. It is followed by removing the temporary glass wafer carrier, mounting the C4 bumps, and dicing the reconstituted wafer into individual module (27 × 14 mm). Finally, attach the module to a package substrate (40 × 30 mm) and underfilled. This process is very similar to SPIL's.

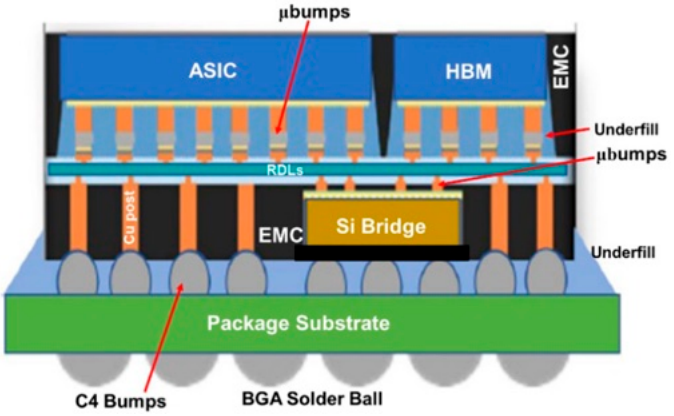

Fig. 41. ASE's sFOCoS.

B. The Structure and Process of Fan-Out Chip on Substrate Chip-Last

Fig. 43 shows a schematic of ASE's FOCoS- chip-last (CL). It can be seen that one ASIC and two HBMs are supporting by a fan-out chip-last (or RDL-first) four-layer (L/S = 2/2 μm) RDL with μbumps, which is connected to a build-up package substrate (47.5 × 47.5 mm) with C4 bumps. The process flow is shown in Fig. 44. It can be seen that, first fabricate the RDLs

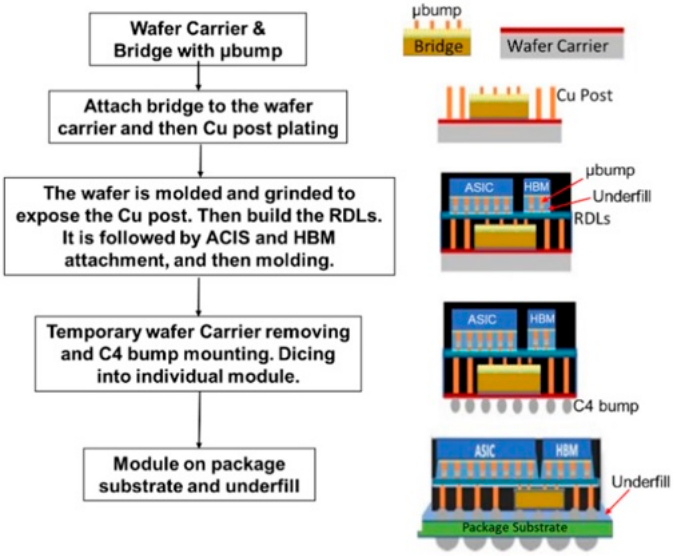

Fig. 42. Process flow of sFOCoS.

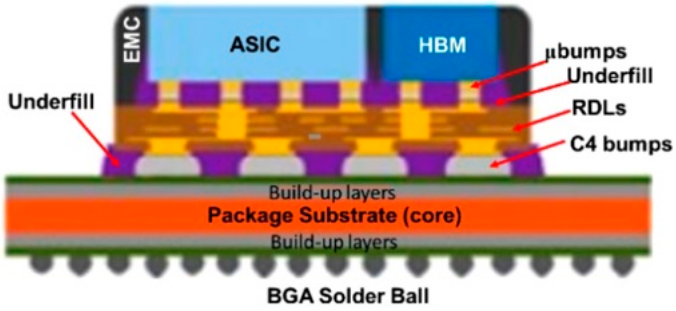

Fig. 43. Schematic of ASE's FOCoS-CL.

on a temporary glass wafer carrier. It is followed by attaching the ASIC and HBM on the RDLs, molding the EMC, removing the temporary carrier, and mounting the C4 bumps. Then back-grind the EMC and dicing the reconstituted wafer into individual module (30 × 28 mm). Finally, attach the individual module to a package substrate.

C. *Reliability and Warpage Between Si Bridge Fan-Out Chip on Substrate and Fan-Out Chip on Substrate Chip-Last*

The reliability and warpage comparing between the sFOCoS and FOCoS-CL is shown in Fig. 45. Fig. 45a shows the JEDEC standard reliability test results. It can be seen that for all the tests, the performances of the FOCoS are better than those of the sFOCoS. One of the key reasons could be the existing of the Si bridge (2.5×10^{-6}/°C), which is very close to the organic package substrate (18.5×10^{-6}/°C). Nevertheless, both FOCoS-CL and sFOCoS passed all the reliability tests.

Fig. 45b shows the warpage comparison between the FOCoS-CL and sFOCoS. The temperature profile is the lead-free soldering reflow profile: from room temperature to peak temperature (260°C) and then return to room temperature. First of all, the overall warpages between the FOCoS-CL and sFOCoS are very close and in the acceptable range. Near at room temperature, the warpage of the sFOCoS is slightly lower than that of the FOCoS-CL, while near at peak temperature, the warpage of the sFOCoS is higher than that of the FOCoS-CL.

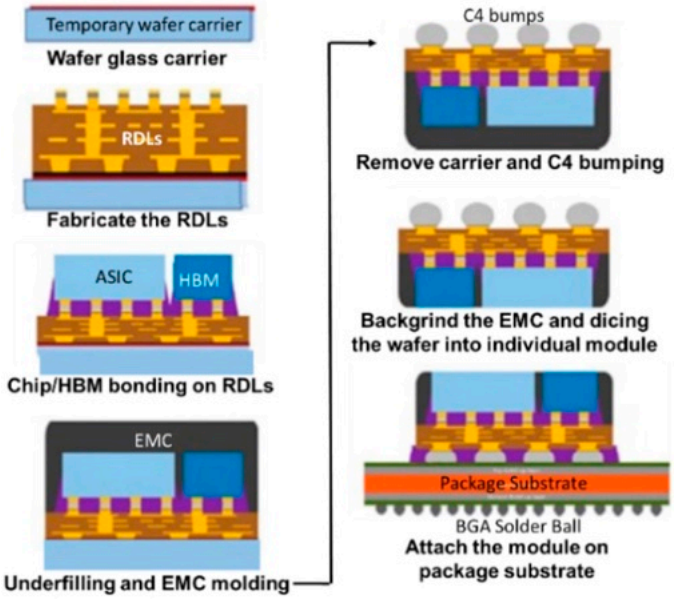

Fig. 44. Process flow of FOCoS-CL.

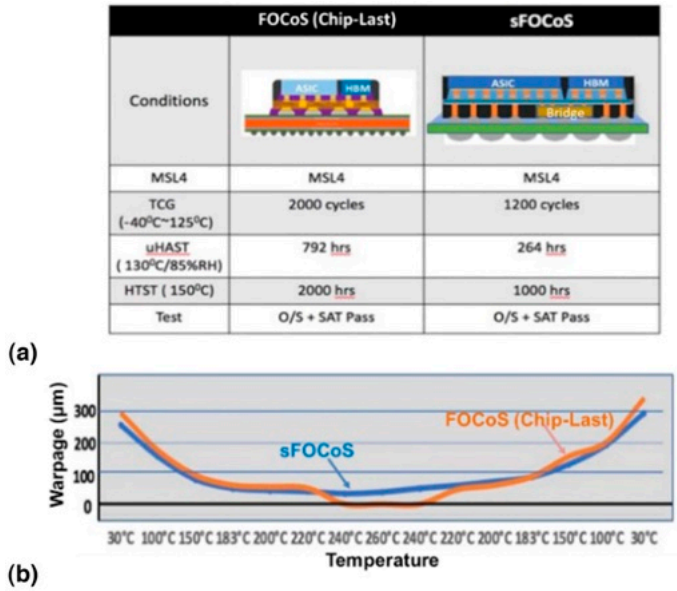

Fig. 45. Comparison between FOCoS-CL and sFOCoS. (a) Reliability tests. (b) Warpage.

Amkor's S-Connect

Figs. 46 and 47 show the schematic of Amkor's embedded bridge in EMC and connected to a fan-out RDL substrate called S-connect [27]. It can be seen that the fan-out RDL is supporting the ASIC and HBM on its topside and the bridge and some integrated passive devices (IPD) at its bottom side. Their bridge can be either the ordinary Si bridge made from a silicon wafer (Fig. 46), or a molded RDL bridge die made from fan-out packaging as shown in Fig. 47. Thus, there are two different S-connects, one is with the ordinary Si bridge (Fig. 46) and the other is with the molded RDL bridge (Fig. 47).

A. *S-Connect with Si-Bridge*

The S-connect with Si-bridge is shown in Fig. 46. The assembly process of the key components is also shown in Fig. 48. First, separately: (1) fabricate the RDL on a temporary wafer

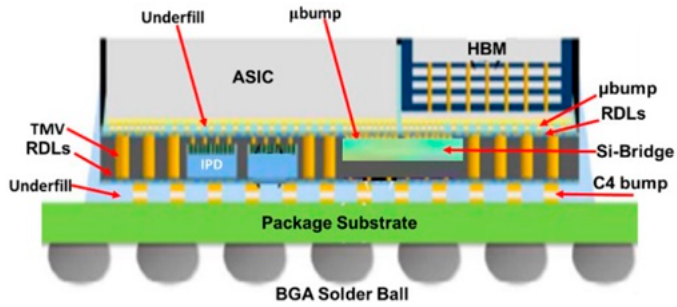

Fig. 46. Amkor's S-connect with Si-bridge.

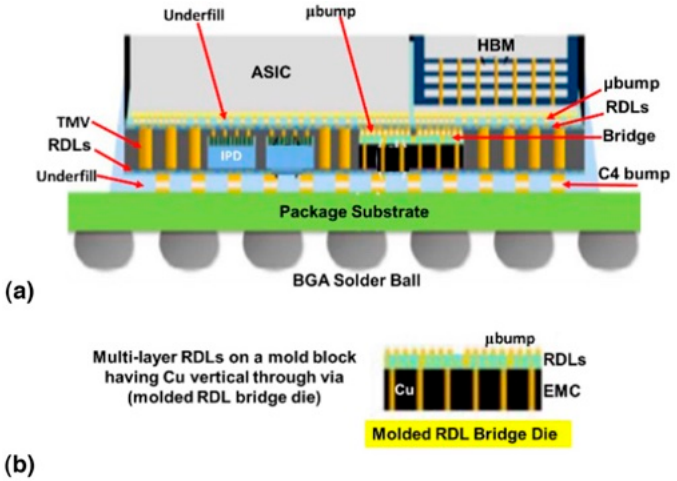

Fig. 47. Amkor's S-connect with molded RDL bridge die.

glass carrier; (2) wafer bumping of the ASIC and HBM and then singulation; (3) fabricate the Si-bridge with µbumps and then singulation; and (4) fabricate the IPD with µbumps and then singulation. Then, assembly all the key components into a module shown in the right-hand side of Figs. 46 and 48. The SEM image of the S-connect cross section with Si-bridge is shown in Fig. 49.

B. S-Connect with Molded Redistribution Layers-Bridge

The S-connect with molded RDL bridge is shown in Fig. 47. The assembly process of the key components is also shown in Fig. 48. First, separately: (1) fabricate the molded RDL bridge on a mold block having Cu vertical through via as shown in Fig. 47b; (2) wafer bumping of the ASIC and HBM and then singulation; (3) fabricate the Si-bridge with µbumps and then singulation; and (4) fabricate the IPD with µbumps and then singulation. Then assembly all the key components into a module as shown in the left-hand side of Figs. 47 and 48. The SEM image of the S-connect cross section with molded RDL bridge is shown in Fig. 50.

IME's Embedded Fine Pitch Interconnect

Fig. 51 shows the embedded bridge in EMC and connected to fan-out RDL called embedded fine pitch interconnect (EFI) [28]. It can be seen that RDL layer is supporting the ASIC, HBM, and SERDES on its topside and the Si-bridge on its bottom side. The whole module is attached to a PCB.

A. Process Flow of Embedded Fine Pitch Interconnect

The fabrication process flow is shown in Fig. 52. It can be seen that the RDL is first fabricated on a temporary glass wafer carrier with a sacrificial layer (Figs. 52a and 52b). It is followed by electroplating the Cu posts and attaching the Si-bridge on the RDL (Figs. 52c and 52d). Then, mold the EMC on the whole wafer, backgrind the EMC to expose the Cu post, and make isolation layer and UBM (Figs. 52e and 52f). It is followed by removing the temporary carrier by laser debonding and cleaning, solder ball mounting, and singulating into individual unit (Figs. 52g and 52h). Then attach the ASIC and memory on the individual unit (a module) and finally attach the individual module to a PCB (Fig. 52i). Fig. 53 shows some of the image of a test vehicle of the EIF. It can be seen that the RDL is supporting one ASIC and two HBMs and the Si bridge.

B. Thermal Performance of Embedded Fine Pitch Interconnect

Because of the Cu posts and the module is directly attached to the PCB (better thermal conductivity and shorter heat path), the thermal performance should be very good, even the module is consisted of EMC. Fig. 54 shows the thermal performance comparison between a 2.5D IC integration and the EFI structure. It can be seen that the thermal performance of the EFI structure is better than that of the 2.5D structure.

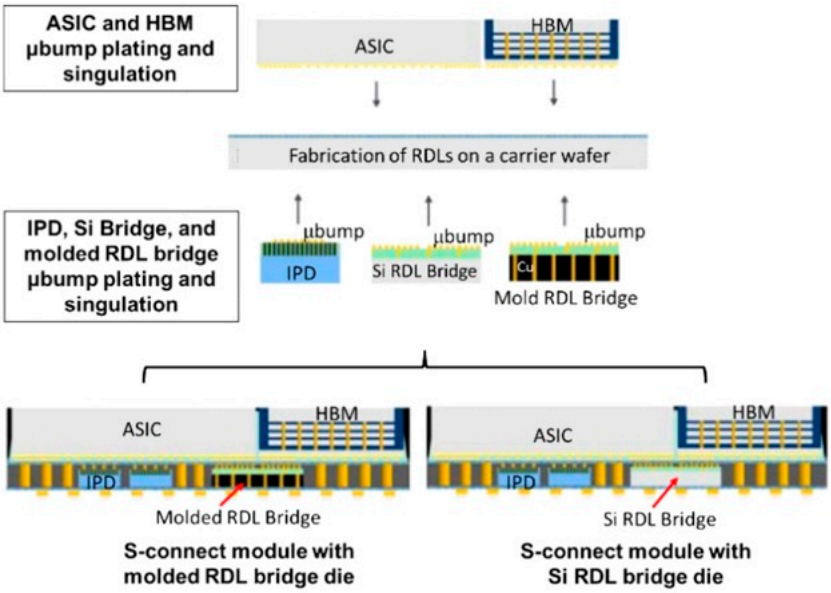

Fig. 48. Process flow of S-connect with Si-bridge and molded RDL bridge.

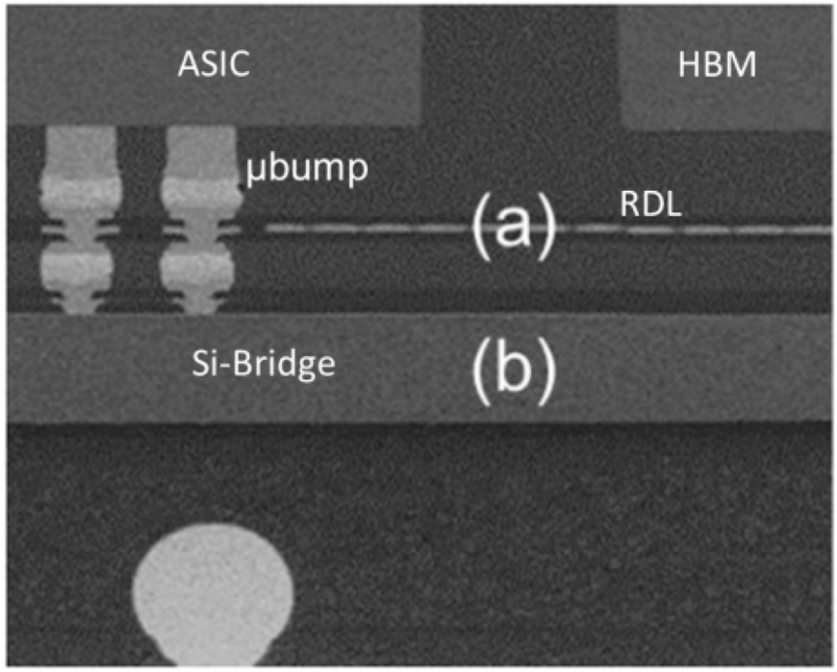

Fig. 49. SEM images of S-connect with Si-bridge.

IMEC'S BRIDGE

Fig. 55 shows imec's bridge [29, 30]. It can be seen that imec proposed the use of the bridges + fan-out wafer-level packaging (FOWLP) technology to interconnect the logic chip, wide I/O DRAM, and the flash memory. The objective is not to use TSVs for all the device chips.

A. The Structure of Imec's Bridge

There are seven separate dice in imec's bridge: wide I/O DRAM, flash memory, logic, two high-density through package vias (TPVs), and two Si bridges. All these dice are with µbumps (Cu pillar + solder cap). The key components are the TPVs (with 5-µm diameter and 50-µm depth TSVs) and the Si bridges (20- to 30-µm thick with 20-µm pitch for the logic die and 40-µm pitch for the TPV die).

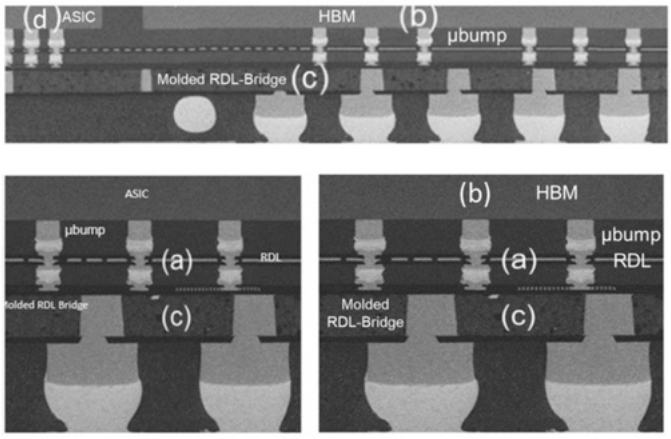

Fig. 50. SEM image of S-connect with molded RDL bridge. (a) RDLs. (b) HBM. (c) Molded RDL bridge. (d) ASIC.

B. The Process of Imec's Bridge

The assembly process of imec's bridge is shown in Fig. 56. It can be seen that, first prepare the seven dice with µbumps and Cu-pillars (Fig. 56[1]). Then attach the die (logic, and two TPVs on a temporary wafer carrier 1 with a temporary bond material [TBM]) (Fig. 56[2]). It is followed by stacking those two Si bridges, wafer-level compression molding an EMC, and grinding the EMC and the backside of the bridges to expose the Cu-pillars (Figs. 56[3] and 56[4]). Then attach another temporary carrier wafer 2 to the backside of those two bridges and Cu-pillar and remove the temporary carrier wafer 1 as shown in Fig. 56(5). It is followed by attaching the memory dice to the logic die and TPV dice, and then wafer-level compression molding (Figs. 56[6] and 56[7]). Then remove the temporary carrier wafer 2, C4 solder bumping, and package singulation as shown in Fig. 56(8).

C. The Challenges of Imec's Bridge

The big challenge of imec's bridge is the stacking of the bridges on the logic die and the TPV die as shown in Fig. 56(3). The surface of the logic die and TPV die must be very flat for the bonding of the Si bridge die. Otherwise, the bridge die shift or tilt could happen as shown in Fig. 57.

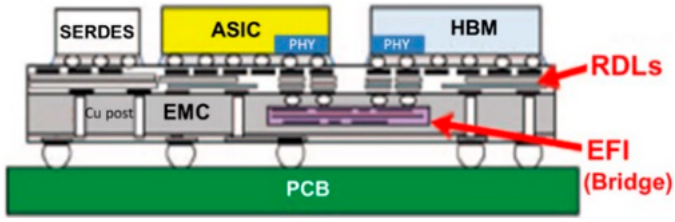

Fig. 51. IME's bridge with EFI.

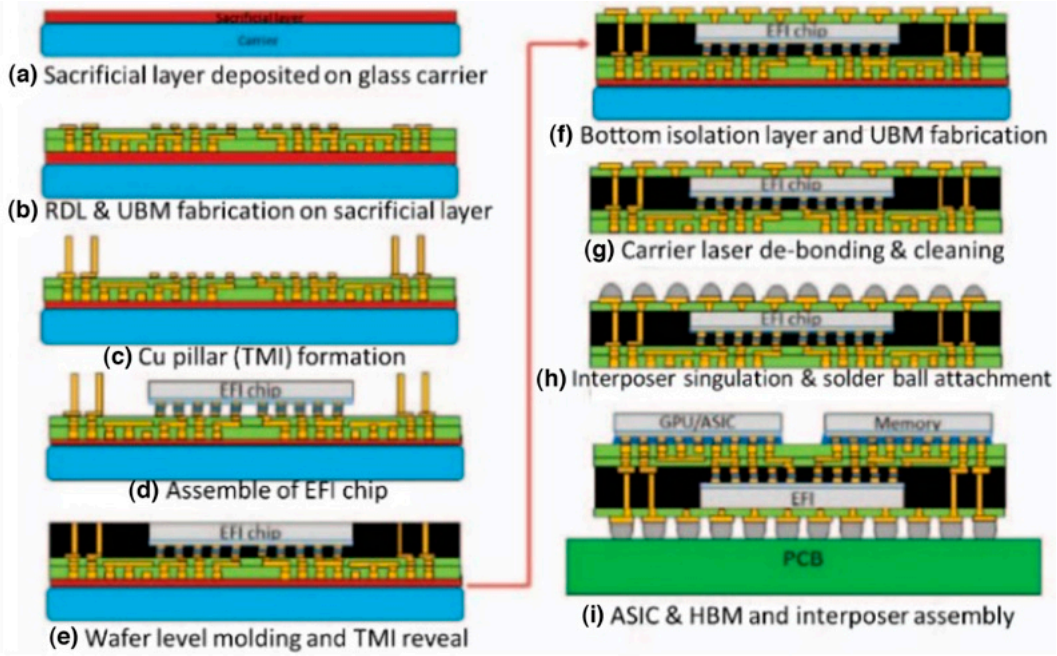

Fig. 52. Process flow of EFI.

Universal Chiplet Interconnect Express Consortium

According to Universal Chiplet Interconnect Express™'s (UCIe™) website, UCIe addresses customer requests for a more customizable, package-level integration—combining best-in-class die-to-die interconnect and protocol connections from an interoperable, multivendor ecosystem. This new open industry standard establishes a universal interconnect at the package-level.

As of August 2, 2022, the UCIe board of directors and leadership (promoters) includes founding members ASE, AMD, Arm, Google Cloud, Intel Corporation, Meta, Microsoft Corporation, Qualcomm Incorporated, Samsung Electronics, and TSMC, and newly elected members Alibaba and NVIDIA.

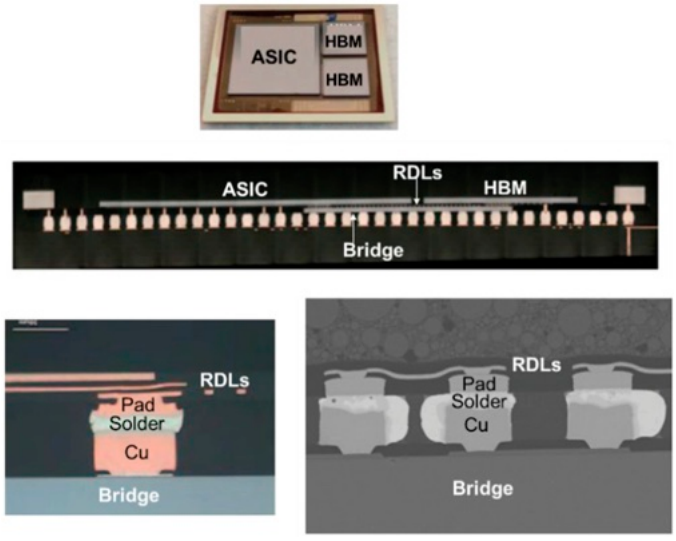

Fig. 53. Images of the EFI.

On March 2, 2022, the consortium published the UCIe 1.0 specification, which provides a complete standardized die-to-die interconnect with physical layer, protocol stack, software model, and compliance testing. Fig. 58 shows the examples of

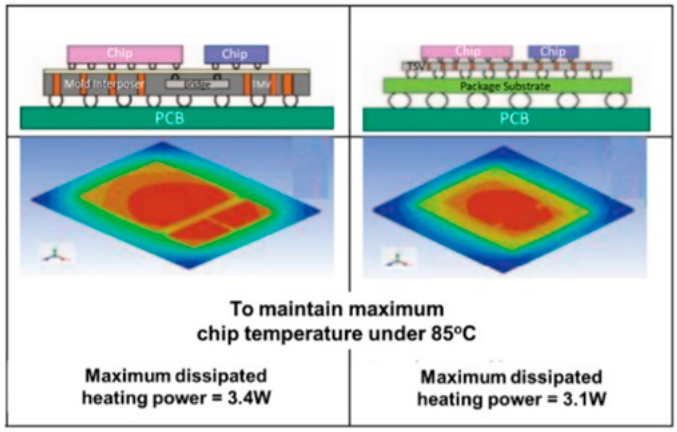

Fig. 54. Comparison between the EFI and 2.5D IC integration.

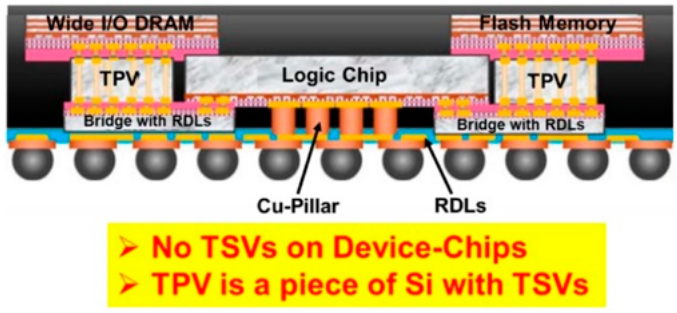

Fig. 55. Imec's bridge for chiplet interconnection.

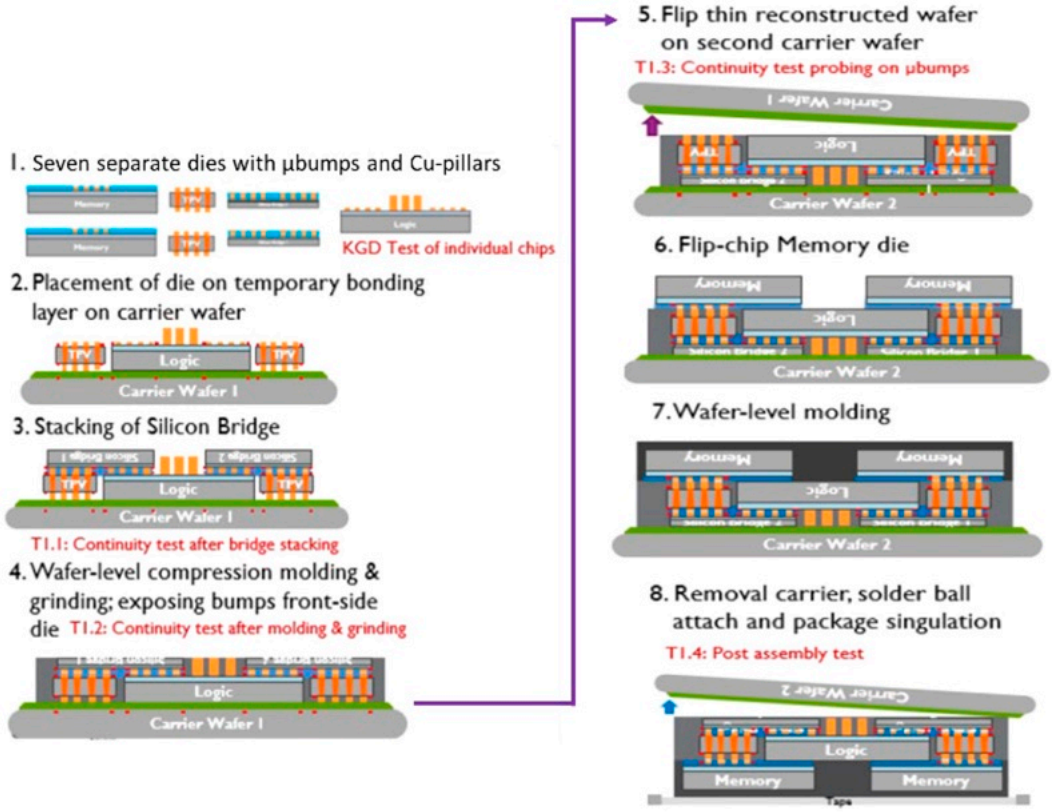

Fig. 56. Process flow for imec's heterogeneous integration with bridges.

standard packaging and advanced packaging with chiplet design and heterogeneous integration, and Table II shows key metrics for standard and advanced packaging.

Unimicron's Hybrid Bonding Bridge

Unimicron proposed the use of Cu–Cu hybrid bonding for the bridge between chiplets in chiplet design and heterogeneous integration packaging (Fig. 59). There are at least two options, one is with C4 bumps on the package substrate and the other is with C4 bumps on the chiplet wafer.

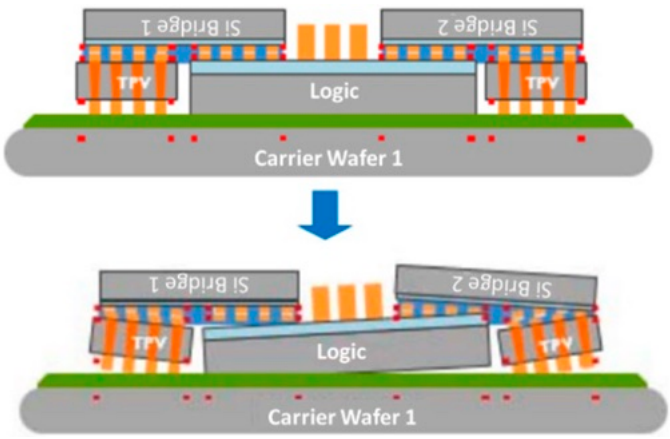

Fig. 57. Challenges for imec's heterogeneous integration with bridges.

A. Hybrid Bonding Bridge with C4 Bumps on the Package Substrate

Fig. 60 shows the process flow of hybrid bonding bridge with C4 bumps on the package substrate. For the bridge wafer, it starts off with CVD to make a dielectric material, such as SiO_2, and then it is planarized by an optimized CMP process to make the Cu dishing. Then, dice the bridge wafer into individual chips (still on the blue tape of the wafer) after coating protective layer on the wafer surfaces to prevent any particle and

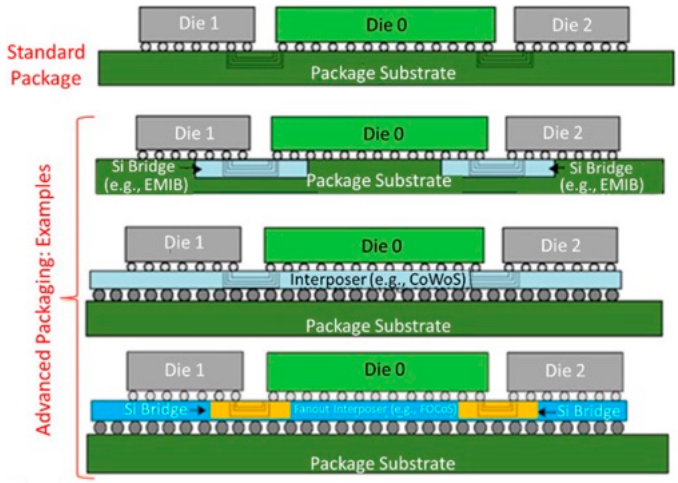

Fig. 58. UCIe's standard and advanced packaging with bridges.

Table II
UCIe 1.0: Characteristics and Key Metrics

Characteristics	Standard package	Advanced package	Comments
Date rate (GT/s)	4, 8, 12, 16, 24, and 32		Lower speeds must be supported—interop, e.g., 4, 8, 12 for 12G devices
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump pitch (μm)	100-130	25-55	Interoperate across bum pitches in each package type across nodes
Channel reach (mm)	⩽25	⩽2	

KP1/Target for key metrics	Standard package	Advanced package	Comments
B/W shoreline (GB/s/mm)	28-224	165-1317	Conservatively estimated: AP: 45 μ; Standard: 110 μ; Proportionate to data rate (4G-32G)
B/W density (GB/s/mm^2)	22-125	188-1350	
Power efficiency target (ρJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5 ns ⩽ 16G, 0.5-1 ns ⩾ 24G		Power savings estimated at ⩾85%
Latency (Tx + Rx)	<2 ns		Incudes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure in Time) ⩽ 1		FIT: #failures in a billion hours (expecting ∼1E-10) w/UCIe Flit mode

contaminant that may cause interface voids during the subsequent bonding process. It is followed by activating the bonding surface by plasma and hydration processes for better hydrophilicity and higher density of hydroxyl group on the bonding surface.

For the chiplet wafer, repeat the CVD for the SiO_2, CMP for the Cu dishing, and plasma and hydration of the activation of the bonding surface. Then pick and place the individual bridge chip on the chiplet wafer and perform the SiO_2-to-SiO_2 bonding at room temperature. It is followed by annealing for covalent bonding between oxide layers and metallic bonding between Cu–Cu contact and diffusion of Cu atoms.

For the package substrate, stencil print the solder paste on the substrate and then reflow into C4 solder bumps. For the final assembly, the bridge + chiplets module is picked and placed on the package substrate, then reflow the C4 bumps.

B. Hybrid Bonding Bridge with C4 Bumps on the Chiplet Wafer

Fig. 61 shows the process flow of hybrid bonding bridge with C4 bumps on the chiplet wafer. It can be seen that comparing with the C4 bumps on the package substrate case, the process steps for the bridge wafer and the chiplet wafer are the same up to bridge-to-chiplet wafer bonding. After that, the C4 bumps are fabricated by wafer bumping on the chiplet wafer. Then dice the chiplet wafer into individual module (bridge + chiplets with C4 bumps). The final assembly is by picking and placing the individual module on the package substrate and reflowing the C4 solder bumps.

Flexible Bridge

In addition to the rigid bridges embedded in build-up organic substrate (e.g., EMIB and DBHi) and fan-out EMC (e.g., Applied

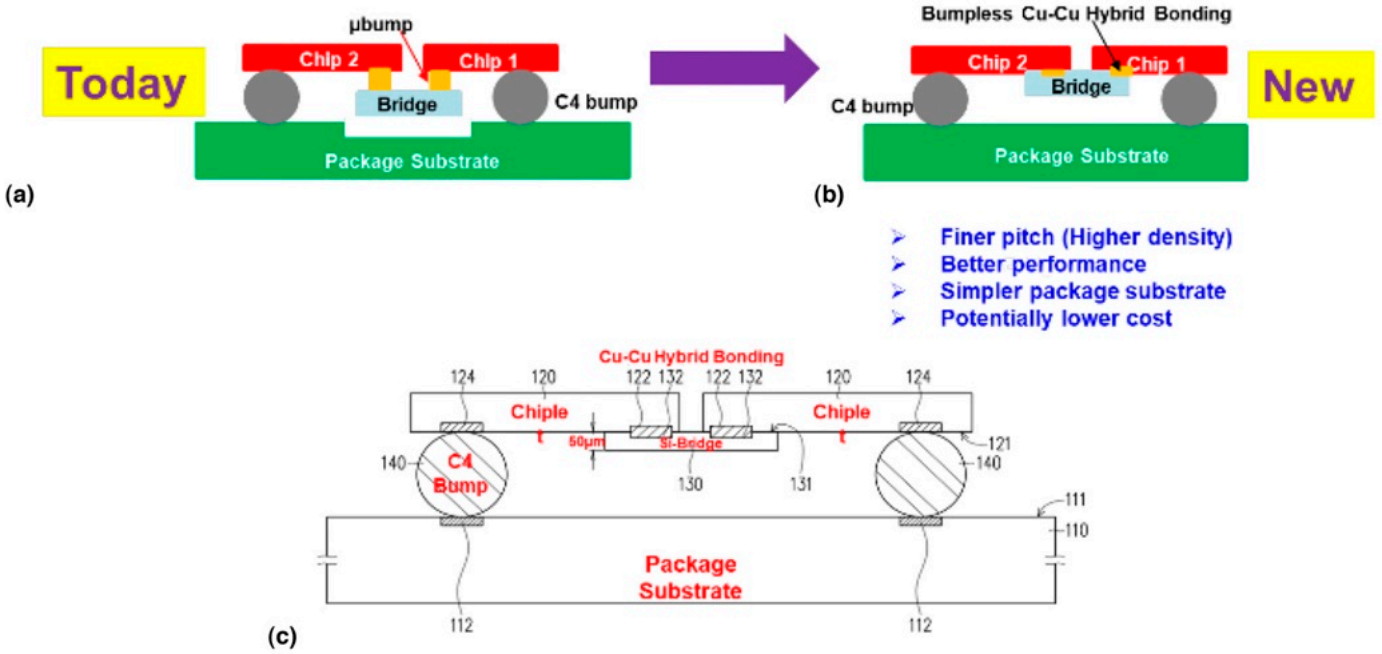

Fig. 59. Hybrid bonding bridge.

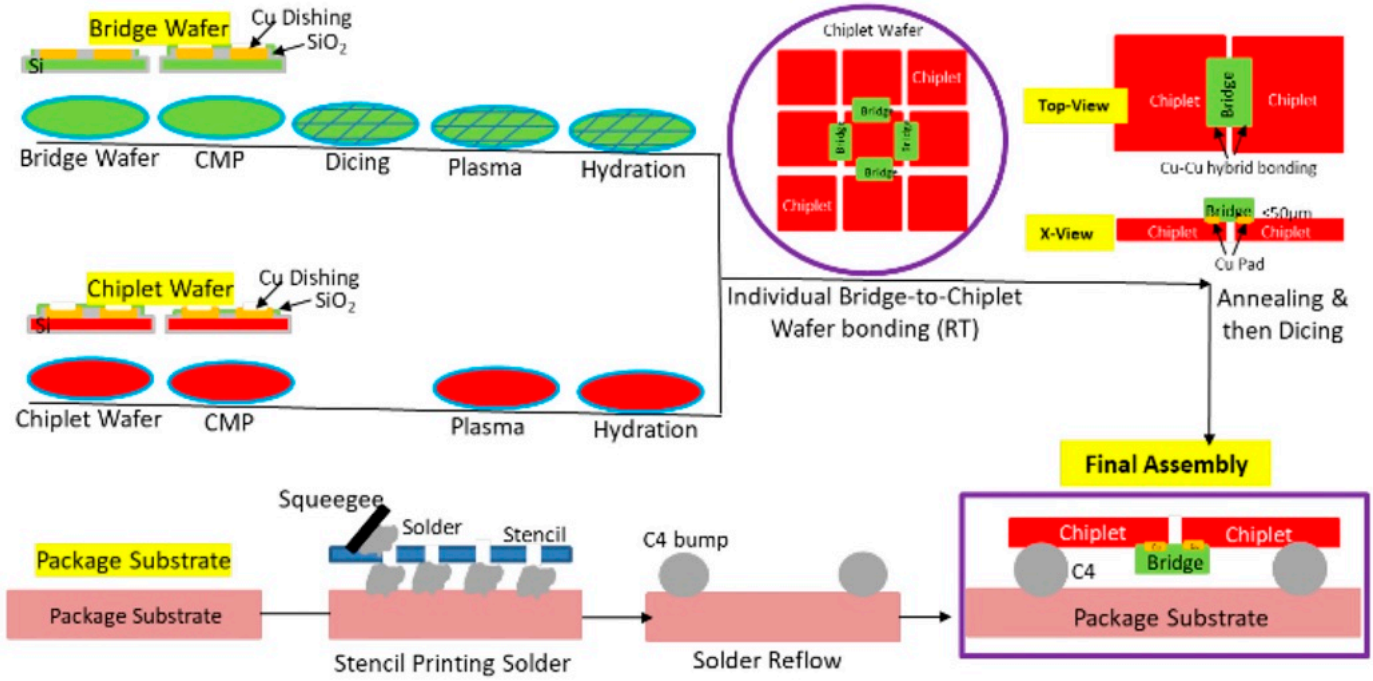

Fig. 60. Hybrid bonding bridge—bridge wafer, chiplet wafer, and package substrate process flow. C4 bumps are on package substrate.

Materials, TSMC, Unimicron, ASE, Amkor, SPIL, imec, and IME), there is the flexible bridge, which is the RDL itself.

The flexible bridge consists of the fine-metal L/S/H conductors in a dielectric polymer, such as polyimide film. The very first flexible bridge patent application US 2006/0095639 A1 was filed by SUN Microsystems on November 2, 2004 (Fig. 62). For high-speed and high-frequency applications, such as millimeter wave frequencies, the dielectric layer can also be a liquid crystal polymer (LCP) and is called LCP-flexible bridge. The assembly process of flexible bridge is very simple and very similar to IBM's DBHi as shown in Fig. 10. However, both the C4 bumps and C2 bumps should be on the chiplet (just like Intel's EMIB case). This is because it is very difficult to do wafer bumping on a flexible bridge. The biggest challenge of the flexible bridge is handling the chiplets and flexible bridges during bonding. Also, there are other challenges if there are more than one flexible

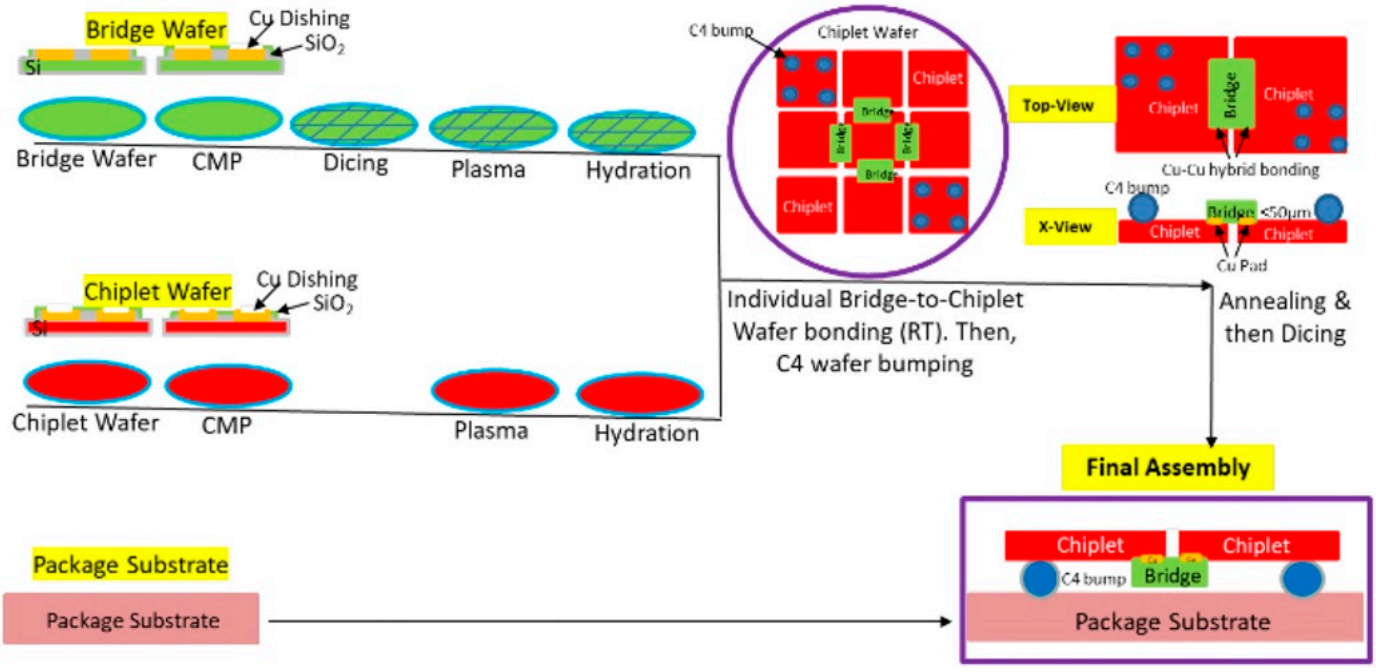

Fig. 61. Hybrid bonding bridge—bridge wafer, chiplet wafer, and package substrate process flow. C4 bumps are on chiplet wafer.

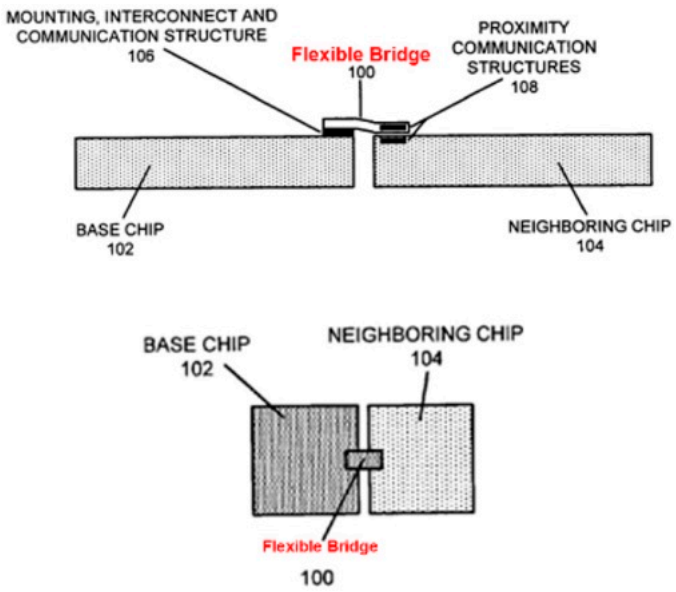

Fig. 62. Flexible bridge.

bridge on a chiplet and there are more than one chiplet with multiple flexible bridges.

Summary and Recommendations

Some important results and recommendations are summarized as follows.

1. Bridge is a small piece of chip without devices but with RDLs to let the chiplets perform horizontal communication.
2. Some bridges also perform vertical communication without devices but with RDLs and TSVs.
3. There are two groups of bridges: rigid bridge and flexible bridge.
4. For rigid bridges, the RDLs are fabricated on a silicon wafer substrate.
5. Today, the rigid bridges are embedded on an organic package substrate, such as the EMIB (Intel) and DBHi (IBM) and embedded in fan-out EMC and connected to fan-out RDLs, such as those by Applied Materials, TSMC, Unimicron, ASE, Amkor, SPIL, IME, and imec.
6. A new rigid bridge called hybrid bonding bridge has been proposed which leads to a very high-performance and very fine pitch package.
7. For a flexible bridge, the RDL comprises the conductor layer and the polyimide dielectric layer.
8. For 5G millimeter wave high-frequency applications, it is recommended to replace the polyimide with the liquid crystal polymer (LCP), i.e., an LCP-flexible bridge.
9. The challenges of various bridges have been provided.
10. Bridge standards are desperately needed. UCIe is the right way to go.

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