Investigation into Impact of Redistribution Layer Design on Thermomechanical Stress in Embedded-Die Package

Masamitsu Matsuura,* Tanemasa Asano, and Haruichi Kanaya

Abstract—Thermomechanical stress generation on a silicon chip in an embedded-die package (EDP) was investigated. Change in thermomechanical stress on the chip with temperature was evaluated using piezo-resistance gauges fabricated on the chip. To investigate the impact of a redistribution layer (RDL) on stress generation, an EDP where filling materials facing the top and bottom sides and the periphery of the embedded die were entirely removed was fabricated. The removal of filling materials was carried out by using the CO2 laser ablation technology. RDL having diagonal paths from the substrate to the chip was designed and fabricated in addition to the conventional orthogonal RDL. RDLs were made of copper. Temperature tests were carried out in the range from −60 °C to 100 °C. The experimental results indicate that, while the origin of thermomechanical stress is a mismatch in coefficients of thermal expansion (CTE) between the chip and the organic substrate, RDL plays a significant role in generating the thermomechanical stress on the chip. The results also show that the diagonal RDL design effectively reduces thermomechanical stress from the orthogonal RDL design owing to its spring characteristic.

Keywords—Embedded-die package, EDP, thermomechanical stress, redistribution layer, RDL, diagonal RDL, laser ablation, piezo-resistance gauge, CTE, heterogeneous integration

INTRODUCTION

The popularity of mobile electronic gears and the Internet of Things (IoT) in people’s daily life keeps pushing semiconductor device technology for further miniaturization of electrical components while enhancing functionality. Heterogeneous integration is a critical vector in the industry for multifunctional and higher power performance. The system-in-package (SiP) integrates multiple chips and passive components on an organic substrate in a single package body and is a popular method among the several integration methods. However, the surface area of a substrate is limited. Therefore, the embedded-die substrate technology that embeds chips and passive components into the substrate is valuable.

In the past years, many types of embedded-die substrate technologies were developed and introduced [1-3]. General benefits of embedded-die technology are enabling higher I/O densities, the integration of both active and passive components vertically and horizontally, and flexible electrical connection with a shorter length than wire bonding. However, due to the technology concept of the package structure, the components embedded into the substrate are covered by substrate materials, such as Ajinomoto build-up film (ABF), prepreg, and so on. Each element encounters residual stress due to material shrinkage, the mismatch of coefficients of thermal expansion (CTE) induced during die embedding processes [4, 5]. As a result, it becomes a significant limitation of using the embedded-die technology for stress-sensitive devices.

In the previous studies [6, 7], we newly designed an embedded-die package (EDP) to investigate the effect of filling materials used to embed a die into a substrate. The experimental results recommend using a lower CTE and lower modulus filling materials to reduce thermomechanical stress on an embedded chip. In addition, the effects of forming slits in the filling material surrounding a chip on thermomechanical stress on the chip have been investigated [8], and it was identified that the thermomechanical stress were generated, even the chip was held only by redistribution layers (RDLs).

In this work, we focus our investigation on the impact of RDL on thermomechanical stress generation on the embedded chip. RDL forms bridges between the embedded chip and the organic substrate and electrically interconnects the embedded chip to the outer components. RDL is usually made of electroplated copper. Typical RDL is in the form of a wire with a thickness of <10 μm. Therefore, its volume is much less than the filling material. However, since the modulus of copper (around 130 GPa at room temperature) is much higher than the filling material, and it keeps a stable modulus value even at higher temperature environments, such as around 123 GPa at 150°C [9]. Therefore, RDL may be of importance in reducing thermomechanical stress on the chip. In this work, we used a newly designed EDP for the assessment of RDL design. This article describes, in fact, that RDL plays a significant role in the generation of thermomechanical stress on the chip, and the design of RDL can reduce thermomechanical stress generation in embedded die.

EXPERIMENTAL METHODS

A. Test Package Structure

Fig. 1 describes schematic illustrations of the fabricated package structures. Fig. 1a is a conventional EDP where the surrounding of the chip is fully filled with resin. Fig. 1b shows a newly manufactured test structure where the filling resin at the top, the bottom, and the periphery of the chip are removed by using laser ablation with a CO2 laser. The chip size was

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3.0 × 3.0 mm² for both test structures. In the conventional EDP, the chip was embedded into the cavity formed in a 150-μm thick core frame with ABF as the filling resin. Four layers of RDL were patterned by electrolytic copper plating using a semi-additive process (SAP). The third RDL contacts the aluminum pads of the embedded die and fan-out onto the core frame, and then it is connected to the fourth RDL using a laser via to form IO pads for electrical measurement. Then, the package top and bottom are covered by a 25-μm thick solder mask.

On the other hand, in the newly fabricated EDP test structure, the chip is mostly isolated from the core frame and the surrounding components, except for the third RDL. In other words, only the third RDL holds the chip. The laser ablation technique using a CO₂ laser was employed to remove ABFs at the top and bottom sides of the chip and at the periphery of the chip. In this article, the space at the top or the bottom of the chip is named gap, and the space at the periphery is named slit. Once finished the isolation using the laser ablation, the core frame is capped using prepreg. Then, it proceeds to the laser via formation using the CO₂ laser, another RDL formation, and solder mask, as same as the conventional EDP. The detailed fabrication process steps and parameters were described in the previous articles [7, 8]. The material sets and mechanical properties used in the fabrication of tested samples are shown in Table I.

An example of the third RDL design that connects the embedded die and core frame is shown in Fig. 2. The package body size is 12.0 × 12.0 mm². The cavity in the core frame for embedding the chip is located in the center of the package body. The cavity size is designed as 3.30 × 3.30 mm², 150 μm wider on each side. The cavity corners were rounded with a 0.5 mm radius, considering placement accuracy during the flip-chip in the embedded-die manufacturing process. A 25-nm thick of titanium and a 150-nm thick of copper using a sputtering method were employed for the seed layer. Then, a 6-μm thick of RDL was plated by conventional copper electroplating using a SAP. The RDL of the fan-out area was designed as a 100-μm width, and the capture pad size of aluminum pad openings which is 70-μm octagon shape, is designed as a 270-μm diameter. The RDL is arranged with a 300-μm pitch, and it fans out perpendicularly to the direction of the four sides of the die. In this article, this direction of RDL defines as 0°. In addition, in the newly fabricated EDP test structure, as shown in Fig. 1b, the slit with 100 μm in width is formed in the periphery of the chip by removing ABF using the laser ablation technique.

In this study, we designed four types of third RDL by changing the angle of RDL. Fig. 3 shows pictures of the chip and RDL taken after forming the third RDL in the fabrication steps. Pictures taken from two samples having different RDL angle θ are shown. Figs. 3a and 3b show views from the frontside (from the third RDL side) and the backside (from the second RDL side), respectively, of the sample θ = +45°. Note that, since slit were formed around the chip, RDL can be observed not only from the frontside, but also from the backside. On the other hand, Figs. 3c and 3d shows views of a sample with θ = ±45°, where RDL with θ = +45° and θ = −45° were designed alternately around the four sides. In this design, RDL at a side is opposed to RDL at a next side.

A list of fabricated samples is given in Table II. In addition to the conventional EDP structure (Sample-1) and the samples having both gaps and slit (Sample-3 to Sample-6), a test sample where only gaps were formed (Sample-2) was prepared. In this sample, both the filling material at the periphery of the chip and RDL hold the chip. Others from Sample-3 to Sample-6 have both gaps and slit while each of them has different RDL design.

### B. Stress Measurement

A test element group (TEG) Si chip, which contained strain gauges and was commercially available in the form of a wafer (WALT Co., Ltd, STAC-0101JY), was used to measure thermo-mechanical stress after packaging. The wafer was thinned from the backside to 150 μm, divided into chips with 3.0 × 3.0 mm²
die size, and then embedded into the package. Each TEG chip has piezo-resistance gauges positioned near the chip center and a corner. The gauges were designed to sense stresses along an axis parallel to the surface of the chip. The positions of both piezo-resistance gauge on the die are highlighted by a red box in Figs. 3a and 3c. The length and width of the piezo-resistance gauge are 350 and 5\( \mu \text{m} \) respectively. Both ends of a piezo-resistance gauge are connected to aluminum I/O pads on the die. The pads were linked through the third RDL to the fourth RDL exposed on the package. For electrical measurements, metal wires were soldered onto the pads of fourth RDLs and connected to a digital multimeter (Keysight Technologies, 34410A) for the resistance measurement.

First, the resistance value at 23°C in the darkroom is measured for all samples since the measurement environment temperature and the light in the measurement room impact the resistance value of piezo-resistance elements. The resistance value at room temperature is treated with initial stress as zero. Then, the packages are placed into a hot and cold oven, and the oven temperature is changed from −60°C to 100°C. The surface temperature of the solder resist of the fabricated package is monitored using a thermocouple attached to the center of the package. The resistance measurement was conducted when the surface temperature of the package reached the target temperature. The stress from measured resistance value was calculated based on chip supplier information, such as stress sensitivity, temperature dependent coefficient of stress sensibility, and so on.

**RESULTS AND DISCUSSION**

Stress values at different temperature environments obtained from change in resistance of piezo-gauges are shown in Fig. 4. Figs. 4a and 4b show thermomechanical stress near the center and the edge of the chip, respectively.

Overall, tensile thermomechanical stress is commonly observed for all samples at elevated temperatures and increases with temperature rise. Table I describes the CTEs of the materials used in the EDPs. The generation of tensile strain can be explained by considering the fact that the CTE of both the core frame material FR-4 and the filling material ABF GX-T31 is larger than that of silicon (3.9 ppm/K) [7]. First, we compare the results from the conventional EDP (Sample-1) and the one in which the gaps on both sides of the chip were formed (Sample-2). Both samples have orthogonal RDL connections to the chip. In the conventional EDP, the stress near the center was around 430 MPa at 100°C, and near the edge was about 602 MPa. The stress value near the edge of the die is higher than near the center, and this phenomenon is commonly observed in all samples. In contrast, the EDP sample, where the gaps but no slit were formed, showed a significant increase in tensile stress. This result indicates that ABF layers on the top and bottom sides of the chip in the conventional EDP impede the thermal expansion of the chip along directions parallel to the chip surface.

Next, we look into the results obtained by changing the angle of RDL access lines to the chip. The samples for this investigation (Sample-3 to Sample-6) were all fabricated to have both gaps and slit, i.e., the chip was held only by the RDL.

<table>
<thead>
<tr>
<th>Type of EDP</th>
<th>Conventional EDP</th>
<th>With gaps</th>
<th>With gaps and laser slit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample#</td>
<td>Sample-1</td>
<td>Sample-2</td>
<td>Sample-3</td>
</tr>
<tr>
<td>Air gaps</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Laser slit</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>RDL angle</td>
<td>0°</td>
<td>0°</td>
<td>0°</td>
</tr>
<tr>
<td>Example of RDL pictures</td>
<td><img src="image_url" alt="RDL pictures" /></td>
<td><img src="image_url" alt="RDL pictures" /></td>
<td><img src="image_url" alt="RDL pictures" /></td>
</tr>
</tbody>
</table>
interconnections. In the case where the RDL access is orthogonal, namely the access angle is 0°, we find from the results shown in Figs. 4a and 4b that significant thermomechanical stress is generated in spite of the fact that the chip is held only by the RDL. The magnitude of stress near the chip center is almost similar to that observed in the conventional EDP (see Fig. 4a), while that near the corner is slightly less than the conventional (see Fig. 4b). When the RDL lines were made at an angle of +45°, on the other hand, the amount of thermomechanical stress on the chip was remarkably reduced. This is true for both near the center (Fig. 4a) and near the corner (Fig. 4b) of the chip. Moreover, we see that making the RDL access line at +22.5° results in the generation of thermomechanical stress whose magnitude is between 0° and +45°.

Two mechanisms can be considered to explain the reduction of the amount of thermomechanical stress by making the RDL line diagonal. One is the rotation of the chip according to the diagonally applied force to the chip. The other is enhanced stress relief in the RDL lines owing to bending deformation of the RDL lines. To investigate this point, a sample in which RDL access lines were made at ±45° was prepared to investigate effects of canceling out rotational forces. The observed magnitudes of thermomechanical stress were close to those obtained from the +45° sample. This result clearly indicates that the bending deformation of RDL access lines plays a key role in reducing thermomechanical stress.

The effect of diagonal RDL access line design on the reduction of the amount of thermomechanical stress is assessed based on a simple mechanical model illustrated in Fig. 5. In the model, an RDL line made of copper bridges the two rigid solids. One is assumed to be a silicon chip, and the other is considered an FR-4 core frame. Both ends of the RDL line are assumed being fixed to the rigid solids. When the package temperature rises, the spacing between the two solids, \( L \), expands due to the difference in CTE between silicon and core frame material. In the RDL access line angle of 0°, the RDL line extends by \( \Delta L_1 \), as illustrated in Fig. 5a. \( \Delta L_1 \) is described based on Hooke’s law as below.

\[
\Delta L_1 = \frac{F_0 L}{Eiw},
\]  

Fig. 4. Thermomechanical stresses observed in the six test structures at temperatures ranging from -60 °C to 100 °C: (a) near the center of the chip and (b) near the corner of the chip.

Fig. 5. Mechanical model of tensile force due the thermal expansion. (a) Orthogonal RDL. (b) Diagonal RDL.
where $F_0$ is a tensile force applied to the RDL, $E$ is Young’s modulus of copper RDL, $t$ is RDL thickness, and $w$ is RDL width. On the other hand, in the case of diagonal RDL design, an expansion and a bending deformation take place simultaneously, as illustrated in Fig. 5b. A tensile force $F_1$ originated from the increase in the spacing $L$ decomposes into two forces, $F_2 = F_1 \cos \theta$ and $F_3 = F_1 \sin \theta$, where $\theta$ is an angle of the RDL from the horizontal. $F_2$ expands along the diagonal RDL while $F_3$ slides the diagonal RDL to the direction perpendicular to the RDL and eventually bends the RDL. The expansion of the diagonal RDL, $\Delta l$, by $F_2$ is described similarly to eq. (1).

$$\Delta l = \frac{F_2 l}{Etw}$$

where $l$ is the length along RDL. Therefore, the extended RDL length in the horizontal direction, $\Delta L_2$, is described in the following equation by trigonometric ratio.

$$\Delta L_2 = \Delta l \cos \theta = \frac{F_1 L \cos \theta}{Etw}$$

Regarding bending deformation, sliding deformation of a beam whose both ends are fixed is equivalent to a combination of two cantilever beams of half-long [10]. Taking this into account, the sliding displacement, $\delta$, produced by $F_3$ is given by,

$$\delta = \frac{F_3 (l + \Delta l)^3}{12EI} \approx \frac{F_1 L^3 \tan \theta}{Etw^3 \cos^2 \theta}$$

where an approximation $l + \Delta l \approx l$ has been applied. The extended RDL length in the horizontal direction $\Delta L_1$ is described by,

$$\Delta L_1 = \delta \approx \frac{F_1 L^3 \tan \theta}{Etw^3 \cos^2 \theta}$$

$$\Delta L_3 = \frac{\delta}{\sqrt{2}} = \frac{F_1 L^3 \tan \theta}{\sqrt{2} Etw^3 \cos^2 \theta}$$

The total expansion in the horizontal direction in the diagonal RDL case becomes $\Delta L_2 + \Delta L_1$. If the expansion of the spacing $L$ is the same for the orthogonal RDL and the diagonal RDL, then

$$\Delta L_1 = \Delta L_2 + \Delta L_3$$

$$\frac{F_0 L}{Etw} = \frac{F_1 L \cos \theta}{Etw} + \frac{F_1 L^3 \tan \theta}{\sqrt{2} Etw^3 \cos^2 \theta}$$

$$\therefore F_0 = F_1 \left( \cos \theta + \frac{L^2 \tan \theta}{\sqrt{2} w \cos^2 \theta} \right)$$

If we define

$$f(L, w) \equiv \left( \cos \theta + \frac{L^2 \tan \theta}{\sqrt{2} w \cos^2 \theta} \right),$$

then

$$F_1 = \frac{F_0}{f(L, w)}$$

Thus, $1/f(L, w)$ gives the ratio of the force applied to the chip in the diagonal RDL structure and that in the orthogonal RDL structure.

Fig. 6 plots $1/f(L, w)$ for $L = 100 \mu m$ as a function of angle $\theta$. Change in values with RDL line width $w$ from 100 to 25 $\mu m$ was also plotted. These plots clearly show the relaxation of thermomechanical stress by the diagonal design of the RDL access line to the chip. For example, the plot suggests that making the RDL access line at 45° for a 100-μm wide line offers about a 50% reduction of a thermomechanical force applied to the chip. This number reasonably explains the experimental results shown in Fig. 4. For example, the thermomechanical stress observed at 100°C near the edge of the +45° RDL design is around 189 MPa, which is around 49% of the 0° RDL sample, while an enhanced reduction was observed near the center.

The plots in Fig. 6 also suggest that a significant relaxation can be achieved at smaller angles by making RDL linewidth smaller. Therefore, diagonal RDL design can be a useful stress-relaxation technique in advanced packaging technology.

The above analysis based on the force per unit length along a periphery of the chip. Therefore, the above RDL design is assumed to be effective for larger chips. However, near the corner of the chip, both elongation and shearing displacements may appear due to orthogonal two forces from the adjacent two sides of the chip. This two-dimensional effect should be taken into consideration also for small chips. For more detailed analysis and design, Finite Element Method (FEM) is needed.

**Conclusions**

Impact of RDL and its design on thermomechanical stress generated on a silicon chip of EDP has been investigated. Test structures were fabricated by using laser ablation to partially or almost completely remove the filling material around the chip. Regarding RDL design, the angle of RDL lines accessing to the chip was changed. The experimental results indicated that RDL plays a significant role to generate thermomechanical stress on the chip due to the CTE mismatch between silicon and the core frame material, i.e., RDL significantly transmit force produced by the CTE mismatch. Designing diagonal RDL access lines has been found to reduce thermomechanical stress. The experimental results from the RDL designed to
cancel out forces in the directions of chip rotation indicated that the reduction of thermomechanical stress is owing to spring function, namely bending deformation of diagonal RDL lines. The results of the analysis based on the mechanical model well explain the experimental observation. The analysis also suggests that the stress reduction effect is pronounced when RDL linewidth shrinks, which implies merit in advanced packaging technology.

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